Test-Structure Free Modeling Method for De-Embedding the Effects of Pads on Device Modeling

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Abstract

On-wafer measurements of devices always include the parasitic effects of probe pads, interconnections, and substrate resistance. In order to extract actual Device Under Test (DUT) parameters from the measurements, several on-wafer test structures such as open, short, and thru are normally required. Various calibration and de-embedding procedures have been developed to use these test structures. [2-11] In this paper a test structure free de-embedding method is demonstrated that finds and removes the influence of parasitics of pad and interconnections with a single measurement. The method uses structural building blocks to construct equivalent circuits of pads, interconnect, and the DUT itself. The equivalent circuit model parameters are extracted simultaneously from the measured s-parameters using the optimization routines in widely used simulators (HSPICE and ADS). The proposed correction procedure is verified by comparison with other methods using an Interdigitated Capacitor (IDC).

Introduction

A device modeling process is important and provides support to a circuit design house. In order to utilize any new fabrication technology efficiently for design work, good behavior models of the various components involved are very important. In integrated circuit design work, for example, good models for transistors are crucial to help obtain fabricated circuits that match designed specifications. In the same manner, accurate, frequency dependent, wide band models of passive components are also very important for successful high-speed circuit design since most practical passive devices have complex geometries, non-uniform current flow, and correspondingly complex field patterns.

In modeling process parasitic effects in on-wafer measurement environment of the devices have a big impact on modeling of DUT and make characterization of the DUT difficult. These parasitic effects come from probe pads, interconnections, and substrate resistance. These influences of parasitics must be subtracted or de-embedded from the measurements to model the DUT. De-embedding is such a correction procedure to extract actual DUT parameters from its measurement environment. As the size of the DUT is shrinking, these parasitics have a significant impact on DUT modeling since the parasitic effects of probe pads and interconnections are comparable to DUT parameters.

In order to extract actual DUT parameters from the measurements environment, several on-wafer test structures such as open, short, and thru are required. Much work has been done to do errorless measurement and various calibration and de-embedding procedures and methods have been developed to use these test structures. [2-11] A more easy, convenient, complete and exact de-embedding method is required to explain high frequency response of DUTs.

In this paper a test structure free de-embedding method is proposed that de-embed the influence of parasitics of pad and interconnections with a single measurement. The proposed correction procedure is verified by comparison with other methods using an IDC. IDCs play an important role in integrated electrical systems. They are used in a wide variety of circuits, including resonators, oscillators, and filters. They are cheap to manufacture, since they are planar devices, unlike the parallel plate or metal-insulator-metal (MIM) capacitor. [14]

In order to verify the proposed de-embedding method's validity, s-parameters extracted from optimized equivalent circuit parameters of pad alone and co-optimized equivalent circuit parameters of pad with DUT were compared with measured s-parameters of pad. The proposed method also was compared with existing de-embedding methods.

This paper consists of three sections. In the first section, various de-embedding methods are compared and demonstrated using a one-step de-embedding method. The second section discusses test structures and measurements, main idea and advantages, procedures of proposed de-embedding methods, and results. Finally, conclusions are presented.

Section I: De-embedding Methods

1. One-step De-embedding Method

The most dominant parasitics are in parallel with the DUT and can be modeled as capacitance with resistance. In this method two measurements are done to obtain DUT parameters: "Pad" and "Pad with DUT" measurement. Figure 1 shows a two-port network "Pad" and "Pad with DUT". Figure 2 shows comparison of y-parameters of "Pad", "DUT", and "Pad and DUT". Effects of probe pad are critical and cannot be ignored in characterization of DUT. One-step de-embedding method was used in this paper in order to make a comparison with proposed method. From the two on-wafer measurements s-parameters are measured and changed into y-parameters. Calculated total y-parameters of "Pad with DUT" are subtracted by pad y-parameters of "Pad" to de-embed DUT parameters. De-embedding procedure is described as [2]:

(1) Measurement of S-parameters: "$[S_p]$" and "$[S_t]$" S-parameters of "Pad", and "Total (Pad with DUT)" respectively.

(2) Changing to Y-parameters: "$[Y_p]$" and "$[Y_t]$"

(3) $[Y_p]=\begin{bmatrix} y_{11p} & y_{12p} \\ y_{21p} & y_{22p} \end{bmatrix}=\begin{bmatrix} G1+G3 & -G3 \\ -G3 & G2+G3 \end{bmatrix}$

(4) Subtraction: $[Y_{DUT}]=[Y_t]-[Y_p]$

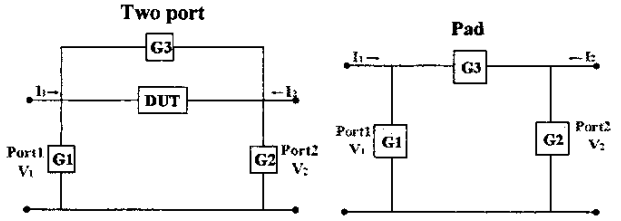

Figure 1. A two-port network "Pad with DUT" and "Pad".

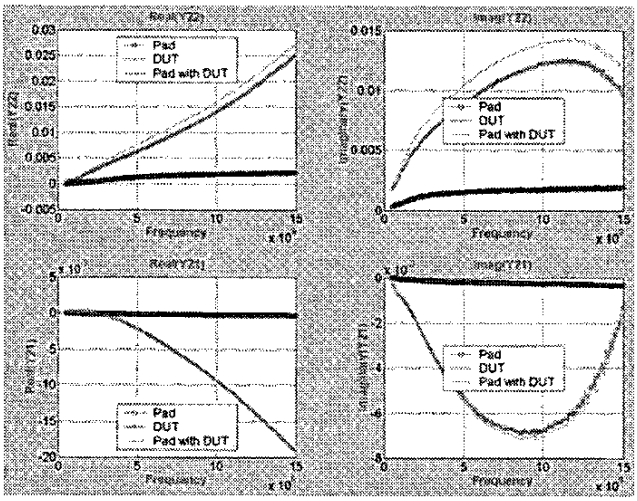

Figure 2. Y-parameters of "Pad", "DUT", and "Pad with DUT".

2. Two-step De-embedding Method

The one-step de-embedding procedure assumes that series parasitics are negligible compared to parallel parasitics but in case of low impedance and high transconductance devices, these series effect must be taken into account. In order to perform the two-step de-embedding procedure, one more dummy test structure is needed: "Short" which can determine interconnect lines behavior (losses and phase shift) caused from the interconnection. In this method three measurements are done to obtain DUT parameters: "Pad", "Short", and "Pad with DUT" measurement. Figure 3 shows a two-port T-network model: "Pad", "Short", and "Pad with DUT". From the three on-wafer measurements s-parameters are measured and changed into y-parameters. First, calculated "Pad with DUT" and "Short" y-parameters are subtracted by "Pad" y-parameters then obtained y-parameters are subtracted to de-embed "DUT" y-parameters. De-embedding procedure is described as [3,5]:

(1) Measurement of S-parameters: "$[S_p]$", "$[S_s]$", and "$[S_t]$" S-parameters of "Pad", "Short", and "Total (Pad with DUT)" respectively.

(2) Changing to Y-parameters: "$[Y_p]$", "$[Y_s]$", and "$[Y_t]$"

$[Y_s]=\begin{bmatrix} y_{11p} & y_{12p} \\ y_{21p} & y_{22p} \end{bmatrix}=\begin{bmatrix} G1+G3 & -G3 \\ -G3 & G2+G3 \end{bmatrix}$

(3) Subtraction 1: $([Y_s]-[Y_p])^{-1}=\begin{bmatrix} H1 & 0 \\ 0 & H2 \end{bmatrix}$

(4) Subtraction 2: $[Y_{DUT}]=\left(([Y_t]-[Y_p])^{-1}-([Y_s]-[Y_p])^{-1}\right)^{-1}$

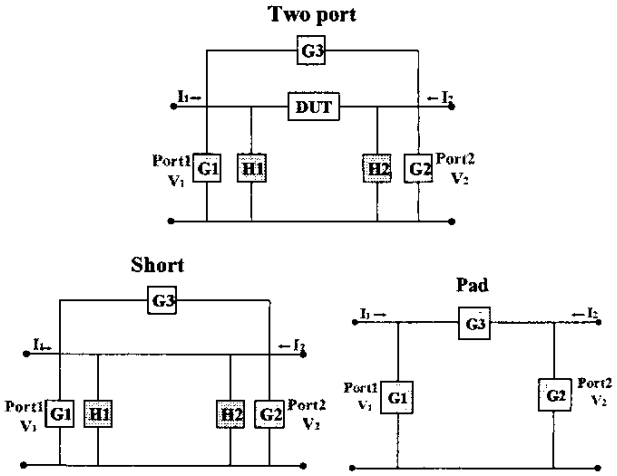

Figure 3. A two-port network "Pad with DUT", "Short", and "Pad".

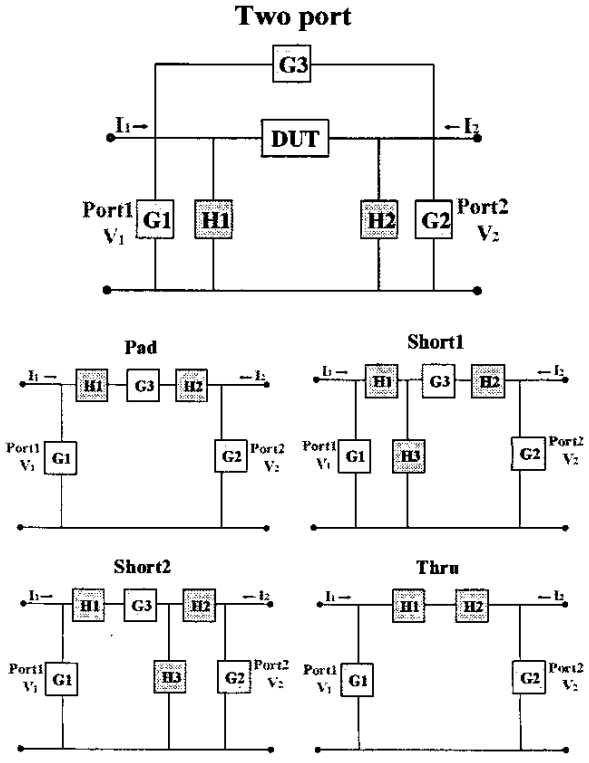

Figure 4. A two-port network "Pad with DUT", "Pad", and "Short1", "Short2", and "Thru".

3. Three-step De-embedding Method

The two-step de-embedding technique is not a sufficient method for accurate modeling of DUT because it ignores the series interconnection between pad and DUT. These parasitics can be removed using "Thru". In order to perform three-step de-embedding procedure, four dummy test structures are needed: "Open", "Short1", "Short2", and "Thru". Figure 4 shows a two-port network models for "Pad", "Short1", "Short2", and "Thru". From the five on-wafer measurements s-parameters are measured and changed into y-parameters.

This method includes three steps. First, subtracting the y-parameter of the open which is shunting the input and output ports. Second, subtracting the series z-parameters derived from measurement of the shorts and thru structures. Finally, subtracting the coupling capacitance between the input and output ports. De-embedding procedure is described as [4,8]:

(1) Measurement of S-parameters: "$[S_p]$", "$[S_{s1}]$", "$[S_{s2}]$", "$[S_{th}]$", and "$[S_t]$" S-parameters of "Pad", "Short1", "Short2", "Thru", and "Total (Pad with DUT)" respectively.

(2) Changing to Y-parameters: "$[Y_p]$", "$[Y_{s1}]$", "$[Y_{s2}]$", "$[Y_{th}]$", and "$[Y_t]$"

$$[Y_p]=\begin{bmatrix} y_{11p} & y_{12p} \\ y_{21p} & y_{22p} \end{bmatrix},\ [Y_{th}]=\begin{bmatrix} y_{11th} & y_{12th} \\ y_{21th} & y_{22th} \end{bmatrix}$$

$$[Y_{s1}]=\begin{bmatrix} y_{11s1} & y_{12s1} \\ y_{21s1} & y_{22s1} \end{bmatrix},\ [Y_{s2}]=\begin{bmatrix} y_{11s2} & y_{12s2} \\ y_{21s2} & y_{22s2} \end{bmatrix}$$

(3) From "Pad":

$$\frac{-1}{y_{12p}}=H_1+H_2+\frac{1}{G_3}=\frac{-1}{y_{12th}}+\frac{1}{G_3} \Rightarrow G_3=\left(\frac{1}{y_{12th}}-\frac{1}{y_{12p}}\right)^{-1}$$

$$y_{11p}=G_1+\frac{1}{H_1+H_2+\frac{1}{G_3}}=G_1-y_{12p} \Rightarrow G_1=y_{11p}+y_{12p}$$

$$y_{22p}=G_2+\frac{1}{H_1+H_2+\frac{1}{G_3}}=G_2-y_{12p} \Rightarrow G_2=y_{22p}+y_{12p}$$

(4) From "Thru", "short1", and "Short2":

$$-y_{12th}=\frac{1}{H_1+H_2},\quad y_{11s1}=G_1+\frac{1}{H_1+H_3},\quad y_{22s2}=G_2+\frac{1}{H_2+H_3}$$

$$H_1+H_2+H_3=\frac{1}{2}\left(\frac{-1}{y_{12th}}+\frac{1}{y_{11s1}-G_1}+\frac{1}{y_{22s2}-G_2}\right)$$

$$H_1=\frac{1}{2}\left(\frac{-1}{y_{12th}}+\frac{1}{y_{11s1}-G_1}-\frac{1}{y_{22s2}-G_2}\right)$$

$$H_2=\frac{1}{2}\left(\frac{-1}{y_{12th}}-\frac{1}{y_{11s1}-G_1}+\frac{1}{y_{22s2}-G_2}\right)$$

$$H_3=\frac{1}{2}\left(\frac{1}{y_{12th}}+\frac{1}{y_{11s1}-G_1}+\frac{1}{y_{22s2}-G_2}\right)$$

(5) From above results:

$$[Y_A]=[Y_{meas}]-\begin{bmatrix} G_1 & 0 \\ 0 & G_2 \end{bmatrix},\ Y_A=\frac{1}{Z_A}$$

$$[Z_B]=[Z_A]-\begin{bmatrix} H_1+H_3 & H_3 \\ H_3 & H_2+H_3 \end{bmatrix},\ Y_B=\frac{1}{Z_B}$$

$$[Y_{DUT}]=[Y_B]-\begin{bmatrix} G_3 & -G_3 \\ -G_3 & G_3 \end{bmatrix}$$

4. Cascade De-embedding Method

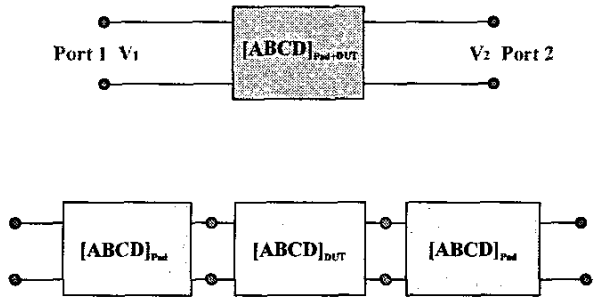

Figure 3. A two-port network and cascade connection of Pad and DUT.

A connection of the pad to DUT is a cascade connection, so ABCD parameters can be applied for the de-embedding procedure. ABCD parameters of pad can be extracted from the measured one-port s-parameter (s_{11}) of the probe pad. The relation between the s_{11} and y_{11_pad} and ABCD-parameters presented in [1,7]

$$y_{11\_pad}=\frac{1}{Z_0}\frac{(1-s_{11\_pad})}{(1+s_{11\_pad})},\quad \begin{bmatrix} A_{pad} & B_{pad} \\ C_{pad} & D_{pad} \end{bmatrix}=\begin{bmatrix} 1 & 0 \\ y_{11\_pad} & 1 \end{bmatrix}$$

Total ABCD parameters of Pad and DUT can be easily determined from the measured s-parameters and expressed in

$$A_{pad+DUT}=\frac{(1+s_{11\_pad+DUT})(1-s_{22\_pad+DUT})+s_{12\_pad+DUT}s_{21\_pad+DUT}}{2s_{21\_pad+DUT}}$$

$$B_{pad+DUT}=Z_0\frac{(1+s_{11\_pad+DUT})(1+s_{22\_pad+DUT})-s_{12\_pad+DUT}s_{21\_pad+DUT}}{2s_{21\_pad+DUT}}$$

$$C_{pad+DUT}=\frac{1}{Z_0}\frac{(1-s_{11\_pad+DUT})(1-s_{22\_pad+DUT})-s_{12\_pad+DUT}s_{21\_pad+DUT}}{2s_{21\_pad+DUT}}$$

$$D_{pad+DUT}=\frac{(1-s_{11\_pad+DUT})(1+s_{22\_pad+DUT})+s_{12\_pad+DUT}s_{21\_pad+DUT}}{2s_{21\_pad+DUT}}$$

The relationship of ABCD-parameters between the "pad", "DUT", and "Pad +DUT" can be expressed in

$$\begin{bmatrix} A_{DUT} & B_{DUT} \\ C_{DUT} & D_{DUT} \end{bmatrix}=\begin{bmatrix} A_{pad} & B_{pad} \\ C_{pad} & D_{pad} \end{bmatrix}^{-1}\begin{bmatrix} A_{pad+DUT} & B_{pad+DUT} \\ C_{pad+DUT} & D_{pad+DUT} \end{bmatrix}\begin{bmatrix} A_{pad} & B_{pad} \\ C_{pad} & D_{pad} \end{bmatrix}^{-1}$$

From the de-embedded ABCD-parameters of DUT s-parameters can be calculated by

$$s_{11\_DUT}=\frac{A_{DUT}+B_{DUT}/Z_0-C_{DUT}Z_0-D_{DUT}}{A_{DUT}+B_{DUT}/Z_0+C_{DUT}Z_0+D_{DUT}}$$

$$s_{12\_DUT}=\frac{2(A_{DUT}D_{DUT}-B_{DUT}C_{DUT})}{A_{DUT}+B_{DUT}/Z_0+C_{DUT}Z_0+D_{DUT}}$$

$$s_{21\_DUT} = \frac{2}{A_{DUT} + B_{DUT}/Z_0 + C_{DUT}Z_0 + D_{DUT}}$$

$$s_{22\_DUT} = \frac{-A_{DUT} + B_{DUT}/Z_0 - C_{DUT}Z_0 + D_{DUT}}{A_{DUT} + B_{DUT}/Z_0 + C_{DUT}Z_0 + D_{DUT}}$$

Section II: Proposed De-embedding Method

1. Fabrication of Test structures and Measurements

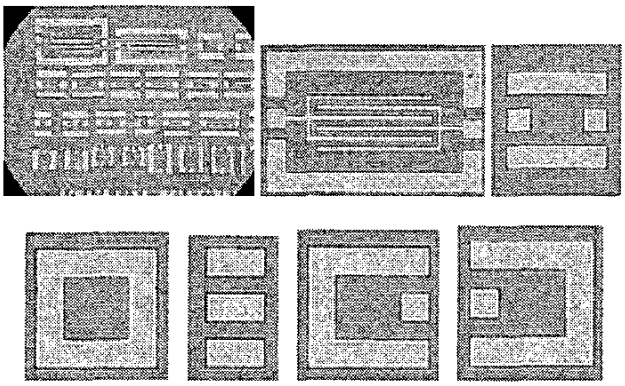

Figure 6. Test bed, IDC, pad, short, thru, short1, and short2.

The test structure design was fabricated at the cleanroom of the Microelectronics Research Center (MiRC), Georgia Institute of Technology. The test structure was fabricated on commercially purchased SiO_2 coated Si substrate. The thickness of SiO2 layer is 4000Å. To further increase the isolation from the probe pads from the substrate, a thick benzocyclobutene (BCB, Cyclotene® 3022-46) was spin-coated on the wafer at a spin speed of 3500 rpm. A small amount of adhesion promoter was dispensed and span dry prior to the coating of BCB. Then, the BCB coated substrate was cured in a N2 flow furnace for 1 hour at 250°C to achieve a 95%~100% degree of polymer conversion. The resulting thickness of BCB is around 3 μm to 3.5 μm with dielectric constant (1 KHz) of 2.65. The metal (Ti/Au, thickness is 300 Å /3000 Å respectively) of probe pad was deposited by e-beam evaporation at high vacuum. Then the IDC pattern are defined by standard photolithography and baked on hotplate at 125°C to harden the etch mask. The Au was etched by heated I2 gold etchant, and Ti was etched by HNO3.

For the high frequency measurements, a HP Network Analyzer was used in conjunction with a Cascade Microtech probe station and ground-signal-ground (GSG) configuration probes. Calibration was accomplished using a supplied substrate and utilization of the Short-Open-Load-Thru (SOLT) calibration method. Data was gathered for each of the test structures at over 201 frequency points between 1GHz and 15GHz and stored with the aid of computer data acquisition software and equipment.

2. Main Idea and Procedure of Proposed Method

Usually on-wafer s-parameter measurement can exactly characterize the behavior of frequency response of DUT at the microwave arena. This measurement based modeling technique has several advantages, it can be applied to arbitrary structures including multi-port devices, it automatically takes into account processing effects such as non-uniform dielectric thickness, processing fluctuations and non-ideal material properties, which would be very difficult to achieve with any method that requires multi-structure measurements, and it reduces the number of measurements necessary to characterize devices. The previous works were cumbersome because of additional test structures and measurements for de-embedding. These complex works are needed because all active and passive components suffer from parasitic effects of pads and interconnections that can affect the electrical behavior of the device at different frequencies.

In this paper a test structure free de-embedding method is demonstrated that finds and removes the influence of parasitics of pad and interconnections with a single measurement. Through this method parasitic effects of pad and interconnections can be de-embedded from only one test structure without any dummy structures or at least with less dummy structures. The method uses structural building blocks to construct equivalent circuits of pads, interconnect, and the DUT itself. These equivalent circuit models of the DUT could be lumped or distributed model for pads and DUT itself and these extracted equivalent circuit model parameters can be obtained using the optimization routines in widely used simulators (HSPICE and ADS).

3. Estimation of Initial Parameter Values from Measurements for Optimization

The equivalent circuit model is obtained by fitting circuit parameter values to the measured s-parameters through optimization. In this procedure the optimized parameters could be diverge depending on initial values of parameters and may deviate from measured s-parameters in case of local minimum points. To find the global minimum point, it is essential to find reasonable and representative estimated initial values of parameters. For estimation of initial values, DC I-V and C-V measurements are done. However these measurements are not suitable for estimation because I-V measurement is usually done at high current level and C-V measurement is done in low frequency range that is not sensitive enough to actual operation range of the DUT [3]. In this method initial values were directly founded from measurements by calculation of initial parameter values using simple equivalent circuit models. This step was done by conversion from measured s-parameters to y or z-parameters. Calculated initial parameter values are presented in Table1.

(1) Estimation of initial parameter values for "Pad" optimization: One-port

In order to find equivalent circuit model of one-port measurement such as pad, simple series RC model was assumed and initial parameter values were calculated (Fig. 7). These estimated values show good agreement with measured s-parameter in Fig. 8 and best result was obtained after optimization procedure.

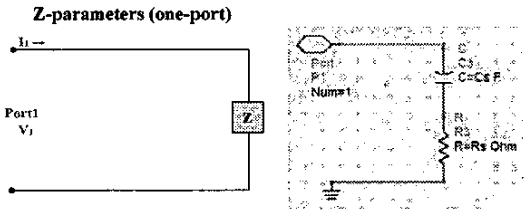

Figure 7. A one-port network and equivalent circuit.

$$s_{11} \Rightarrow z_{11} = R_s + jX_s = R_s + \frac{1}{jwC_s}$$

$$R_s = \mathrm{Re}al(z_{11}), C_s = \frac{-1}{w\,\mathrm{Im}ag(z_{11})}$$

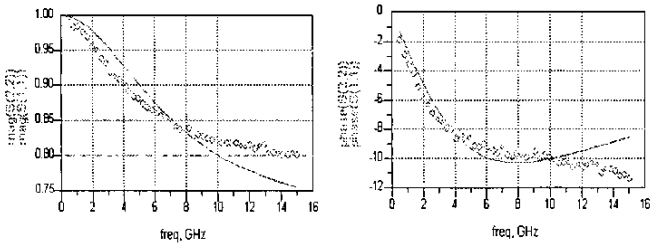

Figure 8. Result of pad using calculated initial values.

(2) Estimation of initial values for DUT and "Pad with DUT" optimization: Two-port

In order to find equivalent circuit model of "DUT" and "Pad with DUT" measurement, simple series and parallel RC model was assumed and initial parameter values were calculated (Fig. 9). These estimated values show good agreement with measured s-parameter in Fig. 10-11 for "DUT" and "Pad with DUT" and best result was obtained through optimization procedure.

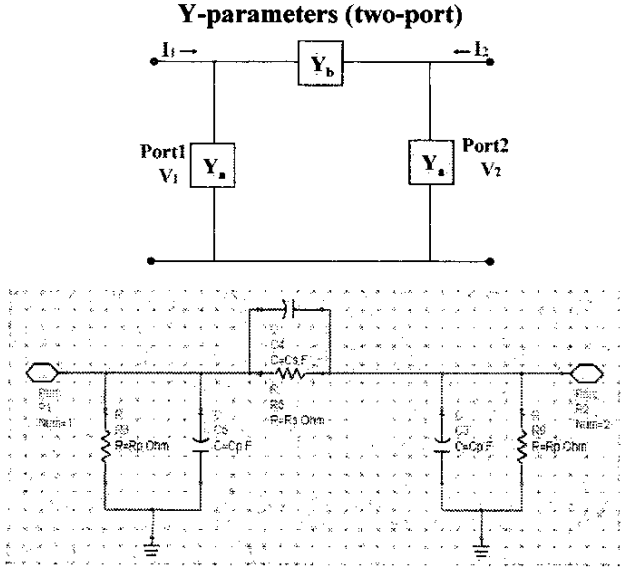

Figure 9. A two-port network and equivalent circuit.

$$y_{11} = \frac{I_1}{V_1}\Big|(V_2 = 0) = Y_a + Y_b, y_{21} = \frac{I_2}{V_1}\Big|(V_2 = 0) = -Y_b$$

$$Y_a = \frac{1}{R_p} + jwC_p, Y_b = \frac{1}{R_s} + jwC_s$$

$$R_s = \frac{-1}{\mathrm{Re}al(y_{21})}, C_s = \frac{-\mathrm{Im}ag(y_{21})}{w}$$

$$R_p = \frac{1}{\mathrm{Re}al(y_{11} + y_{21})}, C_p = \frac{-\mathrm{Im}ag(y_{11} + y_{21})}{w}$$

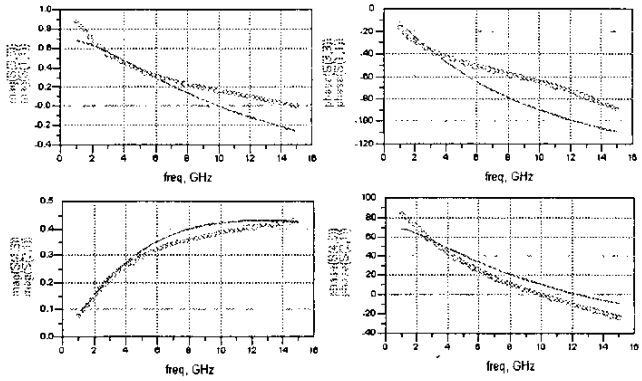

Figure 10. Result of DUT using calculated initial values.

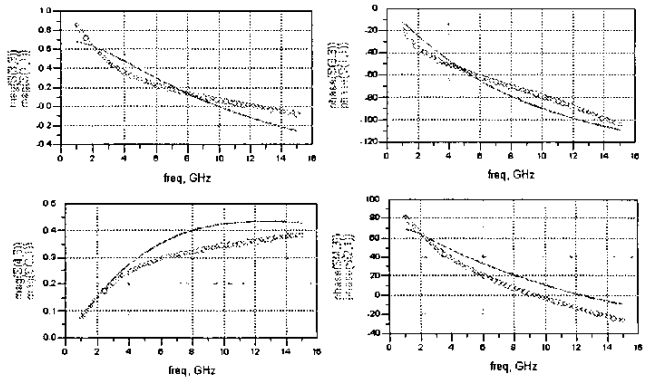

Figure 11. Result of "Pad with DUT" using calculated initial values.

4. Result of Optimization

Optimized parameter values were found for "Pad", "DUT", and "Pad with DUT" from the initial parameter values that were calculated with the previous procedure. S-parameters extracted from optimized equivalent circuit parameters of pad alone and co-optimized equivalent circuit parameters of pad with DUT were compared with measured s-parameters of pad to verify this method's validity. Figure 12 shows schematic and result of optimization for pad alone. Figure 13 shows schematic and result of optimization for DUT alone. These s-parameters were obtained by the one-step de-embedding method. Figure 14 shows a test structure that is partitioned into three components: pad (from dotted plane A to B), IDC (from dotted plane B to B'), and pad (from dotted plane B' to A') and these components were optimized simultaneously. Figure 15 shows comparisons in magnitude and phase of pad for measured, co-optimized with DUT, and optimized pad alone. This result shows very good agreement between this modeling methodology and other de-embedding methods.

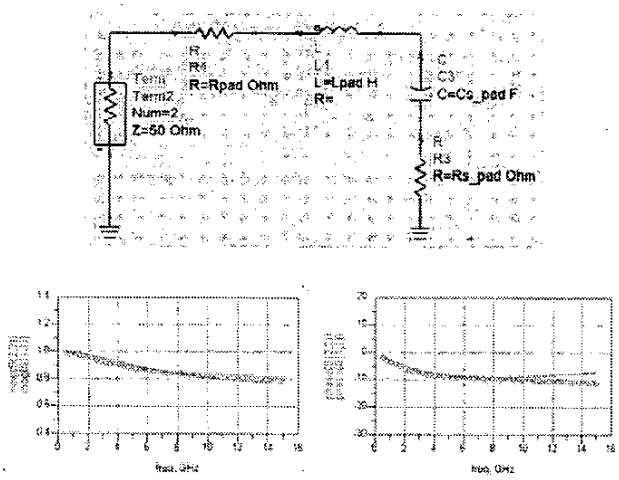

Figure 12. Schematic and result of optimized pad.

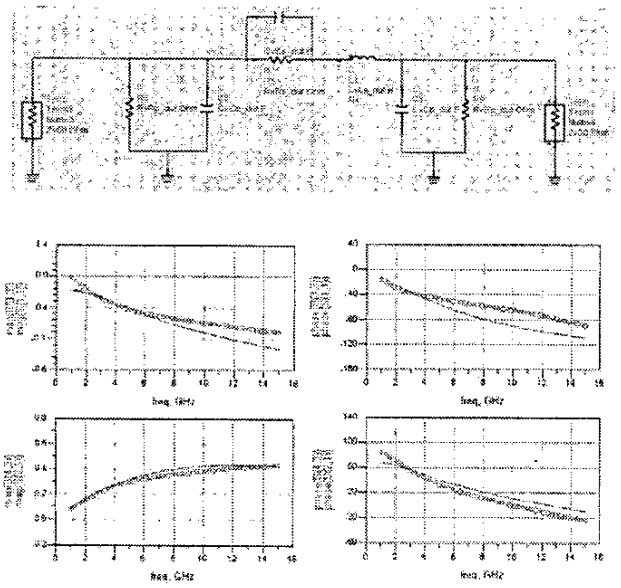

Figure 13. Schematic and result of optimized DUT.

Conclusions

In order to characterize the DUT more easily and conveniently, a de-emdedding method was proposed. The validity and accuracy of a test structure free de-embedding method is demonstrated that finds and removes the influence of parasitics of pad and interconnections with a single measurement. This method is quick, accurate, and convenient for RF device modeling.

Acknowledgments

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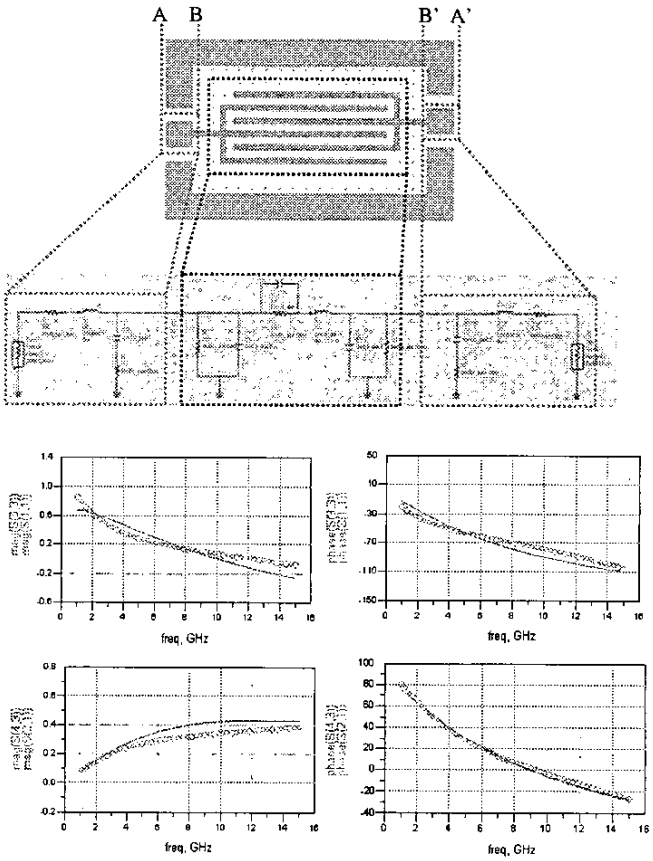

Figure 14. Figure 1. Test structure (pad with IDC), schematic, and equivalent circuit models of pad and IDC itself with a comparison of measured test structure s-parameters and simulated or optimized equivalent circuit model s-parameters.

	Calculated Initial parameter values from assumed simple equivalent circuit model	Optimized parameter values
Pad	C_{s_pad}=72.9 (pF) R_{s_pad}=280.2 (Ω)	C_{s_pad}=70.07(pF) R_{s_pad}=250.3 (Ω) L_{pad}=0.499 (nH) R_{pad}=60.12 (Ω)
DUT	C_{s_pad}=175.9 (pF) R_{s_pad}=4563.5 (Ω) C_{p_pad}=163.2 (pF) R_{p_pad}=300.4 (Ω)	C_{s_pad}=165.4 (pF) R_{s_pad}=4281.3 (Ω) C_{p_pad}=132.9 (pF) R_{p_pad}=210.3 (Ω) L_{s_pad}=1.023 (nH)
Pad with DUT	C_{s_dut}=195.3 (pF) R_{s_dut}=4849.3 (Ω) C_{p_dut}=174.2 (pF) R_{p_dut}=343.6 (Ω)	C_{s_pad}=63.9(pF) C_{s_dut}=154.3 (pF) R_{s_pad}=243.2 (Ω) R_{s_dut}=3998.3 (Ω) L_{pad}=0.63 (nH) C_{p_dut}=145.8(pF) R_{pad}=53.8(Ω) R_{p_dut}=198.5 (Ω) L_{s_dut}=1.59(nH)

Table 1. Initial and optimized parameter values.

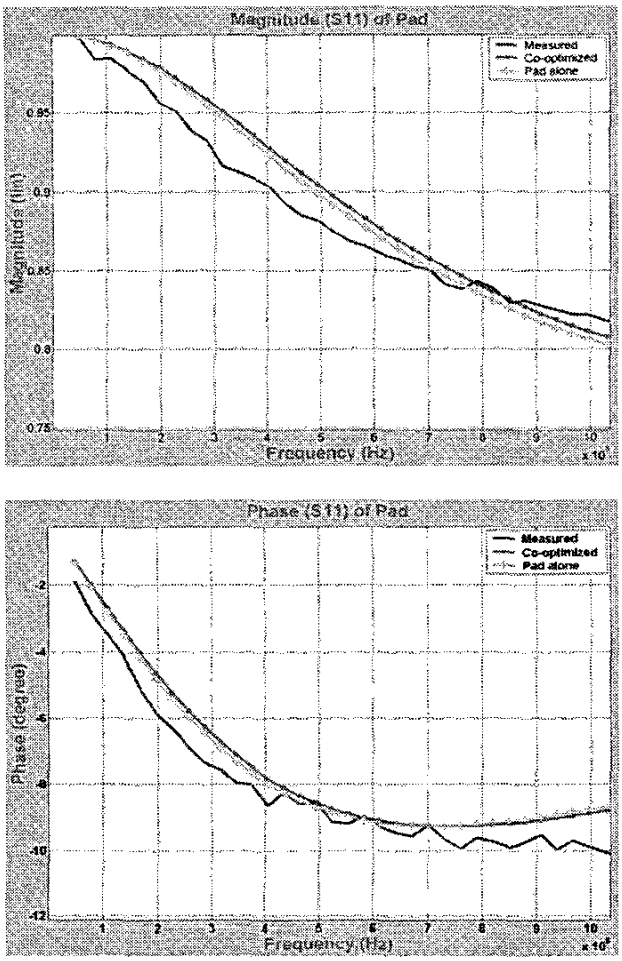

Figure 15. Magnitude and phase of pad for measured, co-optimized with DUT, and optimized pad alone.

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