Comparison of Electrical and Optical Interconnect

Jaemin Shin, Chung-Seok Seo, Ananthasayanam Chellappa, Martin Brooke, Abhijit Chatterjee and Nan M. Jokerst
Department of Electrical and Computer Engineering
NSF Packaging Research Center
Georgia Institute of Technology
Atlanta, GA 30332
Email: {jaemin, andyseo, ananth, martin.brooke, chat, nan.jokerst}@ece.gatech.edu

Abstract

In this paper, we present a comparison between electrical and optical interconnect for chip-to-chip signaling in terms of data rate and system power consumption on FR4 circuit boards. The results show that optical interconnection is the only functional technology for a single serial line of 20cm length at a 10Gbps data rate. Low power CMOS logic driving parallel unterminated copper interconnect on FR4 substrates should be replaced by terminated transmission lines at 10cm lengths for 10Gbps aggregate throughput and at 20cm for 1Gbps aggregate throughput. Terminated copper transmission line interconnect on FR4 substrates can achieve 10Gbps per line operation at 20cm, provided no vias are used in the interconnect, or via technology with low reflection loss is developed. With vias, terminated copper transmission line interconnect must be replaced at 20cm for 10Gbps per line, however, 4 parallel terminated transmission lines with vias each running at 2.5Gbps can achieve 10Gbps aggregate communication over a 20cm length. Thus, serial optics should only be used to replace 4 parallel electrical transmission lines if the power dissipation of the optical driver circuitry is less than 4 times the 2.5Gbps electrical driver power consumption.

For electrical interconnect, two interconnection technologies were studied. The first technology uses ideal sources to drive a single serial terminated 50Ω copper transmission line on FR4 both with and without vias. The second technology uses conventioinal CMOS digital interface circuits and parallel unterminated, 50Ω transmission line interconnect of width 16, 32, and 64bits made from copper on an FR4 substrate. These two technologies represent low power CMOS and the ultimate limit of FR4 copper traces for unequalized digital signaling. For optical interconnect, commercial SiGe optoelectronic laser driver circuit technology and published optical waveguide data were used to determine performance limits. Compliance with the IEEE 802.3ae XAUI interface eye mask was used to determine acceptable data transmission in all cases.

1. Introduction

Since the semiconductor diode laser was developed in the 1960s, optics has been an interesting area in digital computation because it has better characteristics compared to electrical interconnect.

As electrical computational systems are getting faster and larger, electrical interconnect becomes a critical hurdle to improve overall system performance because it causes crosstalk, reflection, switching noise, clock skew, timing jitter, etc. Due to its characteristics such as high spatial bandwidth, high speed, low crosstalk, etc, optical interconnect is one of the best possible solutions that overcome the disadvantages of electrical interconnect.

The effort that tried to seek the breakpoint beyond which optical interconnect dominates over electrical interconnect was made from several viewpoints in the 1990s[1-7]. The interesting result is that electrical interconnect should be replaced with free-space optical interconnect over around 3cm distance[4] because free-space optical interconnect dominates electrical interconnect from the system power dissipation's point of view when the interconnect length is over 3cm. From the speed point of view, free-space optical interconnect is always faster than electrical interconnect.

In 1992, S. E. Schacham, *et al*, presented a comparison between electrical interconnect and optical waveguide interconnect[1]. According to their results, there is no obvious benefit in replacing electrical interconnect with optical interconnect unless there is significant distance involved. However, the possibilities of the use of optical interconnect were discussed.

The performance in terms of processing throughput, power consumption and size of computer and network systems is widely considered to be limited by the performance of cost effective chip-to-chip board level interconnect. Although CPU core clocks are in the GHz, bus clock rate is generally just a few hundred MHz on FR4. Thus, it is reasonable to develop optical interconnect as a substitute for the electrical interconnect in the computer and network system.

In this paper, we present models for electrical interconnect on FR4, HSPICE simulatin results, measurement results of two types of transmission line and comparison between simulation and measurement using eye diagram. Transmission lines with and without vias are modeled for electrical interconnect and the effect of the via on the eye diagram is shown by varying line length and signal frequency. For optical channel, polymer waveguide data was referred to match the electrical channel. Herein, the performance of conventional buses to the transmission line and the optical waveguide alternatives was investigated and the superiority for these technologies according to data rate and channel power dissipation is estimated. Furthermore, the unterminated CMOS link[16] and commercial SiGe optoelectronic circuit technology[10-13] are compared to conclude the dominance with regard to data rate and power consumption for a variety of aggregate throughputs and interconnect lengths. The IEEE 802.3ae XAUI interface eye mask is used as a guide for acceptable data transmission in all cases. On the basis of the entire investigation result, electrical and optical interconnect are discussed as a final point.

2. Approach to off-chip electrical interconnect

The selection of compared objective is important to get reliability for the following step. The transmission line model is specified and the simulation and the measurement for the circuit with transmission line is described to compare with optical interconnect.

2.1. Simulation

Eye diagrams and power consumption in the circuit are intimately related with interconnect length and data rate.

In this section, CMOS interconnect with transmission line is simulated using HSPICE transient simulator over the interconnect length and the signal frequency. First of all, the transmission line needs to be generated for CMOS interconnect channel and it would be compared to fabricated transmission line in order to support fully the following simulation. HSPICE model of transmission line shown in Figure 1 is the single lossy U model on FR4 which is supplied from commercial board supplier. Eye diagrams with pseudo-random bit (PRB) input are presented at different frequencies as high as 1, 2.5 and 10Gbps and different lengths as long as 1, 10 and 20cm. The IEEE 802.3ae XAUI interface eye mask is applied as a guide for acceptable data transmission in all eye diagram. The trend of electrical transmission capability as variables of data rate and interconnection length is obtained from this simulation.

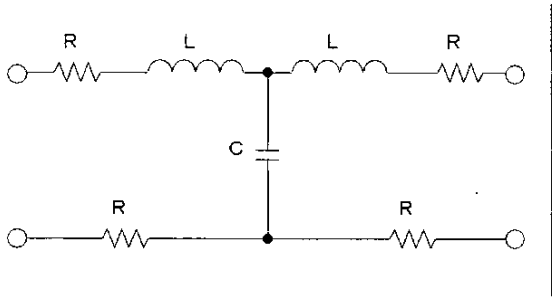


Figure 1. Schematic of lossy U model transmission line

Using this transmission line model, CMOS interconnect with transmission line which does not have termination is shown in Figure 2

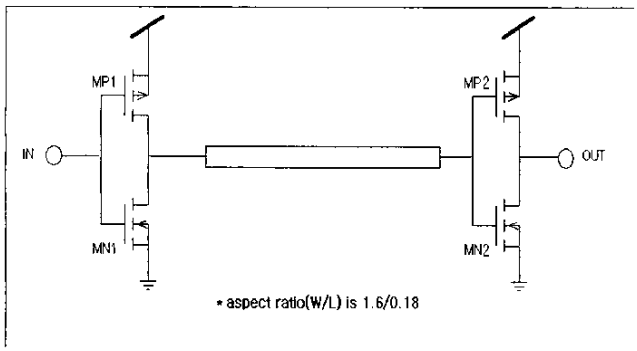


Figure 2. Schematic of CMOS inverter interconnect

This circuit is simulated with the above transmission line model in Figure 1 and TSMC 0.18μm CMOS transistor model from MOSIS. This CMOS circuit normally works up to around 100Mbps and it needs wider data buses for Gbps speed. Consequently 16, 32 and 64bit wide data buses are considered to get satisfactory eye diagrams for 1, 2.5 and 10Gbps data transmission

The important optical issue is acquainted with the power consumption problem at the driver and receiver circuits. Power consumption is extracted from the HSPICE simulations for comparison. By taken together, each trend of eye diagram, its derivative acceptance table and power dissipation give us some ideas to compare with optical interconnect.

2.2. Measurement

Transmission lines of the different lengths were on FR4 board is designed, fabricated and measured with termination at different lengths and signal frequencies. This transmision line structure, a prototype for simulation model, is conducive to attaining consistent results.

1, 10 and 20cm long transmission lines that are 2500μm wide for 50Ω impedance matching were fabricated on FR4 that has 4.34 relative dielectric constant. All transmission lines are conventional microstriplines.

Normally, board-level interconnect is affected by elements such as vias. To recognize the effect of via, transmission lines were examined with and without via. Via size is specified to the minimum fabricating capability of 20 mils. Transmission lines with via were connected from top layer through via path to bottom layer on two layer structure.

Eye diagrams for 0.5, 2.5 and 10Gbps data rates from 2^7-1 PRB input pattern were captured for different length on the digital oscilloscope. The result of the measurement and simulation proves the reliablility of the following simulation of CMOS inverter interconnet and the effect of via. In addition, transmission line without via is measured to display S11 and S21 data that is useful to analyze reflected signal and transmitted signal degradation.

3. Approach to optical interconnect with waveguide

For the board-level optical interconnect, optical waveguide on the board and laser driver are specified and studied to compare to the electrical part.

The developement of advanced optical device stimulated the development of various higher quality optical waveguide. Among these optical waveguides, the optical waveguide from AlliedSignal manufacture whose polymer type is Halogenated Acrylate[9] is considered because its good optical loss property complies with 50Ω charateristic impedance matching of electical transmission line. Optical loss data at 840, 1300 and 1550nm wavelength is refered from the datasheet[9].

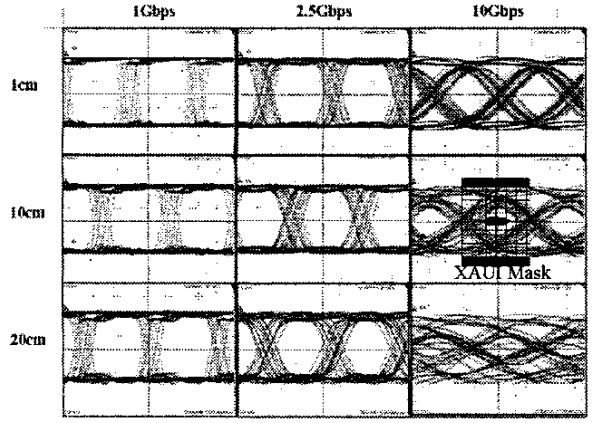
In general, it is known that optical channels have superior speed performance compared to electrical interconnect due to the intrinsic property of the medium[1-7]. Unsurprisingly, power consumption on driver circuit becomes a critical issue between them. Herein, commercial SiGe HBT laser drivers from Maxim integrated product[10-13], which have respectively 1.25, 2.5 and 10Gbps data rates, are considered as references for the eye diagram and the power consumption.

4. Results and Analysis

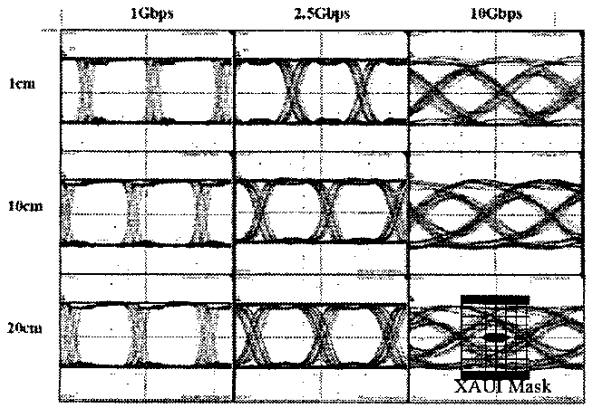
It is necessary to compare optical and electical interconnect from the viewpoint of influential factors. In this paper, superiorities of data rate, channel power dissipation and power consumption in the driver are obtained as a function of channel length by measurement, simulation, and data survey.

The electrical transmission line has been studied on various approaches by RF and analog laboratories and there are many models and simulations for it. It can be said that its model is likely to change with each material property, nonlinearity, and unexpected factor when simulating. Accordingly, it is necessary to establish reliability of the transmission line model and simulator by measuring the transmission lines fabricated. Before discussing simulation of transmission line, it is attractive to observe the effect of accompanying connection element like via. Thus, transmission line with via was additionally measured in the same condition of transmission line without via. For the measurement configuration, all transmission line measurement was performed with termination to reduce the reflection loss. Measurement and comparison are more significant for signal analysis in the high frequency system.

As shown in Figure 3(a) and (b), vias have a critical effect on data transmission according to the eye pattern.



(a) Transmission line with via

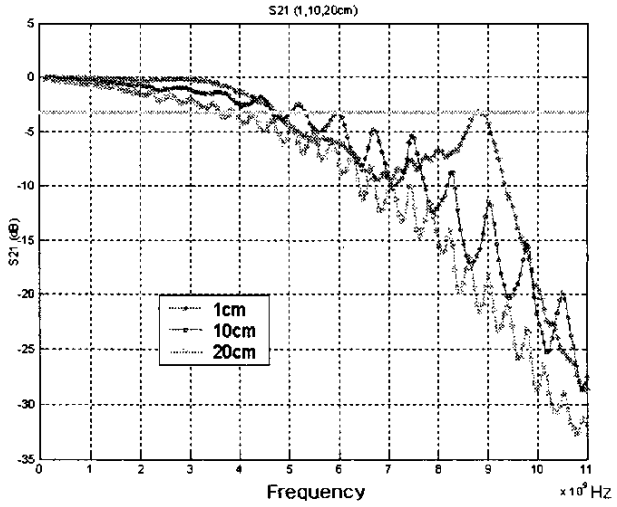


(b) Transmission line without via

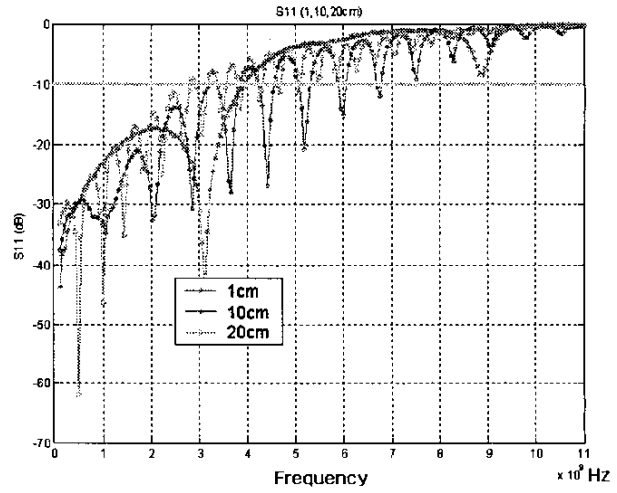
Figure 3. Measured eye diagram of transmission line

Moreover, the eye on the 20cm long transmission line with vias is almost closed at 10Gbps as compared to the one without vias. Therefore, a 20cm long terminated transmission line with via has to be changed to 4 parallel same lines at 2.5Gbps for 10Gbps aggregate data rate. It is indicated from the above result that more element effects on board which may be ignored at low frequency need to be taken into account at high frequency.

To view intrinsic characteristics of transmission line, S-parameter data was extracted from transmission line structures without vias. As presented in Figure 4(a) and (b), the S-parameter data reveals the transmitted and reflected signal on transmission line without vias.



(a) S21 of transmission line



(b) S11 of transmission line

Figure 4. Measured S-parameter of transmission line without via

In the worst case, S21 on the 20cm long line stays less than 3dB until 4GHz and then falls more sharply. S22, for the same case the above, has less than −10dB up to 2.5GHz. It is evident that the transmission line simulation shows an expected trend in that longer lines generate more oscillation

on both figures. Therefore, in this paper, uncoupled straight transmission lines were employed to compare to simulation results.

The transmission lines mentioned above were simulated using HSPICE under the same conditions as the lines measured to obtain the eye diagrams shown in Figure 5.

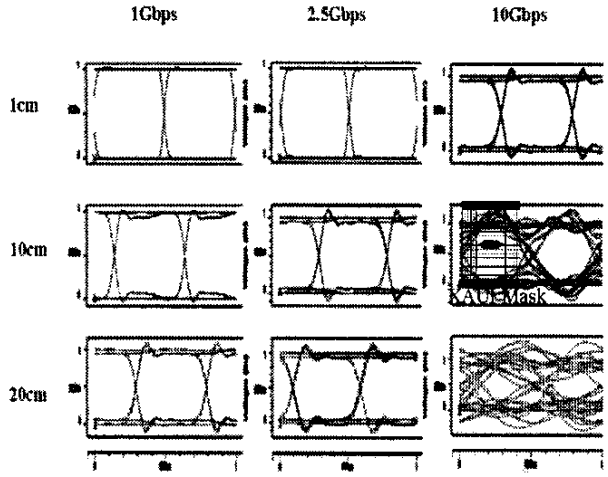


Figure 5. Simulated eye diagram of transmission line

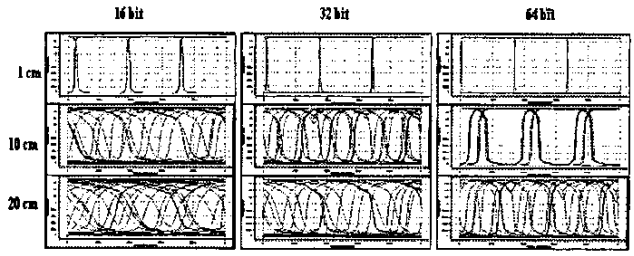
The eye diagram from simulation is similar to the measured result and all but the 20cm line at 10 Gbps are acceptable for the IEEE 802.3ae XAUI interface eye mask. Hence the simulated model can be said to be a suitable electrical interconnect model for the following circuit interconnect simulation.

To transmit more data over longer length electrically, numerous approaches have been attempted at the circuit level such as CMOS, LVDS, CML and PECL. In this paper, to show the trend of data rate and power consumption with different line lengths, simple unterminated CMOS inverter interconnect with TSMC 0.18μm transistor and transmission line without via was designed and simulated for competitively low power consumption instead of the speed benefit that some other driving scheme might have. Restricted data rate on single channel can combine with multiple parallel channels for higher aggregate speed although with higher total power consumption.

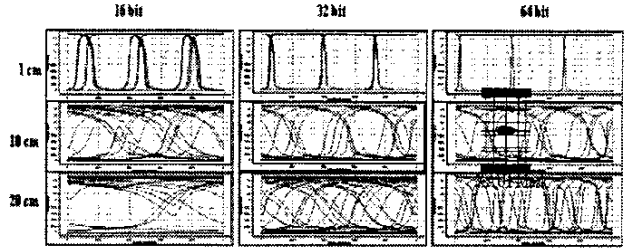
16, 32 and 64bit wide data channels were utilized for 1, 2.5 and 10Gbps CMOS interconnect like eye diagrams in Figure 6(a), (b) and (c).

. All eye diagrams from simulation are judged with the IEEE 802.3ae XAUI interface eye mask and the acceptance table obtained is presented is Figure 6(d).

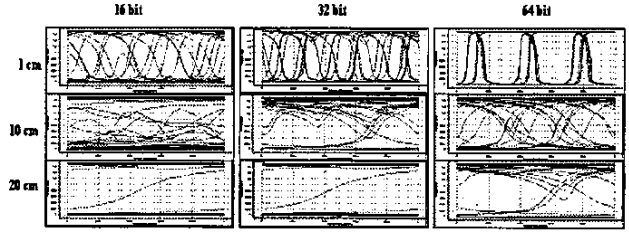
Figure 7 shows the eye diagrams for optical laser driver data from Maxim integrated products.



(a) 1Gbps eye diagram



(b) 2.5Gbps eye diagram

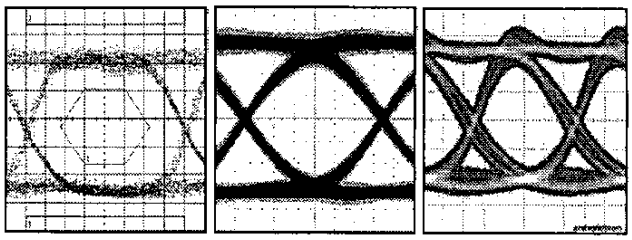


(C) 10Gbps eye diagram

Rate / Length	1Gbps			2.5Gbps			10Gbps		
	×16	×32	×64	×16	×32	×64	×16	×32	×64
1cm	P	P	P	P	P	P	F	P	P
10cm	F	F	P	F	F	P	F	F	F
20cm	F	F	F	F	F	F	F	F	F

(d) Acceptance table for 1, 2.5 and 10Gbps

Figure 6. Simulated eye diagram and acceptance table of 16, 32, 64bit wide CMOS interconnect with transmission line



(a) 1.25Gbps (b) 2.5Gbps (c) 10Gbps

Figure 7. Laser driver data from Maxim integrated product

((a) MAX3286, (b) MAX3865 and (c) MAX3932)

In the case of 1Gbps rate, 1cm long line permits all 16, 32 and 64bit wide channels and 10cm long line requires more than 64bit wide channel to achieve the data rate consequently increasing the circuit complexity. If there are terminations to reduce reflection loss, it is possible to improve performance in the acceptance table.

With regard to Figure 6(a), it can be said that for CMOS logic drivers unterminated interconnect should be substitued with a maximum of 10cm long terminated interconnect for 10Gbps throughput and a maximum of 20cm long lines at 1Gbps.

As mentioned in Section 2.2, transmission lines have serious signal losses as length and signal frequency increase. On the other hand, optical fiber channels have little loss even in the meter range. However, for optical interconnect on the board, optical waveguide needs to be considered as the channel against transmission lines on FR4 because optical fiber is incompatible with printed wiring boards due to its inflexible characteristic.

Optical waveguide technology using polymer has been developed with optical integrated interconnect. Advanced polymer technology facilitates lower loss optical waveguides. In particular, polymer type of Halogenated Acrylate[9] from AlliedSignal manufacture has less than 0.01dB/cm at 840 nm wave length, 0.03dB/cm at 1300nm wave length, 0.07dB/cm at 1550nm wavelength respectively. The data say that even 20cm long optical waveguide has as low channel power dissipation as 1.4dB optical loss at 1550nm wavelength. Additionally, laser drivers can handle 1.25, 2.5 and 10Gbps data capabilities with only a single channel yielding the eye digrams in Figure 7(a), (b) and (c)[10-12]. Therefore, it is reasonable that optical interconnect with driver is superior to electrical interconnect with CMOS dirver in tems of data transmission capability and channel power dissipation.

The remaining thing to discuss is circuit power consumption to drive the signal. For 10Gbps data rate, 64 channels of CMOS interface have only 6mW totally. On the other hand, 1.25, 2.5 and 10Gbps SiGe HBT laser drivers from Maxim Integrated Products have 156, 214 and 540mW respectively. The power consumption of these laser drivers is considerably higher than the electrical CMOS link. However, it is hard to generalize that power consumption of the CMOS driver sums up all the electrical interconnect power. As mentioned earlier, though a single terminated transmission line with vias cannot accomplish 10Gbps at 20cm, 4 parallel lines at 2.5Gbps yield 10Gbps aggregate throughput. Therefore, it can be argued that an optical interconnect should replace 4 terminated transmission line with drivers if it comsumes less power than the 4 electrical drivers.

5. Conclusions

Electrical and optical interconnect were compared to evaluate superiority of data rate, channel power dissipation and power consumption in driver as a function of line length. Transmission lines were simulated by HSPICE transient simulator and measured for two different physical conditions – with and without via – to obtain eye diagrams and S11 and S22 data. As a result of these, it is known that vias significantly affect the data transmission on 20 cm long lines at higher than 2.5Gbps. The simulation result on the model of the transmission line without via was matched to the result of the measurement to justify simulations with the CMOS inverter as driver. CMOS inverter driven interconnect was simulated at three different data rates for the same case as the transmission line and the data of the commercial SiGe HBT laser driver from Maxim Integrated Products was referred to compare with CMOS interconnect. Moreover, optical loss per interconnection length of the advanced optical waveguide material was supplied from reference[9]. Eye diagrams of commercial laser drivers are far more acceptable than those of CMOS interconnect. Furthermore, channel loss of optical waveguide is less than of electrical transmission lines apparently. For transmission lines with via, signal degradation at 10Gbps is overcome by using 4 parallel lines of same length at lower individual speed.

Therefore, with respect to power consumption, it can be said that an optical interconnect should replace electrical interconnect, provided it is 4 times less than power consumption of electrical interconnect.

Acknowledgments

The authors would like to thank the National Science Foundation Electronic Packaging Research Center and the State of Georgia Yamacraw Program for their support of this work.

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