

Heterogeneous Integration: From Substrate Technology to Active Packaging

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Abstract

Heterogeneous integration of dissimilar materials and devices is necessary for the continued advancement of electronic and optoelectronic systems. A range of processes has been developed in recent years that will enable system integration and advanced packaging. Herein, we outline our approaches towards heterogeneous integration.

Introduction

For decades, semiconductor research has focused on the goal of marrying dissimilar materials and devices for enhanced functionality, and reduced cost and size. Direct heteroepitaxy was the first approach to achieve this end, and continues as an active and viable approach for some systems. During the past decade, however, more emphasis has been placed on advanced processes that combine packaging and integration either at the wafer- or device-scale. While a range of challenges- from circuit design to bonding technology- must be addressed to enable heterogeneous integration; enhanced flexibility in device and materials design is also enabled. In active packaging (1), a term first used in 1994, a generalized approach to concurrent package and device design is articulated. Our use of the term focuses on the notion that the processing required for integration, such as substrate removal and bonding, is coupled with pre- and post-processing to enable new device configurations not achieved in standard growth, fabrication, and packaging sequence. For example, an active packaging approach enables collector-up HBTs, and inverted metal-semiconductor-metal devices with enhanced responsivity and alignment tolerance.

Our work focuses on the integration of a range of materials and devices, such as InP-based heterojunction devices, GaN metal-semiconductor-metal detectors, and InP-based detectors with Si CMOS electronics or on Si wafers. We are also investigating the use of bonded substrates for regrowth, such as strained channel (InGaAs) HEMTs on InGaAs substrates. These technologies are discussed below.

Integration of GaN with Silicon

The integration of GaN dissimilar materials, devices, and circuits offers opportunities that include advanced signal processing for integrated UV optical imaging arrays, and advanced packaging and automated tuning for high power devices. We have developed an approach for achieving device-quality GaN epitaxial material by Molecular Beam Epitaxy (MBE) concurrent with an integration process, by exploiting lithium gallate (LiGaO₂ or LGO) substrates. As described below, these substrates offer numerous advantages over the more commonly used sapphire and SiC. The integration process exploits a selective wet chemical etch and device- and circuit-scale bonding process.

Growth and Characteristics of GaN on Lithium Gallate

Independent of the ultimate desire for integration, the growth of GaN epitaxial layers on lithium gallate (LiGaO₂) offers distinct advantages toward achieving device quality material. Hexagonal GaN has a lattice mismatch of only -0.19% to the b-axis of LiGaO₂ (2). The dislocation density of GaN grown directly on LiGaO₂ is in the $10^7 - 10^8 \text{ cm}^{-2}$ (2,3), compared to $10^9 - 10^{11} \text{ cm}^{-2}$ for direct heteroepitaxial growth of GaN on sapphire. X-ray measurements indicate the high crystalline quality of GaN grown on LiGaO₂, producing a FWHM of 100-180 arcsec for a [00.4] reflection and 200-300 arcsec for a [10.5] reflection. The electronic and structural quality of AlGa_{0.4}N - GaN heterojunctions is inferred from the conductivity of two-dimensional electron gases (2DEG) induced at the interface. Figure 1 shows the temperature variable sheet charge and mobility of a 2DEG produced for a structure grown directly on LGO with a 0.8 μm GaN buffer followed by 35 nm of AlGa_{0.4}N. The measured mobility is $1365 \text{ cm}^2/\text{Vs}$ at 300K and $3700 \text{ cm}^2/\text{Vs}$ at 80K. The sheet charge was $7.7 \times 10^{12} \text{ cm}^{-2}$ (4).

MSM photodetectors have been grown on LGO for integration with Si. Unintentionally-doped GaN was grown on (001) LiGaO₂ using plasma-assisted radio-frequency molecular beam epitaxy. A five-period Al_{0.4}Ga_{0.6}N/GaN

superlattice was deposited as part of the nucleation layer, followed by a 1- μm thick unintentionally doped GaN epitaxial layer. Secondary ion mass spectroscopy

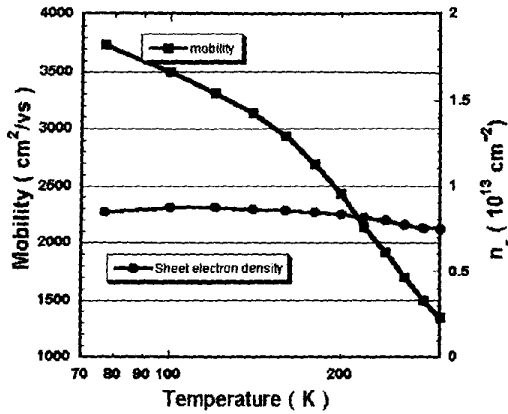


Figure 1. Two-dimensional gas mobility and sheet charge as a function of temperature for GaN on LGO

(SIMS) analysis indicates that the Al-containing layer impedes Li outdiffusion from the LiGaO₂ substrate.

Integration of GaN MSM Photodetectors with Si

Metal-semiconductor-metal (MSM) photodetectors were fabricated and tested before and after integration onto a SiO₂/Si wafer. Interdigitated-finger MSM devices were 47 μm long, with 2 μm finger width and 5 μm finger spacing, and an active detection area of 50x50 μm^2 . The devices were fabricated using standard photolithography to pattern photoresist, and subsequent metallization and liftoff processes to define metal Schottky metal contacts on the GaN. The Schottky contacts were 500Å Pt/2000Å Au. A cleaning step (hydrofluoric (HF) acid dip for 1 min and warm ammonium hydroxide (NH₄OH) for 15 min prior to the metallization) was used to remove the oxide on the GaN surface. This step lowered the MSM dark current by several orders of magnitude.

The integration process begins with the GaN/ LiGaO₂ sample. Mesas were patterned on the GaN surface using a photoresist mask and dry etching in a Plasma Therm inductively coupled plasma (ICP) system using Cl₂/BCl₃/Ar gases with flow rates of 8 sccm/12 sccm/5 sccm operating at 500 W plasma power, 90 V DC bias, and a substrate temperature of 15 °C. Under these conditions, the etch rate of GaN ranged from 2000 Å– 2400 Å per minute while the etch rate of the LiGaO₂ substrate was <10 Å/min. Thus, the mesa etch stops at the GaN/LiGaO₂ interface. The GaN mesas

were then coated in Apiezon W (black wax) to protect and support the GaN mesas during the subsequent LiGaO₂ substrate removal process.

The GaN epitaxial layer is impervious to most wet chemical acid solutions, thus, removal of the LiGaO₂ substrate from the GaN epitaxial layer is highly selective. The sample was kept in HF:H₂O (1:10) for approximately two hours to remove the substrate. The etch rate of LGO in HF:H₂O (1:10) is approximately 4.5 $\mu\text{m}/\text{min}$. The mesas embedded in the Apiezon W were bonded to the SiO₂- (9000Å) coated Si through contact bonding. The Apiezon W is then dissolved with trichloroethylene. Figure 2 shows an SEM image of a 170 μm x 90 μm mesa, 1 μm thick GaN thin film MSM photodetector bonded to a SiO₂/Si substrate (5).

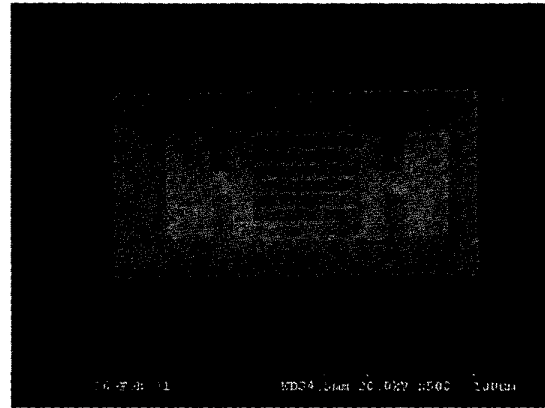


Figure 2. GaN MSM detector bonded onto a SiO₂/Si host substrate

It is important to note that this is a low temperature process, which indicates the successful implementation of this process for integration with Si CMOS circuitry. This process is to be contrasted with that of Wong, et al. They reported a process to separate GaN-based devices using a laser separation technique that decomposes the interface between the GaN and the sapphire substrate (6,7).

The dark current and photoresponse of the on-wafer and bonded GaN MSMs were compared. The characteristics and calibration of the measurement system are first described. A Keithley 617 electrometer was used to measure the current-voltage (I-V) characteristics of the device. A 250W tungsten lamp was used to determine the photoresponse. The light from the source was collimated and focused onto the detector using calcium fluoride lenses. A laser line filter at 308 nm (with a bandwidth of 10 nm) was used. The system exploited in this study was calibrated with an ultraviolet-enhanced calibrated Si photodetector and a Newport 1853 optical power meter. The measured dark currents and responsivities for the on-wafer MSMs and the thin film

MSMs after bonding to the SiO_2/Si host substrate are shown in Figures 3 and 4.

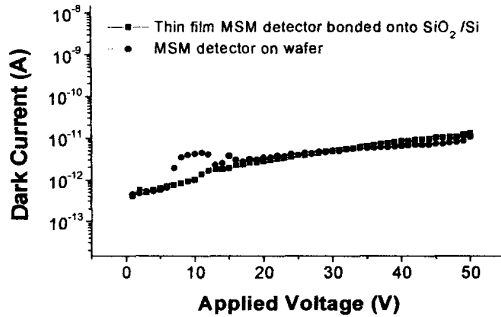


Figure 3. Dark Current versus voltage for on-wafer and bonded detector

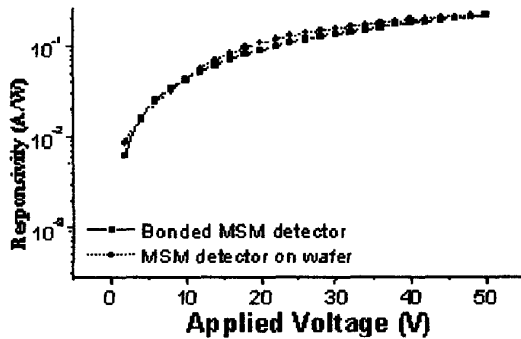


Figure 4. Responsivity for on-wafer and bonded detectors

The measured dark currents of 0.577 pA at 5V and 11.46 pA at 50V on-wafer degrade slightly to 0.627 pA at 5V and 13.36 pA at 50V after bonding, as shown in Figure 3. This degradation is within the measurement error tolerance. The 10 V low bias dark current of 1.01 pA of the thin film GaN MSM detector is comparable to the best reported low bias dark current of 0.8 pA at 10 V for on-wafer MSMs with similar area and finger spacing, but with a 4 μm thick GaN layer (6). In addition, this device exhibits no reverse bias breakdown up to 100 V. We have made recent advances on the performance of on-wafer devices and have achieved dark currents of 3.7 pA at 100V.

The measured responsivity values of the GaN MSM, with no AR coating, of 0.107 A/W at 20V and 0.222 A/W at 50V reverse bias conditions before bonding, decreases to 0.089 A/W and 0.218 A/W, respectively, at the same bias condition after bonding, as shown in Figure 4. These results are also competitive with the best reported responsivity results (8).

The use of MSM detectors as a vehicle for integration technology exemplifies the active packaging approach. Concurrent device processing and integration enables enhanced responsivity by introducing the finger contacts at the device - substrate interface, thus increasing the detector area usually blocked by the surface metal fingers (9). Ultimately, UV and IR detectors will be vertically stacked to build compact and high performance integrated systems.

Integration of InP-Based Technology

The process for the integration of InP-based materials, such as AlInAs-GaInAs HBTs and GaInAs epitaxial films for alloy substrates, is achieved by selective etching and wafer-scale bonding via direct bonding or the use of an oxide (borosilicate glass) interlayer for either subsequent processing or re-growth on a composite substrate. In this case, the bonding to GaAs substrates utilized a low temperature bonding procedure in which a plasma activation step along with DI water rinsing was used to create a room temperature bond. The bonding procedure requires no added pressure hence minimizing device degradation. The room temperature bond is robust enough to withstand mechanical operations such as lapping and etching.

A full 2"-wafer low-temperature bond and transfer has been applied to GaInAs-AlInAs heterojunction diodes (designed to mimic a typical emitter-base junction of an HBT) to integrate

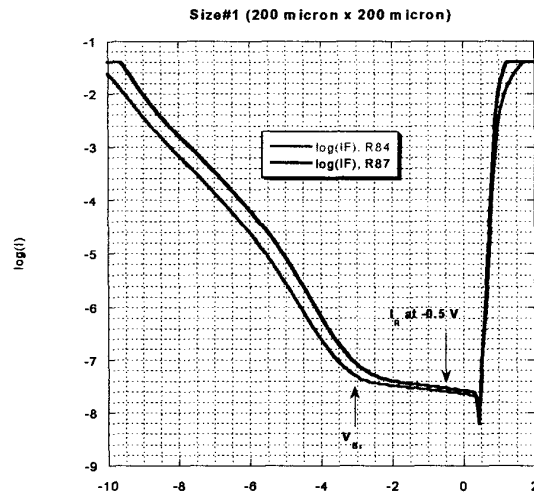


Figure 5. I-V Characteristics of on-wafer (R84) and bonded (R87) diodes

devices onto a GaAs platform. Ultimately, other substrates, such as sapphire will be used for the package. Heterojunction diodes show only small changes in relevant properties – breakdown and turn-on voltages, leakage currents, and

ideality factors. Figure 5 shows a comparison of I-V characteristics (leakage currents) of the as-grown structure (R84) and the bonded structure (R87).

Regrowth on Bonded Substrates

Bonding and substrate removal technologies also enable the growth of devices onto substrates that cannot be produced in bulk form. We are currently investigating the growth of AlInAs-GaInAs HEMT structures on InGaAs substrates of a range of compositions. Figure 6 shows an AFM micrograph of an InGaAs substrate bonded with borosilicate glass onto GaAs. Regrowth of HEMT structures on the InGaAs substrate shows the promise of this technique. Electron mobilities of $>7000 \text{ cm}^2/\text{Vs}$ have been demonstrated compared to $10,000 \text{ cm}^2/\text{Vs}$ achieved for control samples grown on InP substrates (10). Ultimately, the growth of HEMTs on alloy substrates may enable the achievement of compositions and pseudomorphic structures not currently accessible today.

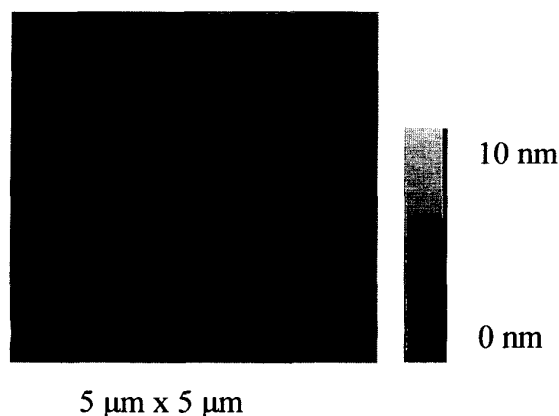


Figure 6. AFM Image of GaInAs (rms roughness = 0.21 nm) film bonded to GaAs

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