Highly Alignment Tolerant InGaAs Inverted MSM Photodetector Heterogeneously Integrated on a Differential Si CMOS Receiver Operating at 1 Gbps

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Abstract

The increasing demand for high bandwidth, low latency I/O in gigascale systems is challenging current packaging technology. Optoelectronic I/O offers needed performance, but presents new challenges in mixed signal (digital, analog, optical, RF) design and test. In addition, the integration of OE interconnect must be suitable for high volume, low cost manufacturing of digital systems. This paper explores the heterogeneous integration of very large area, highly alignment tolerant photodetectors onto Si CMOS differential analog receiver circuits to realize noise-tolerant receiver interfaces for high-density interconnection electrical substrates with integrated optical links as well as for fiber optic links. The realization of an optically interconnected microprocessor that employs such a photodetector will also be discussed.

Introduction

Digital noise is a critical factor in the design of the integration of optoelectronic interconnections into digital electronic systems. When complex VLSI circuitry such as a microprocessor is integrated onto the same integrated circuit as a sensitive optoelectronic receiver amplifier, the 100 – 500 mV of noise created by typical microprocessors generates high levels of signal noise in the receiver input. This noise can be alleviated through the use of differential receiver circuits, which utilize more space and more power, but are capable of operating in noisy digital environments. In this paper, we will report on the design, heterogeneous integration, and test of a 0.35 μm digital Si CMOS differential receiver optoelectronic integrated circuit (OEIC) that was designed for 1 Gbps operation and for integration with complex, noisy Si CMOS logic circuitry.

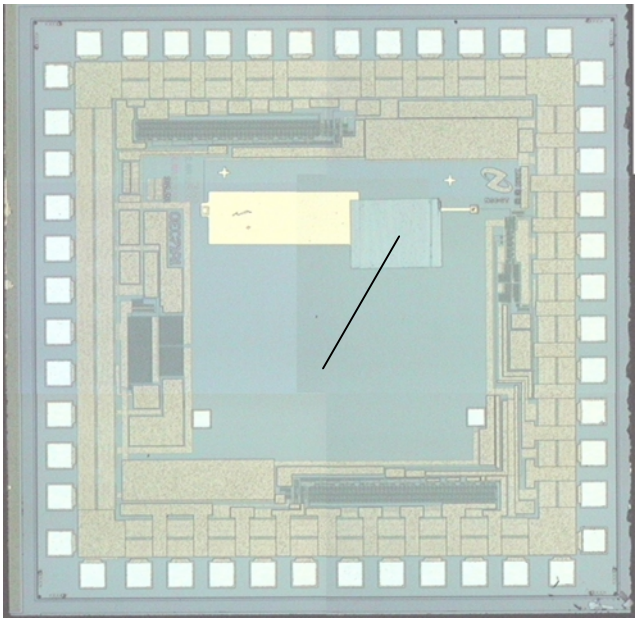
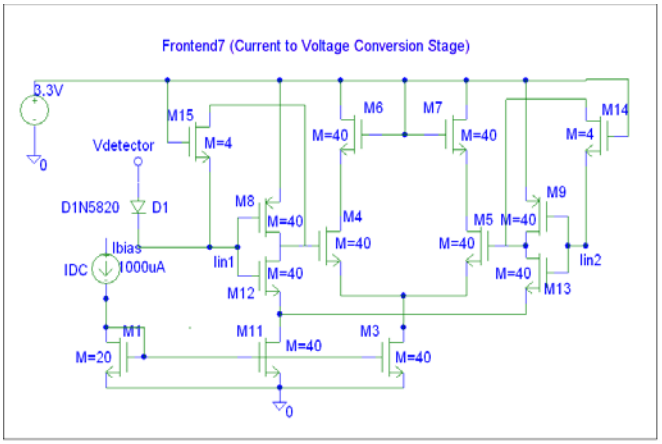


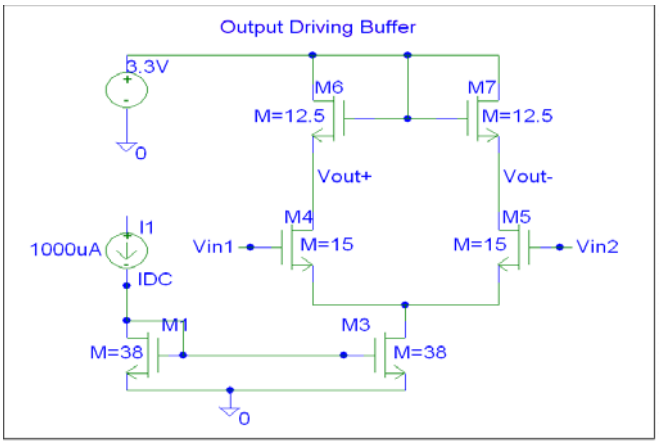
Figure 1: 250 x 250 μm^2 InGaAs/InP I-MSM integrated onto 0.25 μm differential Si CMOS receiver.

The 1 Gbps differential receiver was integrated with a large-area thin film InGaAs/InP inverted (I-) metal-semiconductor-metal (MSM) photodetector to realize an OEIC sensitive to wavelengths of 1.3 and 1.55 μm. This integrated receiver is shown in Figure 1. The I-MSMs exhibit responsivities comparable to PIN photodiodes while maintaining lower capacitances per unit area than PINs, which enable much larger detecting areas for similar device capacitances. This paper reports the hybrid integration of a 250 x 250 μm^2 InGaAs I-MSM onto the fully differential Si CMOS receiver. This heterogeneous integration technique enables independently optimized OE active components to be utilized in conjunction with Si CMOS circuits for low cost applications. The OEIC receiver operated at 1 Gbps with a bit-error-rate (BER) of 6.8 x 10^{-10} and demonstrated a high level of alignment tolerance. The alignment tolerance of the OEIC and the theoretical alignment tolerance of OEICs integrated with PINs, MSMs, and I-MSMs at SONET OC-48 (2.4 Gbps) will be presented in this paper.

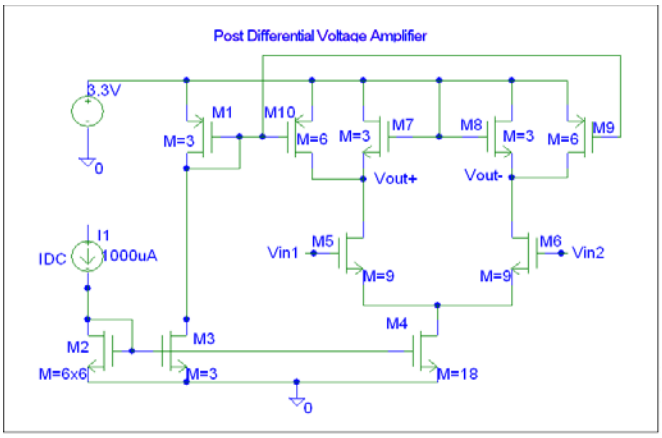
This receiver design has also been integrated into 0.8 μm digital Si CMOS on a single chip with a microprocessor. A single ended and a differential receiver were both integrated with the microprocessor onto a single Si CMOS integrated circuit, however, the microprocessor noise levels precluded the use of the single ended receiver when it was integrated. The differential receiver was integrated with an I-MSM, and operated at 100 Mbps in the noisy digital environment with a BER of 10^{-9}. The single instruction multiple data (SIMD) microprocessor performed simple operations based upon the optical input data. Measured results from this optically interconnected single chip microprocessor will be presented in this paper.



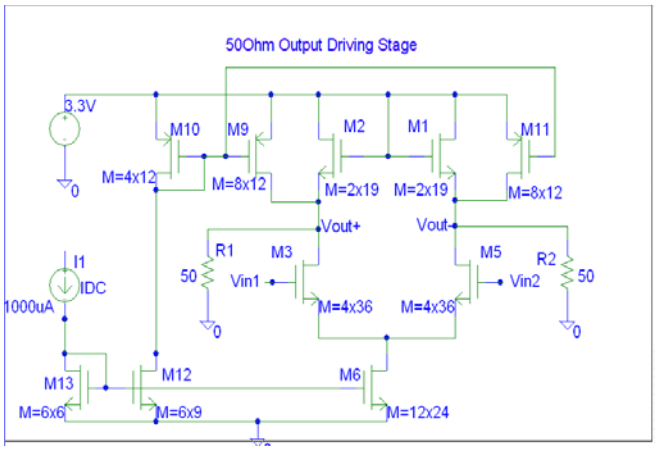
(a) Transresistance amplifier



(c) Buffer stage



(b) Voltage-mode amplifier



(d) Output driver stage

Figure 2: Differential receiver circuit schematics.

Differential Receiver Design

Noise immunity is a critical issue for highly sensitive analog circuitry operating in mixed signal systems. Many optical receivers use a single-ended analog preamplifier, which is highly susceptible to power supply fluctuations and external noise. In particular, analog receivers operating in digital environments are subject to fluctations in power rail voltages and noise pickup through the substrate. For these types of mixed signal applications, a differential or balanced analog topology provides improved noise immunity as well as stable biases for optoelectronic devices within the system.

The integrated receiver shown in Figure 1 was designed in 0.35 µm CMOS and fabricated at the National Semiconductor Corporation foundry. Schematics for the differential receiver are shown in Figure 2. A low noise differential current input transresistance feedback amplifier (Figure 2a) serves as the front-end. The geometry of this stage is carefully designed to ensure that noise is picked up equally on each input. This allows the differential nature of the amplifier to remove the noise at the output. The latter stages of the multi-stage amplifier are voltage-mode amplifiers (Figure 2b) which consume less power at a given bandwidth than the transresistance amplifiers [1]. A differential output stage (Figure 2d) after the post amplifier was used to drive the 50 Ω output termination and enable output swing voltages of more than 200 mV peak to peak at each output (more than 400 mV differential). A buffer stage (Figure 2c) was used between the post amplifier and the output stage to improve performance.

Photodetector Design, Fabrication, and Integration

For alignment tolerant OE receivers, large-area photodetectors are ideal, but detector capacitance increases with increasing detector area. Since the bandwidth of a photodetector is limited by either the RC time constant of the device or the transit times of photogenerated carriers within the device, increased capacitance (and hence, a large detecting area for alignment tolerance) can impose bandwidth limitations on an integrated receiver. MSM photodetectors have much lower capacitances per unit area than typical PIN photodiodes, enabling much larger detecting areas for a given input capacitance to a receiver circuit. However, the interdigitated electrode structure of the MSM, shown in Figure 3, shadow portions of the detector, resulting in responsivities that are significantly lower than PINs.

Enhancing the responsivity of MSM photodetectors has been the focus of a great deal of research. In [2], back-illumination of an MSM was used to demonstrate a record responsivity of 0.96 A/W; however, this integration scheme complicates packaging. Transparent indium-tin-oxide (ITO)

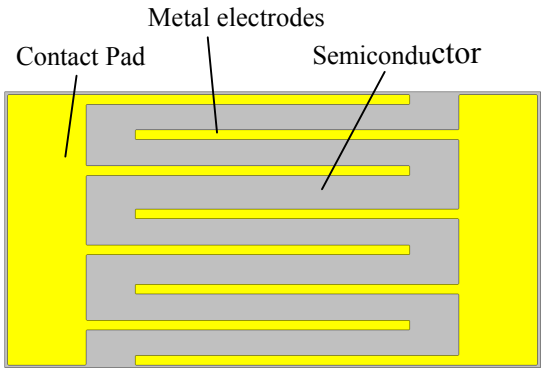


Figure 3: Conventional MSM structure.

electrodes were reported in [3]. These devices had responsivities of 0.76 A/W, but the high resistivity of the electrodes degraded the bandwidth of the device. Sub-micron electrode widths with micron spacings have been reported in [4]. Although these devices exhibited responsivities of 0.75 A/W, the sub-micron features complicate fabrication. The I-MSMs reported in this paper represent another approach to enhancing MSM responsivity. Essentially the devices are integrated onto the receiver circuits as thin film devices (the growth substrate has been removed) with the electrodes and contact pads on the bottom of the device. In this way, the shadowing effect of the electrodes is eliminated and the low capacitance per unit area of the detector is maintained. I-MSMs do exhibit a slightly slower transient response than conventional (C-) MSMs [5], but the improved responsivity and large area of the device provide a high level of alignment tolerance that is ideal for low cost applications. Typical responsivity for the devices reported here was 0.5 A/W, although a responsivity 0.7 A/W has been reported for an I-MSM with a 1 μm thick absorbing region [5]. For a specified data rate, the electrode geometry, layer structure, and area of the I-MSM can be optimized for a particular application. The results reported herein pertain to OE receivers designed specifically to optimize alignment tolerance.

The I-MSM photodetectors used for this project were grown by molecular-beam-epitaxy (MBE) on semi-insulating InP. The grown layers consisted of the following structure: 2000 Å InGaAs stop etch layer, 400 Å InAlAs cap layer, 500 Å graded layer, 7400 Å InGaAs absorbing layer, 500 Å graded layer, and 400 Å InAlAs cap layer. All layers were nominally undoped and grown lattice matched to the InP substrate. The InAlAs cap layers were used to enhance the Schottky barrier height of the MSM photodetector and reduce surface recombination velocity. The graded layers reduce any energy band discontinuities, which can trap photogenerated carriers and degrade the bandwidth of the detector. The InGaAs absorbing region made these detectors suitable for detecting wavelengths of 1.3 μm and 1.55 μm. Ti/Au electrodes were deposited as the Schottky contacts with thicknesses of 250 Å and 2250Å, respectively.

The detectors were fabricated with 250 x 250 μm^2 detecting areas. The electrode fingers were 2 μm wide with 5 μm spacings to reduce the capacitance of this large-area

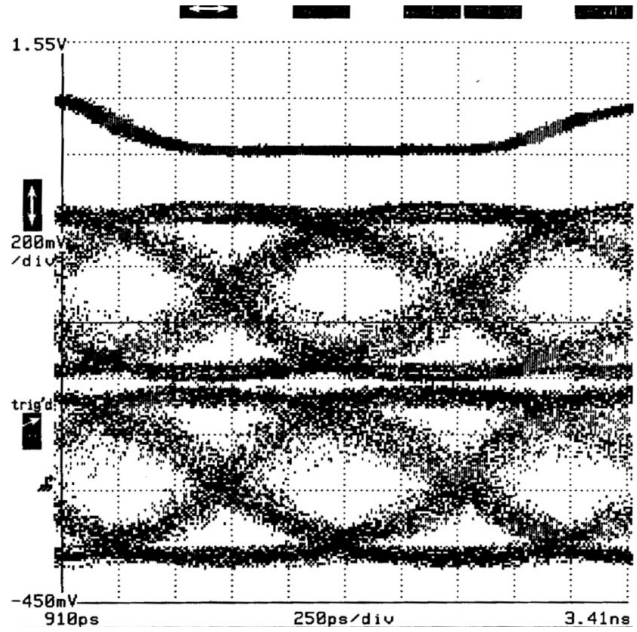


Figure 4: Eye diagram of the differential receiver outputs at 1 Gbps.

device while still achieving the desired data rate of 1 Gbps. The calculated capacitance of the I-MSMs was 0.43 pF.

The device mesas were defined using standard photolithography and wet-etched down to the stop etch layer using a citric acid/H_2O_2 (10:1) solution. The mesas were then embedded in a handling layer of Apeizion W wax with the substrate exposed. The substrate and stop etch layer were removed using HCl and a second citric acid/H_2O_2 (1:1) solution, respectively. The exposed bottoms of the mesas were then bonded to a transparent transfer diaphragm and the handling layer was removed. Individual mesas were then transferred from the diaphragm and metal-metal bonded to contact pads on the receiver circuit. Polyimide 2611 was spun onto the integrated circuits and cured at 200 °C for two hours. After curing, the polyimide was removed in an O_2 reactive-ion-etch (RIE) process. As a final step, the integrated circuit was wirebonded to a printed circuit board for testing.

Experimental Results

The bit-error-rate (BER) performance of the integrated receiver was tested using a distributed feedback (DFB) laser pigtailed to a single-mode fiber. The laser was operated CW and emitted a beam with a wavelength of 1550 nm. The single-mode fiber was coupled via FC/FC connectors to a Mach-Zehnder $LiNbO_3$ modulator being driven by the BER transmitter. The output of the modulator was coupled with FC connectors to a cleaved single-mode fiber. The cleaved end of the fiber was aligned to the integrated receiver using a fiber chuck and an XYZ translation stage. The detector was biased with a Keithley SMU, which also measured average photocurrent. This photocurrent could be used in conjunction with the detector responsivity (0.5 A/W) to calculate average power coupled to the detector from the fiber. The receiver demonstrated a BER of 6.8×10^{-10} at a data rate of 1 Gbps with an average optical input power of –10 dBm. The eye diagram at this data rate is shown in Figure 4.

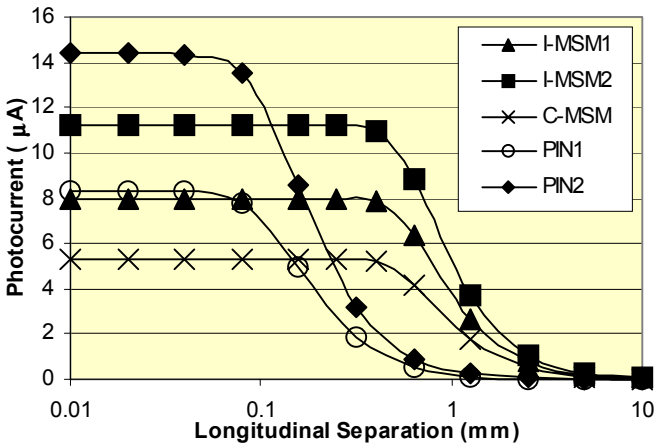


Figure 5: Theoretical longitudinal alignment tolerance of various photodetectors for a 2.4 Gbps receiver.

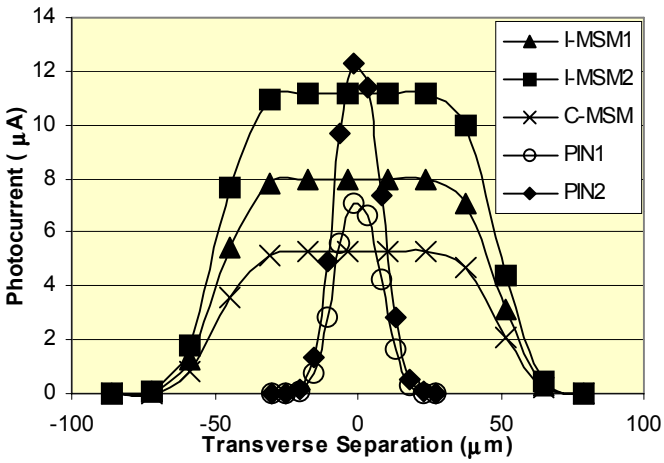


Figure 6: Theoretical transverse alignment tolerance of various photodetectors for a 2.4 Gbps receiver (longitudinal separation = 100 µm).

The alignment tolerance of the integrated receiver was measured at 650 Mbps. We believe that these are the fastest reported alignment tolerance measurements reported to date. Power coupled from the fiber to the detector was measured as a function of two types of misalignment: longitudinal and transverse. Longitudinal separations refer to the distance between the edge of the cleaved fiber and the surface of the photodetector. Transverse separation is defined as the amount of off-axis separation between the center of the fiber and center of the detector for a given longitudinal separation. Both theory and experimental measurements show that the normalized power coupled from the fiber to the detector have a 3 dB decrease in coupled power at a longitudinal separation of ~2.9 mm. There is a slight discrepancy between theory and experiment, which is most likely due to oversimplifications in the coupling model, which will be discussed below. Next, the power coupled from the fiber to the detector as a function of transverse separation for a longitudinal separation of 500 µm was measured and theoretically calculated. Again, theory and experiment are in agreement, showing a 3 dB decrease in coupled power at a transverse separation of ±125 µm.

Theoretical Alignment Tolerance Comparison

Theoretical longitudinal and transverse alignment tolerance were calculated using a simple coupling efficiency model. In this model, the intensity function of the beam emitted from the cleaved end of the single mode fiber was approximated as a circular Gaussian beam. Although an oversimplification, this approximation greatly reduces computation time. To calculate longitudinal alignment tolerance, the intensity function was integrated over the area of the detector as a function of longitudinal separation. To calculate transverse alignment tolerance, the limits of integration along one of the transverse axes were adjusted to account for transverse misalignments between the fiber and detector.

Using this simple coupling efficiency model, the alignment tolerance of photoreceivers integrated with PINs, C-MSMs, and I-MSMs were compared for SONET OC-48 (2.4 Gbps) short haul links. A minimum output power of –18 dBm was assumed. The following photodetectors were compared: an I-MSM similar to the one integrated on the receiver shown in Figure 1 (I-MSM1), a high responsivity I-MSM with a slightly different layer structure reported in [5] (I-MSM2), a C-MSM identical in structure and electrode geometry to I-MSM1, a standard PIN photodiode reported in [6] (PIN1), and a high responsivity PIN photodiode reported in [7] (PIN2). The MSMs in this comparison were reduced in shape and area from rectangular 250 x 250 μm^2 as described above, to circular with a diameter of 100 µm. This reduction in device area lowered the theoretical capacitances of the detectors from 0.43 pF to 55 fF, which is a typical input capacitance value for a 2.4 Gbps receiver. The PINs were chosen from the literature because their capacitances of 130 fF (PIN1) and 230 fF (PIN2) were comparable to those of the MSMs. Both PINs had 20 µm diameters. PIN1 had a responsivity of 0.52 A/W. PIN2 had used a bottom gold reflector to improve responsivity to 0.9 A/W. I-MSM2 and PIN2 are included in this comparison as best case examples for each type of detector.

Figure 5 shows photogenerated current as a function of longitudinal separation for each detector. Under optimal alignment I-MSM1 and PIN1 generate similar amounts of photocurrent, but the I-MSM provides a much greater degree of longitudinal alignment tolerance. In the case of the high responsivity devices, PIN2 will provide a greater amount of photocurrent than I-MSM2 under optimal alignment; however, the large-area I-MSM again provides much greater alignment tolerance. The PINs show a 3 dB decrease in photocurrent at ~200 µm of longitudinal separation. The I-MSMs does not show such a decrease until 900 µm of longitudinal separation. The C-MSM provides alignment tolerance similar to that of the I-MSMs; however, the overall C-MSM photocurrent is significantly less than either of the I-MSMs due to electrode shadowing.

The comparison of transverse alignment tolerance is shown in Figure 6. These curves were computed assuming a longitudinal separation of 100 μm. Under optimal alignment the PINs and I-MSMs will generate similar amounts of photocurrent. However, the I-MSMs are much more alignment tolerant with 3 dB decreases in photocurrent occuring at ±50 μm of transverse separation. The PIN photocurrents fall of by fifty percent at misalignments of ±10 μm.

Optically Interconnected Microprocessor

As a demonstration of the immunity of the differential receiver described above to digital noise, the receiver was fabricated in 0.8 μm Si CMOS at the MOSIS foundry on the same chip with a SIMD microprocessor. A thin film, large-area (200 x 200 μm^2) I-MSM with the same layer structure as discussed previously was heterogeneously integrated onto the circuit. The I-MSM in this case had 2 μm electrode widths and 3 μm spacings. The OEIC was wirebonded into a 110 pin PGA (pin grid array) package for testing. The integrated receiver/SIMD circuit is a portion of an on-focal plane imaging system. The microprocessor inputs a data stream from an imaging array that is preprocessed using sigma delta analog to digital converters which is subsequently passed to the receiver using an optical link [8]. This processor node is part of a processor array called SIMPil [9].

A 1.3 μm Fabry-Perot laser pigtailed to a single-mode fiber was used as the optical source in the experiment. The laser was directly modulated by a digtial waveform generator. The microprocessor performed a simple add operation on the incoming data, and the add operation increment was defined by the optical digital data stream. Sample numbers were programmed into the waveform generator for the various "add x" operations carried out by the microprocessor. The integrated receiver operated at 100 Mbps with a BER of 10^{-9} and a sensitivity of –20 dBm. The eye-diagram of the differential receiver outputs is shown in Figure 7.

Conclusions

With the increasingly pervasive use of OE interfaces in mixed signal systems, noise immunity of the analog receiver circuitry is a critical factor in the performance of the link. Equally important for development of low cost OE links are manufacturing yield issues. We report a differential Si CMOS receiver integrated with a large-area, thin film InGaAs/InP I-MSM operating at 1 Gbps. This receiver was designed to improve both manufacturing yields through alignment tolerance as well as the immunity of the integrated receiver to power supply fluctuations and external noise. Alignment tolerance measurements for the integrated circuit were reported. The alignment tolerance of I-MSMs were theoretically compared to PINs and C-MSMs for high speed, 2.4 Gbps links. The low capacitance-per-unit-area of the I-MSMs coupled with their high responsivities resulted in alignment tolerances far superior to the other types of photodetectors. The differential receiver was also fabricated on the same chip as a digital microprocessor. The differential topology successfully reduced the noise sensitivity of the analog receiver in order to achieve a BER of 10^{-9} at 100 Mbps.

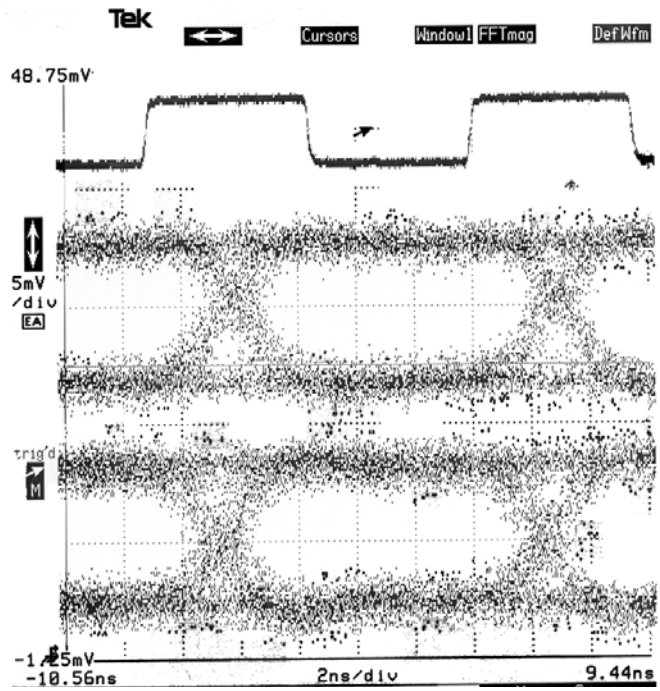


Figure 7: Eye diagram of differential receiver outputs at 100 Mbps on same chip as functioning microprocessor.

Acknowledgments

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