A Scaleable CMOS Current-Mode Preamplifier Design for an Optical Receiver

Myunghee Lee, Olivier Vendier, Martin A. Brooke, and Nan Marie Jokerst
School of Electrical and Computer Engineering
Microelectronics Research Center
Georgia Institute of Technology
Atlanta, GA 30332
Tel) 404-853-9920, Fax) 404-894-0222

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Abstract

We have designed a process-insensitive preamplifier for an optical receiver, fabricated it in several different minimum feature sizes of standard digital CMOS, and demonstrated design scaleability of this analog integrated circuit design. The same amplifier was fabricated in a 1.2 μm and two different 0.8 μm processes through the MOSIS foundry [1]. The amplifier uses a multi-stage, low-gain-per-stage approach. It has a total of 5 identical cascaded stages. Each stage is essentially a current mirror with a current gain of 3. Three of these preamplifiers have been integrated with a GaAs Metal-Semiconductor-Metal (MSM) photodetector and one with an InGaAs MSM detector by using a thin-film epilayer device separation and bonding technology [2]. This quasi-monolithic front-end of an optical receiver virtually eliminates the parasitics between the photodetector and the silicon CMOS preamplifier. We have demonstrated speed and power dissipation improvement as the minimum feature size of the transistors shrink.

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1. Introduction.

There is a demand for wide bandwidth in the data [3-4] and tele communication areas as the information superhighway gains speed. At the same time, there is a trend towards monolithic integration of optoelectronic and electronic components, called OEICs (OptoElectronic Integrated Circuits), to achieve improved functionality and performance, and reduce cost. Most OEICs are designed and fabricated by using GaAs MESFETs [5-13] or Si Bipolar transistors [14] to achieve giga-bit data rate ranges.

To achieve giga-bit data rates with MOSFET transistors, specialized fineline NMOS technology [15] was developed. Several researchers have presented CMOS amplifiers [16-21] for an optical receiver with external P-i-N photodetectors. Most of these amplifiers depend on analog CMOS process technologies [16-19]. Their bandwidth is still limited to about a couple of hundred mega-bits-per-second data rate. To increase bandwidth capability, the design method using multi-channels was introduced [18]. Recently, there have been attempts to use standard digital CMOS technologies [20-21] since there are more demands to have analog and digital circuits on the same chip. Design topologies of these amplifiers are either feedback-type transimpedance or high-impedance-type approaches [4].

Analog integrated circuits using digital silicon CMOS technologies are very attractive since this enables small size, highly integrated analog/digital circuits. Standard digital CMOS IC fabrication processes are well developed and, therefore, cost less than comparable specialized analog IC processes. As the minimum channel length of CMOS transistors moves to a deep submicron level, it is more feasible to implement an amplifier with a wider bandwidth in digital CMOS technology.

However, there are severe disadvantages to using digital CMOS processes for analog integrated circuits. Major limitations include the process sensitivity of active devices and lack of practical passive devices such as resistors and capacitors [22]. These factors decrease the performance of standard analog integrated circuit design techniques. It is also widely known that scaling of analog circuits into the submicron range leads to unacceptable performance for many analog IC designs [23].

To overcome the disadvantages of standard digital CMOS processes, we have designed a preamplifier for an optical receiver which is tolerant to process parameter variations. Current-mode design topology [29-31] was also used rather than a voltage-mode approach. Preamplifiers with exactly the same circuit layout were fabricated using 1.2 μm and two different 0.8 μm minimum feature size processes through the MOSIS foundry to observe the performance scaleability. This silicon circuit was then integrated with a thin-film compound semiconductor detector by using separation and direct bonding [2]. This integration not only provides a highly integrated circuit with

Place Figure 1.

small size, but greatly reduces the packaging parasitics between the photodetector and the silicon circuits, in contrast to hybrid packaging using wire bonding. It enables evaluation of the amplifier performance without unwanted parasitics and helps in predicting general scaleability rules for CMOS analog ICs from these amplifiers.

2. The amplifier circuit.

The preamplifier is designed to meet the specifications of the industry optical communication protocols FDDI and SONET STS-3 [24]. The target bandwidth of the amplifier is greater than 155 Mbps or 100 MHz. In order to obtain such an operating speed, design optimization yields a multi-stage, low-gain-per-stage design shown in Figure 1. Assuming a certain fixed total gain and power dissipation product, an open-loop gain approach provides a better upper -3 dB frequency than a feedback circuit. As the number of stages increases, the required gain and power dissipation available per stage decreases. However, the bandwidth per stage increases, resulting in much higher overall amplifier bandwidth. On the other hand, if too many stages are cascaded, the bandwidth decreases due to the accumulated effect of the parasitic capacitance associated with each amplifier stage. From the analysis shown in Figure 2, an amplifier with about five stages is the optimal design for this application.

The final amplifier design consists of 5 identical stages in cascade, shown in Figure 3, and each stage has a current gain of 3, as shown in Figure 4. The number adjacent to each transistor represents the relative size of the transistor gate width. The real channel width is obtained by multiplying the number by λ, which is the scaleable design-rule parameter. The gate length of every transistor is the minimum feature size of each process. The overall circuit also contains offset control and bias circuitry.

Place Figure 2,

Place Figure 3,

Place Figure 4.

This amplifier has several important features. First, the preamplifier design relies on the matching of the geometric device size rather than on process parameter matching to alleviate the poor device parameter mismatch associated with digital CMOS processes. The amplifier is essentially a current-mode amplifier and the current gain of each stage, A_I, is controlled by the gate width ratio of two transistors forming a current mirror, that is,

$$A_I = \frac{W_{N4a}}{W_{N1}}, \qquad \text{Eq. (1)}$$

where W_{N4a} and W_{N1} are the gate widths of transistors *N4a* and *N1*, respectively, from Figure 4 (b). The gate length of all transistors is the minimum feature size of each process, to maximize the speed.

Second, the input transistor of the current mirror is also used to set the input impedance. The input resistance of the amplifier is approximately

$$R_{IN} = \frac{1}{g_{mN1}} = \left(2\sqrt{K_P \cdot \left(\frac{W_{N1}}{L_{N1}} \right) \cdot I_{DS}} \right)^{-1} \qquad \text{Eq. (2)}$$

where g_{mN1} is the transconductance of transistor N_1. Since g_{mN1} is proportional to the drain-source current, I_{DS}, and the geometric transistor size, *(W/L)*, of N_1, the input resistance can be controlled by adjusting these two parameters. This results in the flexibility to control the input impedance of the amplifier. The other advantage is that the current input signal from the photodetector is fed directly into the amplifier input node without using a resistor, which is difficult to realize in a scaleable CMOS design.

Third, the input buffer, N_2, is used to reduce the input capacitance. Without the buffer, the input gate capacitance would be

$$C_{TOTAL} = 4 \cdot C_{gs} + 2 \cdot C_{db}, \qquad \text{Eq. (3)}$$

where C_{gs} is the gate capacitance and C_{db} the drain-body capacitance of a transistor. Using the buffer, C_{TOTAL} can be reduced to

$$C_{TOTAL} = C_{gs} + 2 \cdot C_{db}. \qquad \text{Eq. (4)}$$

Therefore, the bandwidth of each stage is

$$BW = \frac{g_m}{C_{gs} + 8 \cdot C_{db}}. \qquad \text{Eq. (5)}$$

Finally, a cascode at the output stage increases the output impedance so that most of the signal current is delivered into the following stage. It also helps to reduce the channel length modulation effect. This configuration yields an output resistance of

$$R_{OUT} = \frac{g_m \cdot r_{ds}}{2 \cdot g_{ds}}, \qquad \text{Eq. (6)}$$

where r_{ds} and g_{ds} are the output resistance and conductance, respectively.

The overall transimpedance gain for this 5-stage amplifier is obtained from

$$A_R = A_I^{\,5} \times R_L, \qquad \text{Eq. (7)}$$

where R_L is the output load resistance and 50 Ω was used for the measurement. Since A_I is about 3, A_R is more than 12 KΩ (=243x 50 Ω).

Another important parameter in the design of this optical receiver is the sensitivity, which is determined by the input noise level of the preamplifier. The industry communication protocols specify the sensitivity of an optical receiver front-end [24]. The sensitivity of an amplifier is closely related to the power dissipation. Better sensitivity usually requires more

power dissipation by the front-end amplifier of the receiver. Therefore, in our design approach, the amplifier power dissipation was set to meet the sensitivity requirement, or the power dissipation of the amplifier was minimized as long as the amplifier exceeded the sensitivity limit.

The input noise level was analyzed to estimate the sensitivity of the amplifier. There are two major factors which affect the input noise. The first is the absolute noise level at the first input stage of the preamplifier. The second is the effect of the following stage when the amplifier has cascaded stages and each stage has low gain.

The input noise at the receiver amplifier consist of four terms [3,4],

$$\left\langle i_{TOTAL}{}^2 \right\rangle = 2qI_{da}BI_2 + 2qI_{gate}BI_2 + \frac{8kT}{3\left(\frac{1}{g_m}\right)}BI_2 + \frac{8kT}{3g_m}(2\pi C_T)^2 I_3 B^3, \qquad \text{Eq. (8)}$$

where I_{da} is the dark current of the photodetector, I_{gate} the leakage current of the input transistor, g_m the transconductance of the input transistor, C_T the total input capacitance, q the electron charge, B the operating bandwidth, k the Boltzmann constant, T the absolute temperature, and I_2 and I_3 weighting functions which are dependent only on the input optical pulse shape to the receiver and equalized output pulse shape. For non-return-to-zero coding, I_2 = 0.55 and I_3 = 0.085 [3].

In Eq. (8), the first term is the noise caused by dark current in the photodetector. The second term is the shunt noise caused by the input gate leakage. The third is the series noise term due to the channel thermal noise of N_1. Higher input resistance, $1/g_m$, helps reduce the input noise. However, the maximum input resistance will be limited by the bandwidth requirement. This will be the dominant term at moderate bandwidth. The fourth term is strongly dependent on the bandwidth. Therefore, at higher bandwidths, this term will be dominant. For this reason and due to the bandwidth

requirement, it is important to have a photodetector with a low capacitance. Using a buffer, N_2, shown in Figure 4, also helps reduce capacitance due to the current mirror. The first two terms are usually negligible compared to the last two terms.

3. Simulation

From Eq. (2), the input resistance of the amplifier is $1/g_m$, which is determined by the transistor size and bias current, I_{DS}. Table 1 shows the key SPICE parameters of each process. The transistors of the amplifier use an uniform geometric gate size with a 2 to 1 ratio of width/length except the output stage, which is 3 times larger in gate width. Therefore, I_{DS} is the only parameter to vary the input resistance. I_{DS} is controlled by the bias current, I_{source}. Figure 5 shows the simulated input resistance of each process. The bias current for the amplifier is between 10 μA and 100 μA, and the input resistance ranges from 10 KΩ to 3 KΩ. Assuming that the total input capacitance is around 1 pF, then the required input resistance should be less than 10 kΩ to achieve a 100 MHz overall bandwidth.

Another aspect of the amplifier bias currents, I_{source} and I_{sink}, is the operating condition of the impedance of the output stage and the following input stage. We have estimated the channel length modulation effects from HSPICE simulation using a BSIM Level 13 model [25]. The input and output resistance values are controlled by these bias currents. Figure 6 illustrates the analytical resistance values for 0.8 μm feature size technology as the bias current changes. As the bias current increases, the input resistance decreases, which increases the bandwidth. However, increased bias current also decreases the output impedance. From Figure 6, the slope of the output

Place Table 1.

Place Figure 5, 6, and 7.

resistance is much steeper than that of the input resistance. As a result, the amplifier suffers from overall gain loss at higher bias currents. Figure 7 shows the gain attenuation as the bias current, I_{source}, increases. At around 200 μA, the attenuation is 0.9.

The bandwidth of each amplifier stage, ω_1, is set by Eq. 5. The overall -3 dB bandwidth of the *n*-stage amplifier, ω_n, is

$$\omega_n = \omega_1 \sqrt{2^{\frac{1}{n}} - 1}, \qquad \text{Eq. (9)}$$

where *n* is the number of identical gain stages forming the cascade. Since the amplifier has 5 identical stages, ω_n is about 61 % less than ω_1.

4. Layout

In the layout of the circuit, splitting the power supply rails helps to reduce parasitic feedback, which usually causes oscillation. For this amplifier, the power supplies are separated into two halves. The first half serves only those parts of the circuit that amplify small signals at the input side, while the second serves the large signal and output positions of the circuit. This prevents the larger output signal swings from generating small feedback signals in the sensitive small signal parts of the circuits. Another aspect of the layout that reduces unwanted coupling into the input signal is the long, thin left-to-right geometry of the layout. Small input signals enter on the far left, while the output signals exit on the far right. This maximizes the separation of the sensitive input stages from the larger signal output

stages. Finally, the bonding pads on the critical signal path are as small as possible to minimize the pad capacitance.

To bond the compound semiconductor photodetector to the circuit at the signal input side, two small pads are required with open overglass. The pad size must be as small as possible to minimize the pad capacitance since this capacitance directly contributes to the input capacitance, and, in turn, increases the input impedance required. To reduce the input capacitance due to the pad, placing a floating n-well underneath the pad helps reduce the pad capacitance since the well capacitance is in series with the pad capacitance [32]. This technique also prevents the pad metal from spiking into the substrate.

Figure 8(a) shows the MAGIC layout before fabrication. The two small pads at left center are pads for detector integration. Unpackaged chips were obtained from MOSIS to allow post-processing. Figure 8(b) is a microphotograph of the chip after the integration of the photodetector. The size of the photodetector is 50 μm diameter. It has small metal contact

Place Figure 8

fingers extending from each of two sides of the detector on the bottom of the detector. A metal-semiconductor-metal (MSM) photodetector was selected since low capacitance per unit area is of vital importance in the design of high speed, low power and alignment tolerant photoreceivers. The I-MSM, with the electrodes defined on the bottom of the device, overcomes the low responsivity problem of conventional MSM detectors with fingers on the top by eliminating the shadowing effect of the electrodes [33]. I-MSMs demonstrated up to 0.7 A/W responsivity and the leakage current is low, less than 10 nA at 10 V bias. The frequency response is up to 6 GHz. The measured capacitance was 70 fF for 50 μm active area I-MSMs with 1 μm finger width and

spacing. This capacitance is negligible compared to the input pad capacitance of the first stage.

The integrated OEICs were packaged in a high-speed LDCC package. A special test board was designed using microstrip line techniques to test at full speed.

Place Figure 9

5. Measurements

An eye diagram and a pulsed waveform of these integrated receivers were measured using 2^7-1 NRZ pseudorandom data. Our target operating speed was 155 Mbps. The amplifiers were designed to operate at a +5 V single power supply, but bipolar power supplies were used for all circuitry to simplify the test. However, bias currents and the detector bias were adjusted to achieve the best operating speed for each circuit. An output load of 50 Ω was used at the scope.

Figure 9 shows the test setup block diagram for the integrated receiver. The test setup requires a laser source, a modulator to illuminate the photodetector of the receiver, and an oscilloscope with a bandwidth of 1 GHz to monitor the output of the amplifier.

Figure 10 (a) shows the results of the 1.2 μm amplifier at 80 Mbps. At 155 Mbps, the eye diagram was completely closed. Figure 10 (b) illustrates the amplifier in the 0.8 μm process I at 155 Mbps. Figure 10 (c) is the eye diagram at 155 Mpbs of the amplifier with 0.8 μm process II. The amplitude of the output pulse was about 20 mV_{p-p}. Figure 10 (d) shows the results at 155 Mbps of the same amplifier as Figure 10 (c) but with an InGaAs, 1.3 μm/1.5 μm wavelength I-MSM photodetector. Figures 10(a) through (c) use a

GaAs-based photodetector. Table 2 shows the bias currents and power dissipation of each of the amplifiers measured.

From Figure 10 (c) and (d), the amplifier of Process II is slower than the one from Process I. That is partly because the gate capacitance, C_{gs} of the *n*-MOSFET and the drain-substrate capacitance, C_{db} of the *p*-MOSFET of Process II is larger than those of Process I [1] and partly because the characteristics of the p-channel MOSFET of Process II are not as good as those of Process I. The bandwidths of these amplifiers were determined by Eq. 5, and C_{gs} and C_{db} play a major role in determining the bandwidth.

The results from Figure 10 and Table 2 illustrate that as the minimum channel length of the transistors are scaled down from 1.2 μm to 0.8 μm with a scale factor λ of 1.5, the bandwidth of the amplifiers improves from 80 Mbps to 155 Mbps. The power supply voltage decreases to 5 V from 6 V and, therefore, the power dissipation of the amplifier decreases from 36 mW to about 24 mW.

Since the amplifiers are fabricated by standard digital CMOS processes, the constant-electric-field (CE) scaling law [22, 26-28] might be applied. However, due to the constant bias currents of the transistors, the constant-voltage (CV) or quasi-constant-voltage (QCV) [22] scaling law is optimum for analog and digital VLSI applications. Figure 11 plots the measurement results in Table 2 against each law. Clearly, this design seems to follow the QCV scaling laws. Under the QCV, the scaling law on the supply voltages is $\lambda^{-1/2}$ and the scaling law on the gain-bandwidth product or GBW is $\lambda^{3/2}$.

Place Figure 10

Place Tablee 2

Place Figure 11

6. Conclusions

A multi-stage, low-gain-per-stage, open-loop front-end current-mode transimpedance amplifier was designed and fabricated in different minimum feature size, standard digital CMOS processes through the MOSIS foundry. The amplifier consists of 5 identical cascaded stages. Each stage has a current gain of 3. The amplifier uses a process-insensitive design methodology and does not require any passive resistors. The total transimpedance amplifier gain is about 12 KΩ with a 50 Ω load. After integration of a compound semiconductor thin-film MSM photodetector onto the silicon circuitry, eye diagrams of each amplifier were measured and compared. Since the amplifier is used in the current-mode, the signal current from the MSM photodetector was sent directly into the input of the amplifier without requiring a resistor. The measurement results show that as the size of the device scales down, the bandwidth increases and the power dissipation decreases. The scaling factors shows the same results as the theoretical QCV scaling laws.

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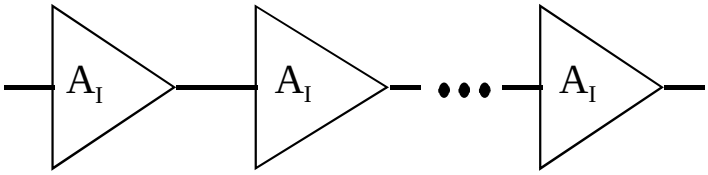


Figure 1. The block diagram of the amplifier.

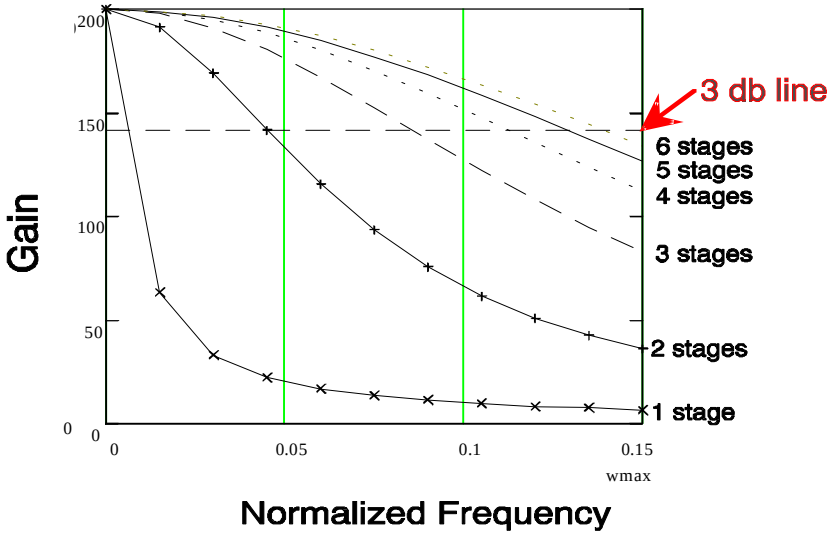
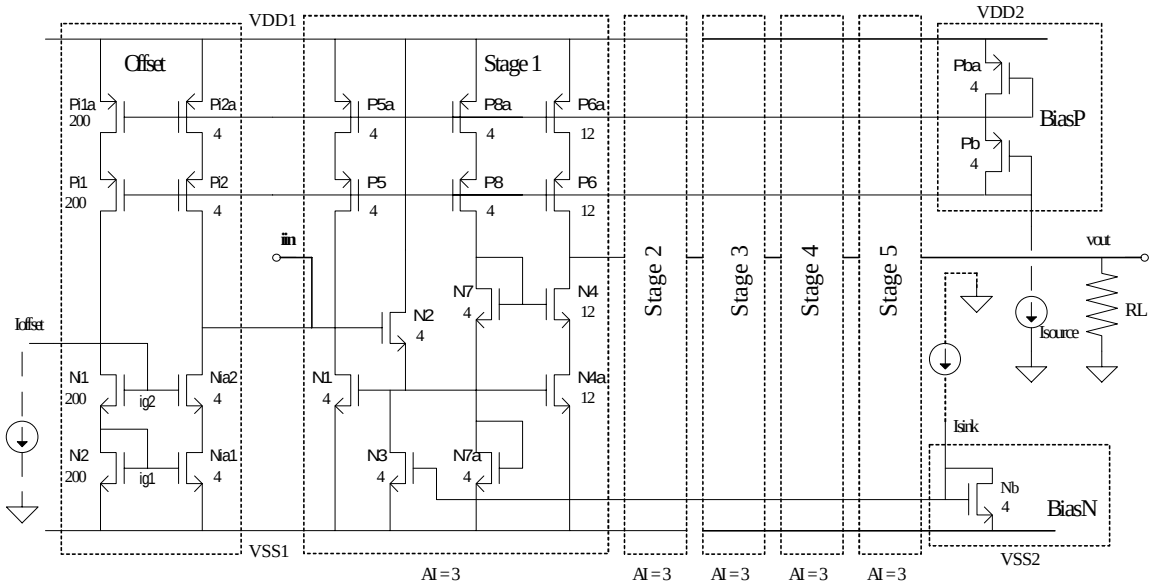


Figure 2. Frequency responses for different numbers of stages assuming a fixed gain and power consumption.



Transimpedance, R = AI**5*RL
= 243*RL

Figure 3. Overall circuit diagram of the amplifier.

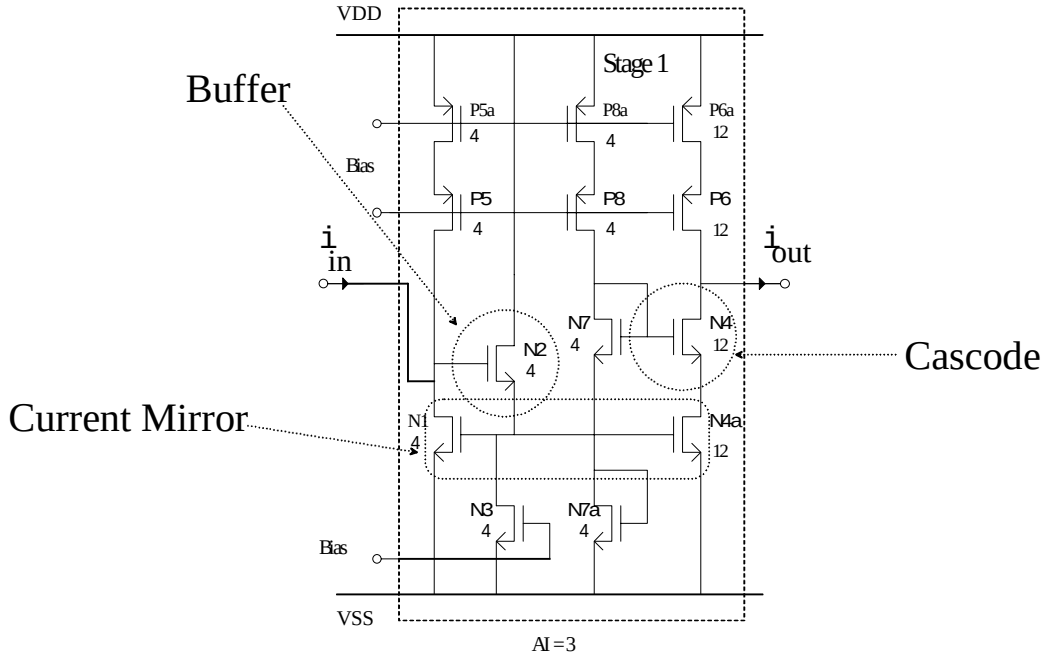


Figure 4. Circuit schematic of one stage.

Table 1. Key SPICE parameters for each process.

	n-channel MOS		*p*-channel MOS	
	K_P [$\mu A/V^2$]	V_{th} [V]	K_P [$\mu A/V^2$]	V_{th} [V]
1.2 μm	109	0.760	41.3	-0.940
0.8 μm (Process I)	125	0.750	62.4	-0.920
0.8 μm (Process II)	183	0.890	53.1	-1.03

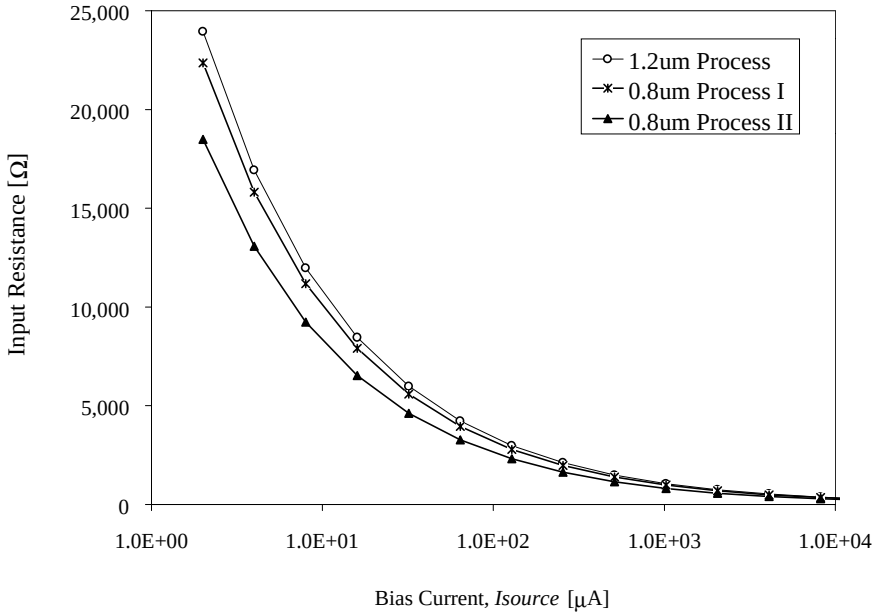


Figure 5. The input resistance at different bias currents.

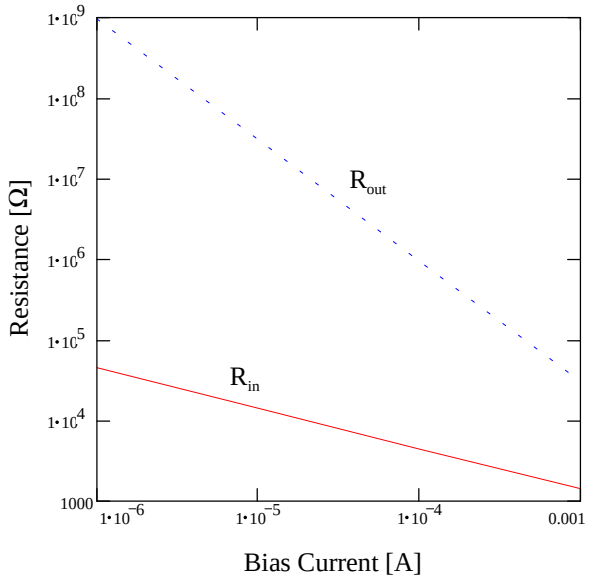


Figure 6. The input and output resistance values at each stage as the bias current changes. The process parameters from 0.8 µm technology were used.

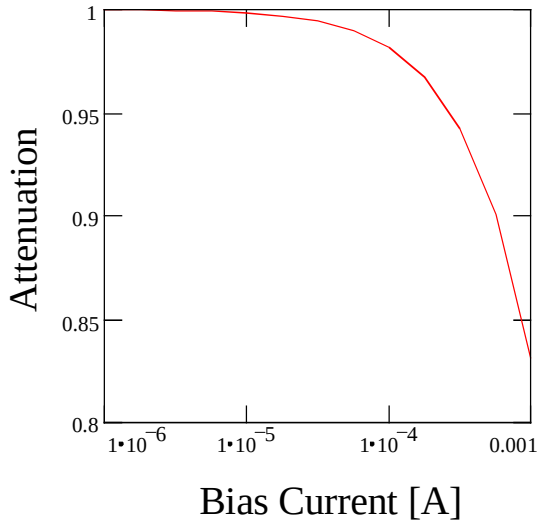
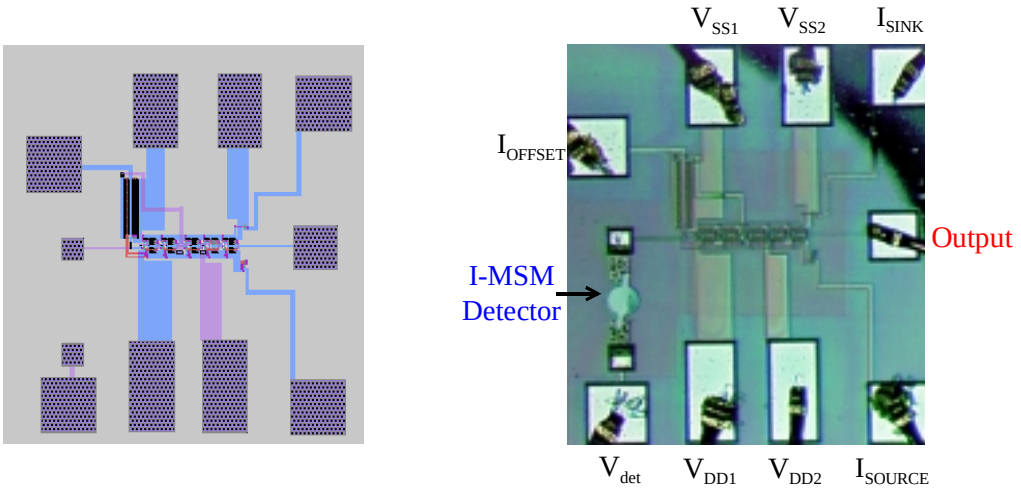


Figure 7. Effect of bias currents on the gain attenuation.



(a) MAGIC layout

(b) Microphotograph of 0.8 μm process chip.

Figure 8. The chip layout before fabrication and microphotograph of the OEIC after integration.

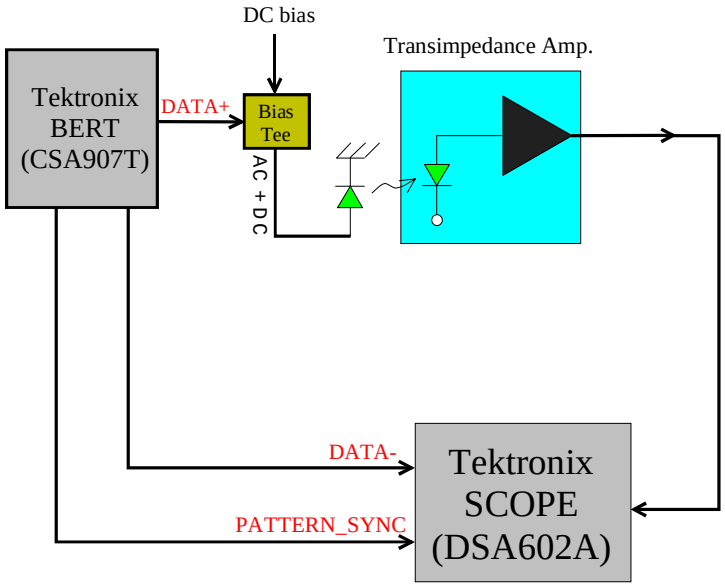
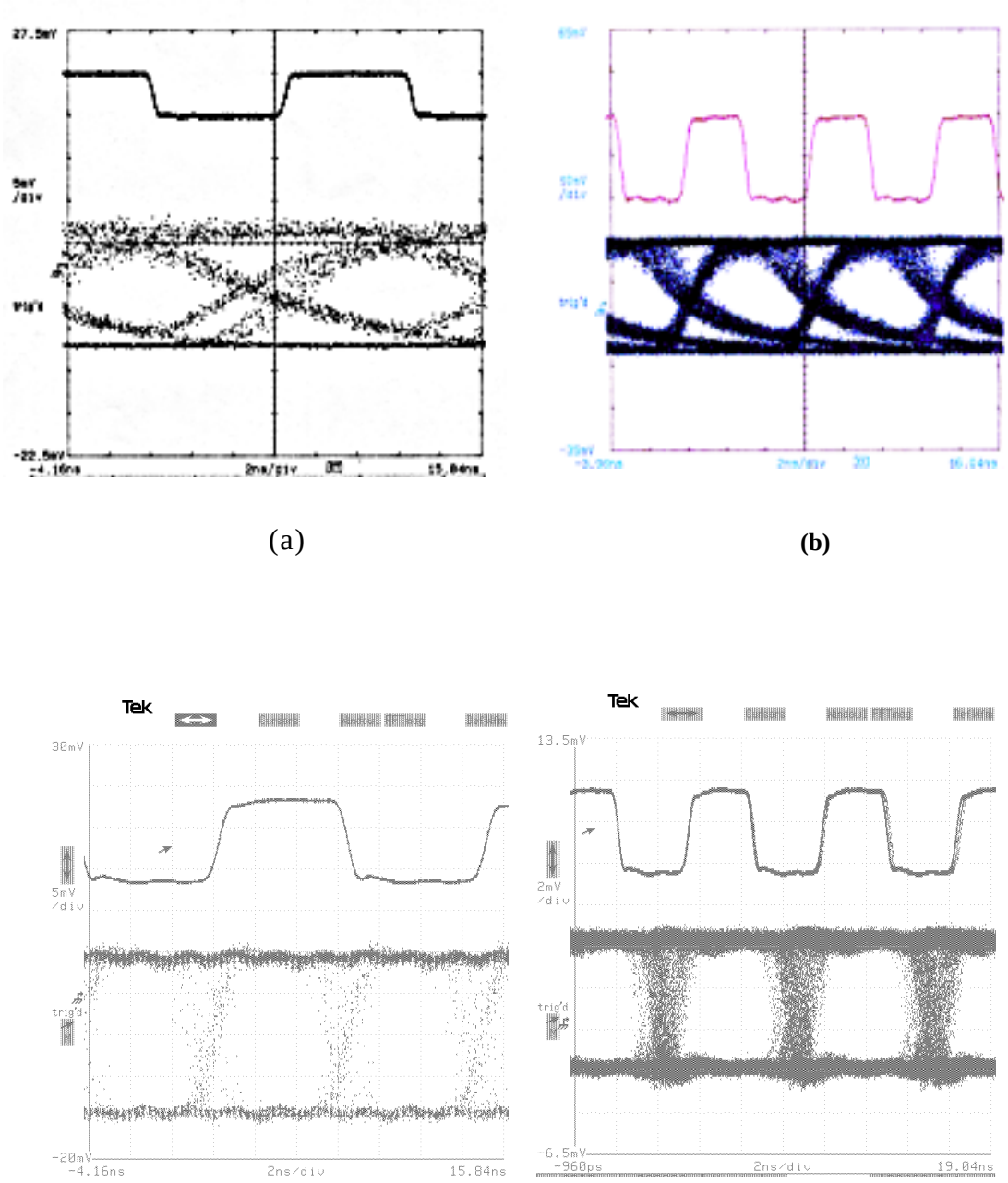


Figure 9. The block diagram of the test structure.



(a) **(b)**

(c) **(d)**

Figure 10. Eye diagrams and pulsed waveforms of each amplifier: (a) 1.2 µm process with GaAs photodetector at 80 Mbps; (b) 0.8 µm Process II with GaAs photodetector at 155 Mbps; (c) 0.8 µm Process I with GaAs photodetector at 155 Mbps; (d) 0.8 µm Process I with InGaAs detector at 155 Mbps.

Table 2. Bias condition and power dissipation of each amplifier.

	1.2 μm	0.8 μm (Process-II)	0.8 μm (Process-I)	0.8 μm (Process-I)
Photodetector Type	GaAs	GaAs	GaAs	InGaAs
I_{source} [μA]	-60	-58	-69	-69
I_{sink} [μA]	+60	+58	+69	+69
Power Supplies [V]	+/- 3	+/- 2.5	+/- 2.5	+2.5/- 2.2
Power Dissipation [mW]	36	24	25	20

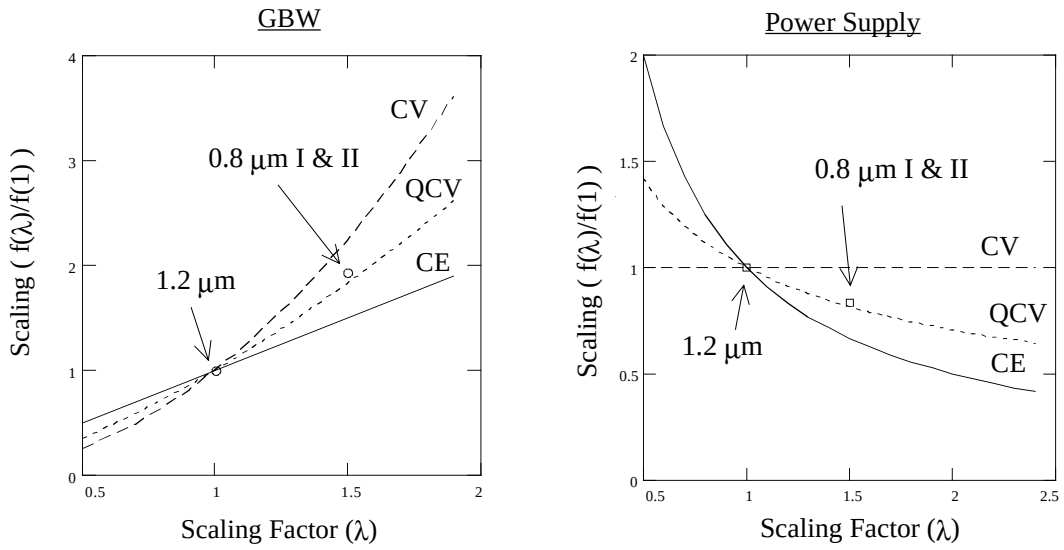


Figure 11. The curves of various scaling laws and measured data. The left and right graphs show the scaling effect on the gain-bandwidth product and power supply, respectively. Circles and rectangulars represent the measured data.