# Microsystem Optoelectronic Integration for Mixed Multisignal Systems

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***Abstract*—The integration and packaging of optoelectronic devices with electronic circuits and systems has growing application in many fields, ranging from long to micro haul links. An exploration of the opportunities, integration technologies, and some recent results using thin-film device heterogeneous integration with Si CMOS VLSI and GaAs MESFET circuit technologies are presented in this paper. Applications explored herein include alignment tolerant optoelectronic links for network interconnections, smart pixel focal plane array processing through the integration of imaging arrays with sigma delta analog to digital converters underneath each pixel, and three-dimensional computational systems using vertical through-Si optical interconnections.**

***Index Terms*—CMOS, GaAs, MESFET, optoelectronic devices, VLSI.**

## I. Short to Micro Haul Optoelectronic Links

As BANDWIDTH and interconnectivity demands have skyrocketed in applications from on-chip to long haul communication, higher levels of integration of optoelectronics with circuits to access higher levels of signal processing and for interconnection are emerging as key requirements in new systems. However, these goals must co-exist with more aggressive cost targets, especially for shorter haul products. In fact, products with optical communication distances at or under a kilometer, all the way down to the milli and micro haul range for electronic interconnection substrates (for System on a Package, or SOP) and for on-chip optical interconnection (for System on a Chip, SOC), are available or imminent in the near term [1]. The variety of products is expanding rapidly, so let us explore a few representative links as a function of nontraditional shorter distances. Optical links in the 0.5–1-km range are currently being developed for broad-band access to the home and small office as the demand for bandwidth at these sites escalates. In the range of under a kilometer, gigabit optical Ethernet was an early product whose market share may soon be subsumed by DSP-based multichannel electrical links for the shorter haul applications; however, announcements for 10-Gb Ethernet optical products, anticipated in 2000, represent a high-volume market which will likely not be easily replaced with wire alternatives. In the tens to few hundred meter range, 10-Gb/s multichannel optical link products are being announced for high data rate board to board interconnections. In the same range, IEEE 1394b optical fiber link interfaces are proposed for consumer electronic equipment for applications such as in-home broad-band networking. Optical fiber links exhibit another attractive feature that has prompted development in the tens to few hundred meter range, namely, electromagnetic interference (EMI) insensitivity and no EMI emission. Thus, engineers working on product classes that pose EMI system challenges, such as automotive and avionic systems, are exploring multiplexed optical fiber links as an attractive alterative to wire-based harnesses. In the milli haul range, high-density wiring (HDW) substrates (the generation of substrate interconnection technology which followed multichip modules, or MCMs) suffer from latency problems as pinouts (inputs/outputs) and interconnection complexity increases. At the micro haul range, for on-chip SOC optical interconnection, projections of the coming generation of Si CMOS electronic systems, termed giga-scale integration (GSI), indicate that the density and speed of CMOS-based systems will not be limited by the CMOS devices, but by the interconnections between devices [2]. To emphasize this limitation, the Semiconductor Industry Association (SIA) Roadmap points to CMOS interconnection technology as a critical technology which must advance to sustain the typical performance scaling (Moore's Law) of CMOS technologies, but they are unable to identify a current technology which will address this interconnection barrier. This interconnection limitation is projected to reach a critical stage in 2009 [3]. The Roadmap goes on to suggest that optical interconnection (the first mention of optics in an SIA Roadmap) and three-dimensional (3-D) architectures are potential solutions to this communication bottleneck projected at CMOS linewidths below 70 nm.

Optical links are now pervasive for long-haul communication; however, the cost of the high-performance optoelectronic interface components typically used in these systems is prohibitive for use in lower cost products which will be manufactured in high volume, moving toward commodity markets. For optical interconnection to become more pervasive to address the incessant demands for bandwidth expansion, the cost of optoelectronic links must decrease. Thus, the development

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of low-cost, high-performance optoelectronic links is a critical issue facing the field, from micro haul to metrohaul systems, since these systems cannot support high-cost interface components. This is a paradigm shift for the field of optoelectronic research, which has traditionally focused upon the highest performance regardless of cost. Now, an alternative design criterion for a new subset of engineers can be to set a performance specification and to focus upon cost reduction of the interface or subsystem while meeting that performance goal. Techniques under development which move toward this goal are device and integration design for cost-effective manufacture and for alignment tolerance, and subsequent low-cost, automated packaging.

The introduction of optoelectronics into electronic systems raises the specter of mixed multisignal systems, which are systems that have intimately integrated analog, digital, rf, and optical signals. Electrical system and microsystem engineers have faced the design and test of mixed signal systems in packages (SOP) which contain analog and digital signals, but with the emergence of optical signals for inter and intra connections to and in packaged systems, and higher speed RF signals entering the systems, the mixed signals now become mixed multiple signals. Even more challenging is the prospect of chip-based systems (SOC) which contain these mixed multiple signals. System analysis and optimization become highly complex when the models must include interfaces such as highly sensitive high-gain optoelectronic receivers in the same package or on the same chip as a highly noisy digital microprocessor. Thus, the education of a new intellectual generation of engineers and engineering teams will necessarily include the knowledge and tools necessary to model, design, and test systems which include analog, digital, RF, and optical signals.

In the pursuit of the modeling and design tools necessary to build mixed multisignal systems, it is important for researchers in the optoelectronic fields to advance the generation of models and circuit building blocks. The modeling tools could usefully take the form of semiempirical device and interface models for circuit simulators such as SPICE. These models need to take basic measured device parameters as inputs to the models, so that designers can adjust the models based upon the characteristics of the devices used in their systems. Additionally, since few electrical engineers are currently educated in the area of optoelectronics, the development of basic optoelectronic interface circuit building blocks, which are optimally scalable (which scale in performance as CMOS linewidths decrease), is critical [4]. These building blocks, with well-defined input/output specifications, will enable designers whose education is primarily in electricallybased design to access optical interfaces with an initial minimum of additional education. Thus, the inclusion of optoelectronic interfaces in electronic designs need not face the potential barrier of engineering education lagging product design requirements.

## II. Optoelectronic Integration

For interconnection distances in the cm to multi-km range, the traditional approach to optoelectronic system realization is hybrid packaging, i.e., independently manufactured optical devices mounted on a board or interconnection substrate next to analog transceiver circuitry. The optoelectronic (OE) devices are electrically connected to the transceiver circuitry through either wire bonds (chip-to-chip wirebonds are risky for reliability, so usually each chip is bonded to a board) or through bump bonds that are electrically connected on the mounting board. As data rates increase, the parasitics associated with this packaging technology degrade performance, unless compromises are made which lead to more costly assembly. For example, small detector capacitance may be necessary to overcome input parasitics to the receiver, which may lead to very small detectors, thus posing optical alignment challenges which lead to higher cost implementations. New methods for the direct integration of OE devices with circuits that are still independently optimized but with enhanced assembly to reduce cost, are needed. The allegory to this packaging story is that of the transition of discrete electronic devices mounted onto boards to integrated electronic circuits. The fastest discrete electronic circuits still outperform integrated electronic circuits, but the discrete implementation is much more costly, and is thus rarely used. An interesting footnote is that the integration of electronic (and now, optical) passives into SOP interconnection substrates is an area of active investigation, awaiting a low cost implementation to become mainstream.

To access high-yield, low-cost Si CMOS VLSI for complex signal processing functions and to integrate optical interconnection into Si CMOS VLSI microsystems for higher data rates over shorter distances for SOC, the integration of OE devices with CMOS analog OE transceivers and with digital Si CMOS VLSI is essential. Si CMOS receivers have been demonstrated with electrical gigabits per second operation (not integrated with OE devices) [5], and recently, integrated directly with an InGaAs photodetector [6]. Optoelectronic device integration with foundry digital Si CMOS, and the independent optimization of the Si CMOS and the OE devices, have been demonstrated with monomaterial (all components in Si) and in hybrid integrated approaches, however, Si CMOS detectors operate at short wavelengths (below $\lambda = 950$ nm) with low responsivity, shallow channel depth (resulting in a thin optical absorption length) or at a slow speed (with gain, such as an optically sensitive base in a BJT) [7], and emitters have been demonstrated only with weak optical emission through defect centers [8]. Efficient optoelectronic interconnections require integration technologies that enable the independent optimization of III–V compound semiconductor devices with Si CMOS VLSI signal processing and computational circuitry.

One method of combining OE materials with Si CMOS VLSI circuits utilizes hybrid epitaxial growth of III–V optoelectronic materials directly onto Si circuitry. The devices reported in the literature suffer from short lifetimes and low efficiencies due to lattice constant mismatch and differing coefficients of thermal expansion [9], or the Si CMOS is damaged by the relatively high-temperature growth process [10], which often causes additional CMOS junction diffusion, although there have been reports of hybrid growth success for modulators on Si substrates [11].

Hybrid integration technologies, where the III–V compound semiconductor material or device is bonded to a Si CMOS VLSI circuit in a CMOS post-fabrication integration sequence, have the potential to create intimately bonded systems with

independently optimized components. Wafer bonding is a technique which uses high pressure and elevated temperatures to atomically bond compound semiconductor device layers to host substrates such as Si or a coated Si substrate [12]. Post processing of the compound semiconductor materials results in devices. These bonding technologies for heterogeneous integration have not yet been reported on Si CMOS circuitry. The drawbacks to wafer bonding include the mismatch between Si VLSI wafer size and compound semiconductor wafer size, which will most likely remain mismatched with time. Thus, for Si CMOS VLSI wafer scale integration, multiple compound semiconductor wafers would need to be bonded or the Si wafer diced to smaller dimensions. A second issue is that the density of compound semiconductor devices for many applications is not the same as that of the Si CMOS VLSI. Thus, while an entire wafer has been bonded, the device layers are only necessary in a relatively small region, thus wasting a potentially large percentage of the relatively expensive compound semiconductor growth.

Flip-chip or bump bonding, is a second hybrid approach for the heterogeneous integration of compound semiconductor devices onto Si CMOS circuitry. Bump bonding has been used in the electronics industry reliably for board mounting and is being used increasingly for chip mounting to high-density interconnection substrates for multichip systems as well. Electronics industry approaches to high-reliability chip bump bonding utilize wafer-scale In-based plated solder balls, which, post dice, are then attached to an interconnection substrate using an alignment and reflow tool. Studies of the speed of bump bond vertical transitions indicate that bump bond electrical transitions can support high-speed operations [13]. Bump bonding of linear and two-dimensional arrays of optoelectronic devices to circuits have been reported [14], and bump bonding promises to be a viable heterogeneous integration technology for arrays of optoelectronic devices. There are a number of drawbacks to bump bonding of optoelectronic devices to circuits, which are more or less critical, depending upon the specific application. The first is the requirement that all device electrical contacts be brought out to the front surface for bump interconnection. This often complicates the fabrication of the compound semiconductor devices (either optoelectronic or high-speed electronic, or a mixture of the two), since the device contacts are generally not in the same epilayer plane and, thus, planarization and planar bumping must be addressed through additional etch, deposition, and masking steps, thus compromising yield. For highly advanced systems, the integration of multiple, independently fabricated arrays of compound semiconductor devices is an assembly challenge. An assembly challenge which has not been addressed is the bump bonding of single devices onto a substrate. Secondly, the compound semiconductor substrate remains on the devices, a disadvantage for some optical applications, where the substrate is absorbing, and thus the optical signal can neither exit nor enter from the surface. An additional highly significant negative to the bump bonding scheme is that the integrated transceiver cannot itself be flipped over and bump bonded to a system interconnection substrate because the optoelectronic device substrate is much thicker than standard bump bonds. One method of circumventing this problem is certainly to etch a large hole in the interconnection substrate to accommodate the optoelectronic device with substrate, but this adds additional interconnection substrate deep etch processing steps which are currently nonstandard, and may severely limit the electrical interconnection substrate layout. An additional drawback to retention of the optoelectronic device substrate is that it precludes the 3-D stacking of multiple devices.

Removal of the compound semiconductor growth substrate has numerous advantages, particularly for optoelectronic applications. Since the functional portions of most high-speed electronic and optoelectronic compound semiconductor devices reside in the grown epilayers of the devices, substrate removal does not affect the device performance and may even enhance device performance by removing an optically absorbing substrate and providing access to electrical contacts on the other side of the device. Some types of thin-film integration enable the independent optimization, fabrication, and testing of the OE and electronic components prior to bonding to the circuit, thus enabling known good die paradigms to be implemented. In fact, foundry Si CMOS VLSI can be accessed and simply post-processed to add the OE components through metallized bonding techniques. There are two basic approaches to thin-film integration, with many variations arising in these two approaches. In the first approach, the compound semiconductor devices are bonded to the host circuit or substrate, with subsequent compound semiconductor substrate removal. This technique can utilize either bump bonding techniques [15] or thinner metallized contacts. The process engineer must be careful to protect the edges of the compound semiconductor devices and the host substrate (e.g., Si CMOS VLSI circuit) during the substrate removal process, which is generally accomplished with either a wet or dry selective etch. The drawbacks to this process are the subset of those associated with bringing all contacts to one face for bump bonding.

An approach to thin-film integration which addresses the drawbacks to bump bonding involves selective compound semiconductor substrate removal prior to integration with the host substrate Si CMOS circuit. This thin-film heterogeneous integration technique enables independently optimized devices (typically 0.1–5 $\mu$m thick) to be selectively aligned and bonded to the host substrate using a transparent transfer diaphragm [16]. Metallized contacts to the host substrate circuit and to the OE device(s), either in single, or array format, form highly reliable thin-film electrical and mechanical contacts. This results in a virtually planar hybrid integrated optoelectronic circuit (OEIC) and enables front and back device contacts, the vertical scalability of stacked thin-film devices, and the mixing and matching of independently optimized multiple OE devices with circuits using standard foundry microfabrication techniques. Fig. 1 illustrates one separation, transfer, and bonding process. There are many variations of this process [16], and the process can and should be varied to optimize the integration of a particular microsystem. Fig. 2 is a photomicrograph of a GaAs metal–semiconductor–metal (MSM) thin-film photodetector which has been separated from the growth substrate using lateral selective etching, and then contact-bonded to a host silicon nitride-coated silicon substrate. Thin-film photodetectors bonded to host substrates in this manner have

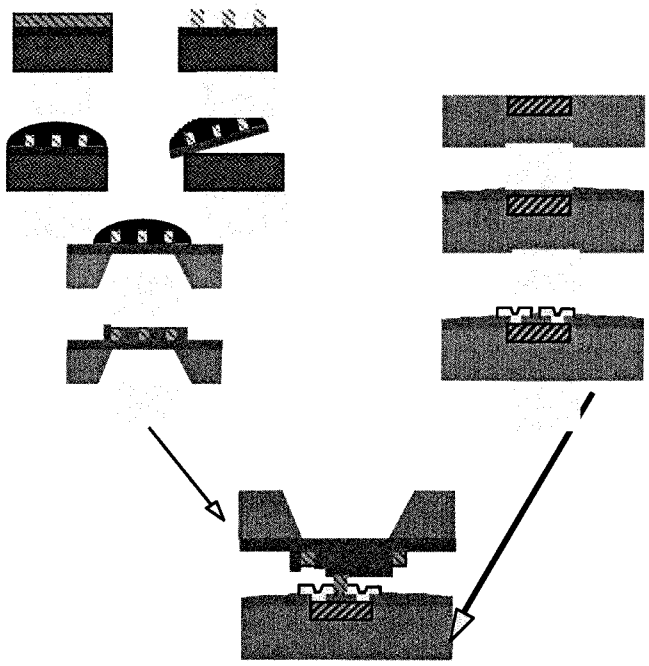

Fig. 1. Thin-film hybrid integration process: (a) as-grown epitaxial sample, (b) top contacted and mesa etched, (c) embedded in Apiezon W handling layer, (d) selective etch substrate removal, (e) bonded to transparent transfer diaphragm, (f) handling layer removed, (g) foundry Si CMOS VLSI circuit, (h) Si CMOS VLSI circuit planarized (if necessary), (i) metallized bonding pads on Si CMOS VLSI circuit for OE device, and (j) OE thin-film device bonded to host substrate (e.g., Si CMOS VLSI circuit).

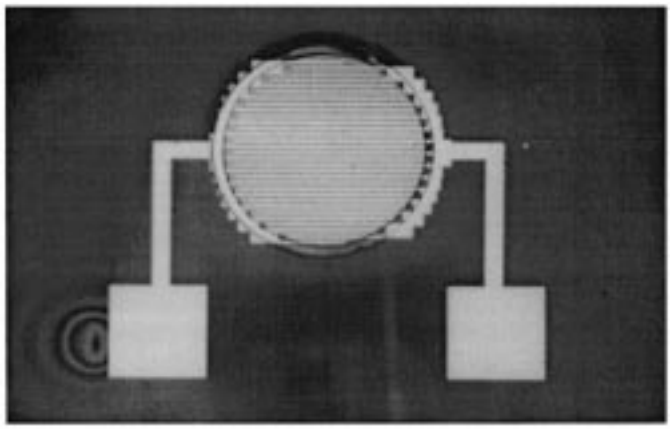

Fig. 2. Thin-film GaAs-based MSM bonded to silicon nitride-coated Si host substrate.

demonstrated operation in excess of 6 GHz [17], [42]. This transfer diaphragm technique is cost effective from a material usage standpoint, since it can distribute the thin-film devices sparsely, and many host substrates (or a 12-in Si CMOS VLSI wafer, or a 16-in high-density interconnection substrate) can be integrated sparsely with a fraction of one thin-film array of devices. The transfer diaphragm technique can be used to either invert or not invert devices. In some cases, inverting the thin-film devices is advantageous. If the devices are inverted, both sides of the thin-film devices can be processed while under rigid substrate (either growth or host) support. This is useful for bonding, since the side of the device that was processed (e.g., metallized) before separation is now bonded to the host substrate, which can also be metallized. Thus, the metal contact on the thin-film device and a metallized host substrate will form a stable electrical and mechanical bond when the metal–metal contact is (optionally) annealed after contact bonding. The primary drawback to this type of thin-film integration is that the cost has been transferred to the assembly process. However, with the advent of thin-film Si circuits, this handling and assembly issue is now being addressed by the semiconductor industry.

## III. Heterogeneously Integrated Links for Mixed Multisignal Systems

A number of heterogeneously integrated links and microsystems have been demonstrated using thin-film integration techniques. One example of a OEIC link that has been demonstrated using this integration technique is cyclic redundancy code-error detection hardware integrated directly with transmitter and receiver Si CMOS VLSI circuits to realize a mixed multisignal OE, analog, and digital microsystem [18]. This OEIC has an integrated thin-film resonant cavity enhanced thin-film light-emitting diode integrated onto a transmitter driver circuit, and demonstrated an improvement in bit error rate (BER) of a factor of over 100 due to the inclusion of the error-detection circuitry. A second example is an imaging array with signal processing Si CMOS VLSI electronics under each pixel, shown in Fig. 3. Each pixel has a Si CMOS VLSI luminance to frequency converter with an interconnection pad. A second imaging array has also been integrated that has a sigma delta analog to digital converter under each pixel (and looks the same as Fig. 3). The ADC under each pixel enables noise shaping and the image data to be transferred in a digital format, thus producing a low-noise signal output, and a plethora of signal processing options, including dynamic signal processing tradeoffs between frame rate and resolution. This enables the user, for example, to peer into imaged shadows at a lower frame rate (like taking a second, closer look). To fabricate the OEIC, the CMOS circuit is planarized, an electrical interconnection via cut through the planarization material, a bottom metal contact deposited, and the thin-film GaAs–AlGaAs P–I–N RCE detector array is bonded onto the contacts. To assure registration of the detectors in the array, a linking layer of compound semiconductor is left between the pixels. Each pixel in the array is individually contacted to the signal processing circuitry beneath it, for massively parallel processing of the imaging array pixels. The integration is completed by reactive ion dry etching of the linking layer, followed by a layer of spin-on isolation with a second via cut to the top of the device for a common top contact, and contact metallization and definition [19]. This same approach has also been used to integrate a thin-film resonant cavity-enhanced light-emitting diode $8 \times 8$ array onto an $8 \times 8$ array of 5-b digital to analog converter/memory to display gray scale images [20]. Both the integrated emitter and detector arrays can be used for 2-D optical links.

Addressing packaging cost with heterogeneous integration is important to achieve low-cost realizations. The packaging of optical links and systems can be significantly improved, with associated cost benefits, if optical alignment tolerance is designed

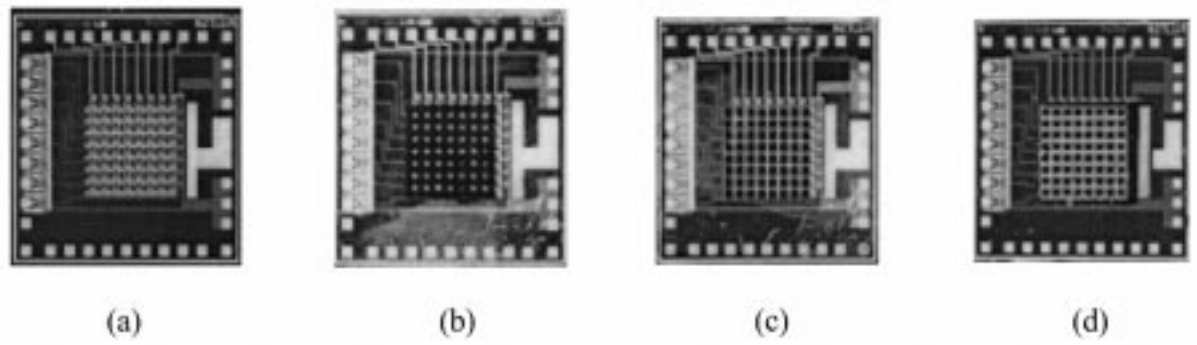


Fig. 3. Photomicrographs of $8 \times 8$ array process: (a) circuit (b) thin-film P–i–N detector devices with linked layer bonded to planarized/via cut/metallized circuit (c) linking layer removed, (d) planarization/isolation, top via metal contact completed.

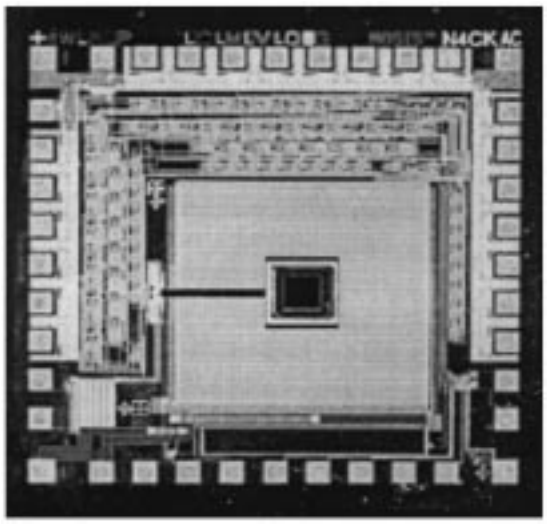

Fig. 4. Hybrid integrated OEIC with a thin-film resonant cavity-enhanced light-emitting diode bonded into the center of a Si CMOS BJT array. The analog transmitter and receiver circuitry and digital signal processing circuitry surround the detector.

into the links. Essentially, this is design for yield. One example of a hybrid integrated OEIC link that is alignment tolerant is the OEIC shown in Fig. 4. This link utilizes a thin-film resonant cavity-enhanced light-emitting diode bonded directly into the center of an array of Si CMOS BJT detectors [7]. This link is slow, due to the BJT detectors, but sensitive, since they exhibit a responsivity of 30 A/W (there is gain in the photoaddressed base of the BJT). The transmitter and receiver circuitry is implemented in Si CMOS VLSI, as is digital signal processing circuitry, all of which surround the Si CMOS BJT detector array. This colocated emitter/detector OEIC is designed to operate in slow (1 Mb/s), short haul (1–10 m) single fiber bidirectional optical links optimized for EMI-sensitive automotive/avionic applications.

The longitudinal (distance of the fiber from the surface of the OEIC) and transverse (side-to-side) alignment tolerance of these OEICs were measured. The 3-dB coupling attenuation due to longitudinal alignment was 1.5 mm for the LED-fiber separation, and 1.6 mm for the fiber-detector separation using a 1-mm core diameter plastic optical fiber. The measured and theoretical longitudinal alignment tolerance were in good agreement. The measured and theoretical $-3$-dB transverse alignment tolerance with a 1-mm longitudinal separation is $\pm 0.4$ mm for the LED-fiber separation, and $\pm 0.7$ mm for the fiber-detector separation [21].

Another example of higher speed alignment tolerant optoelectronic links is an integrated receiver. To demonstrate an alignment tolerant hybrid integrated receiver, metal–semiconductor–metal (MSM) photodetectors are of interest since they are high-speed, large-area photodetectors with moderate responsivity and a larger capacitance per unit area than PIN detectors at high speed. However, the responsivity of MSMs is significantly smaller than that of PINs. When an MSM has the substrate removed and is inverted (an I-MSM, which has the metallic fingers on the bottom of the device, rather than on the top), the responsivity can equal that of a typical PIN (0.7 A/W), yet retain the low capacitance per unit area attractive feature of conventional MSMs. The input capacitance into a receiver largely dictates the speed of the receiver, so minimizing the detector capacitance is critical. In addition, since the thin-film detector can be integrated directly onto the Si CMOS receiver circuit, matching the input resistance to that of a typical 50-ohm package is no longer necessary. Thus, a higher receiver input resistance can be used, reducing the receiver noise. Fig. 5 is a photomicrograph of a thin-film InP–InGaAs ($\lambda = 1.3$ $\mu$m) I-MSM metal/metal bonded to a Si CMOS differential receiver circuit (for operation in a noisy digital environment), which has been tested with an open eye diagram at 250 Mb/s. Recent results for hybrid integrated OEIC receivers with InP–InGaAs thin-film detectors bonded to a 0.25-$\mu$m Si CMOS differential receiver circuit operate at 1 Gb/s with a 250-$\mu$m on a side I-MSM, and bonded to a GaAs MESFET circuit, operate at 2.4 Gb/s with a 50-$\mu$m diameter I-MSM [22].

Heterogeneously integrated transceivers designed for high yield through alignment tolerance may be integrated into SOP and SOC microsystems to realize mixed multisignal systems which address interconnection limitations. In the SOP realm, although materials research is providing improvements in electrical interconnects by utilizing advanced materials (aluminum and standard $SiO_2$ are being replaced with copper and titanium nitride for higher performance interconnections [23]), optical interconnections can provide high-speed, low-loss, low-latency, massively parallel, crosstalk resistant communication, enabling links and signal processing systems suitable for chip-to-chip,

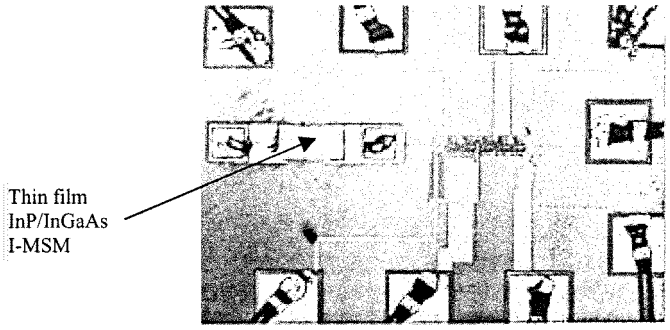


Fig. 5. Hybrid integrated OEIC with InP–InGaAs I-MSM bonded to 0.6-$\mu$m Si CMOS VLSI receiver.

chip-to-board and board-to-board SOP applications [24], [25]. The emergence of waveguide interconnected SOP substrates which combine electrical and optical functions address issues such as low latency clock distribution in the SOP. Use of heterogeneous integration techniques, and, in particular, thin-film integration techniques, for embedded active and passive SOP substrates and microsystems, is emerging as an important optoelectronic interconnection application in the milli-haul range.

Interconnection is an even more pressing issue in microsystems on a chip (SOC). Perhaps the best example to date of a heterogeneously integrated mixed multisignal microsystem is the report of the first single chip optically interconnected microprocessor [26]. This microsystem contains a thin-film I-MSM bonded to the input of a 0.8-$\mu$m Si CMOS differential analog receiver whose outputs feed a Si CMOS VLSI microprocessor. All of these components are integrated onto a single chip, creating a truly challenging mixed multisignal environment with optical, analog, and highly noisy digital signals.

Three-dimensional CMOS architectures with optical interconnections enable the development of advanced microsystems which may address the electrical interconnection limitations of future CMOS technologies [27], [28]. With the integration of thin-film emitters and detectors onto Si CMOS VLSI circuitry, one can envision optical link usage on a SOC level for Si CMOS VLSI circuits and microsystems. As previously mentioned, a significant limitation to SOC microsystems lies in the interconnection of the processing circuitry. Utilizing the SIA roadmap suggestions of using optical interconnections and 3-D interconnections, it is possible to envision vertical optical interconnections between layers of foundry Si circuitry using wavelengths to which the Si circuitry is transparent. Massively parallel applications such as image processing, image generation, and routing can be mapped into architectures which are well suited to 3-D interconnection structures. These architectures, which utilize multiple processors, are systems that could benefit from 3-D vertical optical interconnections. Vertical optical communication through Si circuits for 3-D interconnections was demonstrated using an external solid state laser operating at $\lambda = 1.3$ $\mu$m [29]. Since then, three different demonstrations of vertical optical communication through stacked Si substrates have been reported in the literature [30]–[32]. The first technique utilizes advanced GaAs-based emitters flip-chip bonded to the Si circuits. Unfortunately, optical absorption for this through-Si link is high because the emission energies of these devices is larger than the bandgap of Si, [$E_g(\mathrm{Si}) = 1.0$ eV, $\lambda_g = 1.1$ $\mu$m] [33]. To achieve low-loss propagation in this system, the use of laser drilled free space waveguides through the host substrates is required [30]. The second demonstration utilizes three GaAs-based vertical cavity surface emitting lasers (930 nm $< \lambda <$ 950 nm) for multiple wavelength reconfigurable communication to three separate substrates containing flip-chip bonded multiple-quantum-well detectors. The emitters in this demonstration are all located at the same plane and operate at wavelengths that experience absorption through the substrate. The novelty of this system is that it allows a single source plane and the option to choose the individual receiver plane by choosing the wavelength [31].

The third method utilizes integrated InP-based optoelectronic devices operating at $\lambda > 1.2$ $\mu$m which are bonded directly to Si circuits. This technique has been used to produce two layer through-Si CMOS vertical optical interconnections [34]–[36], a 40-Mb/s single channel link [36], and a three-layer stack of Si CMOS VLSI transceivers which utilized two consecutive through-Si vertical optical links [37]. Since these through-Si 3-D links can be utilized in a Si CMOS VLSI system, the prospects of using these optical links for 3-D interconnections in multiprocessor, massively parallel computational systems have been studied in some depth, with significant enhancements in system performance anticipated for these 3-D topologies [38]–[41].

## IV. Conclusion

Emerging heterogeneous integration techniques for integrating OE devices, analog interface circuitry, RF circuitry, and digital logic into mixed multisignal systems holds great promise for new packaged (SOP) and chip-based (SOC) microsystems. System design for high-yield, low-cost, alignment-tolerant mixed multisignal microsystems is paramount for optoelectronics to achieve pervasive implementation in lower cost, shorter haul electronic systems. High-volume product opportunities are emerging for new optical interconnection lengths ranging from micro haul SOC to milli haul SOP to short haul due to the societal thrust toward ubiquitous high bandwidth data access, but cost is a critical factor in the development of these products. There will be products that address these needs; will they contain optoelectronic components? The current packaging solution for optoelectronic interfaces in electronic systems in through packaged discretes. The high volume product solutions will contain integrated communication links, whether they be optical or electrical. Thus, integration of optoelectronic components with signal processing technology (current Si CMOS VLSI) is one significant step toward optoelectronic integration into electronic systems.

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## REFERENCES


[1] "Optical interconnections for digital systems," *Proc. IEEE*, vol. 88, June 2000.

[2] J. D. Meindl, "Gigascale integration: Is the sky the limit," *Circuits and Devices*, pp. 19–32, Nov. 1996.

[3] , http://notes.sematech.org/97pelec.html, Aug. 1998.

[4] M. Lee, O. Vendier, M. Brooke, and N. Jokerst, "A scaleable CMOS current-mode preamplifier design for an optical receiver," *Int. J. Analog Circuits Signal Processing*, vol. 12, no. 2, pp. 133–144, Feb. 1997.

[5] M. Govindarajan, S. Siala, and R. N. Nottenburg, "Optical receiver systems for high speed parallel digital data links," *IEEE J. Lightwave Technol.*, vol. 13, pp. 1555–1565, July 1995.

[6] M. Vrazel, Georgia Tech, private communication, 2000.

[7] J. Cross, B. Buchanan, L. Carastro, A. Lopez-Lagunas, T. Wang, N. Jokerst, M. Brooke, S. Wills, and M. Ingram, "A single fiber bi-directional optical link using co-located emitters and detectors," *IEEE Photon. Technol. Lett.*, vol. 8, Oct. 1996.

[8] T. G. Brown, P. L. Bradfield, and D. G. Hall, "Optical emission from crystalline Si," in *Proc. SPIE*, vol. 704, 1987, pp. 38–42.

[9] G. W. Turner, C. K. Chen, B. Y. Tsaur, and A. M. Waxman, "Through-wafer optical communication using monolithic InGaAs-on-Si LEDs and monolithic PtSi–Si Schottky-barrier detectors," *IEEE Photon. Technol. Lett.*, vol. 3, pp. 761–763, Aug. 1991.

[10] L. A. Hornak, S. K. Tewksbury, and H. E. Nariman, "GaAs heteroepitaxy with submicron Si CMOS: An experimental compatibility study," *Proc. SPIE*, vol. 1849, pp. 38–47, 1993.

[11] K. W. Goossen *et al.*, "GaAs/AlGaAs multiquantum well reflection modulators grown on GaAs and Si substrates," *IEEE Photon. Technol. Lett.*, vol. 1, pp. 304–306, Oct. 1989.

[12] U. Gosele, U. G. Kastner, S. Senz, P. Kopperschmidt, A. Plossl, R. Scholz, Q. Tong, Y. Chao, and L. Huang, "Wafer bonding: A flexible approach to materials integration," in *Conf. Proc. Eleventh Int. Conf. Indium Phosphide and Related Materials (IPRM'99)*, 1999, p. 231.

[13] D. Staiculescu, J. Laskar, and J. Mather, "Design rule development for microwave flip chip applications," in *IEEE 8th Topical Meeting on Electrical Performance of Electronic Packaging*, 1999, pp. 231–234.

[14] Y. Liu, E. Strezelecka, J. Nohava, M. Hibbs-Brenner, and E. Towe, "Smart-pixel array technology for free-space optical interconnects," *Proc. IEEE*, vol. 88, pp. 764–768, June 2000.

[15] A. Krishnamoorthy and K. Goossen, "Optoelectronic-VLSI: Photonics integrated with VLSI circuits," *IEEE J. Select. Topics in Quantum Electron.*, vol. 4, pp. 899–912, 1998.

[16] C. Camperi-Ginestet, M. Hargis, N. Jokerst, and M. Allen, "Alignable epitaxial lift-off of GaAs materials with selective deposition using polyimide diaphragms," *IEEE Photon. Technol. Lett.*, vol. 2, pp. 1123–1125, Dec. 1991.

[17] O. Vendier, N. M. Jokerst, and R. Leavitt, "High performance thin-film inverted MSM photodetectors," *IEEE Photon. Technol. Lett.*, vol. 8, pp. 266–268, Feb. 1996.

[18] P. May, J. Cross, A. Lopez, S. Wills, N. Jokerst, and M. Brooke, "Improvement in bit error rate for optoelectronic multicomputer interconnection networks using cyclic redundancy code error detection," *IEEE Photon. Technol. Lett.*, vol. 9, pp. 848–850, June 1997.

[19] S. Fike, B. Buchanan, N. M. Jokerst, M. Brooke, T. Morris, and S. DeWeerth, "8 × 8 array of thin-film photodetectors vertically electrically interconnected to silicon circuitry," *IEEE Photon. Technol. Lett.*, vol. 7, pp. 1168–1170, Oct. 1995.

[20] S. Wilkinson, J. Tabler, N. Jokerst, M. Brooke, and R. Leavitt, "An 8*8 array of resonant cavity enhanced light emitting diodes integrated onto silicon grayscale (32 level) driver circuitry," in *Proc. IEEE LEOS 9th Annual Meeting*, vol. 2, Boston, MA, Nov. 18–19, 1996, pp. 277–278.

[21] J. Cross, M. Thomas, and N. M. Jokerst, "Alignment tolerant smart pixel bi-directional optoelectronic links using co-located emitters and detectors," in *Proc. Integrated Photonics Research Conf.*, Victoria, Canada, Mar. 29–Apr. 3, 1998, pp. 260–262.

[22] C. Chun, O. Vendier, E. Moon, J. Laskar, H. C. Ki, N. M. Jokerst, M. Brooke, and J. Mondal, "Integrated 1.55 m receivers using GaAs MMICs and thin-film InP detectors," in *1998 IEEE Radio Frequency Integrated Circuits (RFIC) Symp.*, Baltimore, MD, June 7–9, 1998, pp. 187–190.

[23] N. Awaya, Y. Arita, H. Inokawa, and T. Kobayashi, "Copper interconnection technology for Si large scale integrated circuits," *NTT R&D*, vol. 45, no. 4, pp. 373–378, 1996.

[24] R. T. Chen *et al.*, "60 GHz board-to-board optical interconnection using polymer optical buses in conjunction with microprism couplers," *Appl. Phys. Lett.*, vol. 60, pp. 536–538, 1992.

[25] M. Koyanagi *et al.*, "Three-dimensional memory LSI with optical interconnections," *Electron. Commun. Japan*, pt. 2, vol. 76, no. 2, pp. 1–13, 1993.

[26] J. Chang, M. Vrazel, M. Brooke, and N. Jokerst, "Mixed signal hybrid OEICs: An InP I-MSM integrated onto a CMOS analog optical receiver with a digital CMOS microprocessor," in *Optoelectron. Computing Conf.*, Quebec, Canada, June 2000.

[27] S. Tang and R. Chen, "1-to-27 highly parallel three-dimensional intra and inter board optical interconnects," *IEEE Photon. Technol. Lett.*, vol. 6, pp. 299–301, Feb. 1994.

[28] J. W. Goodman and F. J. Leonberger, "Optical interconnection for VLSI systems," in *Proc. IEEE*, S.-Y. Kung and R. A. Athale, Eds., 1984, vol. 72, pp. 850–866.

[29] L. A. Hornak and S. K. Tewksbury, "On the feasibility of through-wafer optical interconnects for hybrid wafer-scale-integrated architectures," *IEEE Trans. Electron. Devices*, vol. 34, pp. 1557–1563, July 1987.

[30] A. D. Norte, A. E. Willner, W. Shieh, and A. R. Tanguay, "Multiple-layer optical interconnections using through-wafer hollow-dielectric-waveguide vias," *IEEE Photon. Technol. Lett.*, vol. 6, pp. 851–854, July 1994.

[31] J. Yoo, J. E. Leight, G. Giaretta, W. Yuen, A. E. Willner, and C. J. Chang-Hasnain, "Experimental demonstration of a four-plane 2-D multiple-wavelength optical interconnection using integrated VCSEL arrays and MQW/DBR detectors," *IEEE Photon. Technol. Lett.*, vol. 9, pp. 1646–1648, Dec. 1996.

[32] N. M. Jokerst, C. Camperi-Ginestet, B. Buchanan, S. Wilkinson, and M. A. Brooke, "Communication through stacked Si circuitry using integrated thin-film InP-based emitters and detectors," *IEEE Photon. Technol. Lett.*, vol. 7, pp. 1028–1030, Sept. 1995.

[33] J. Geist, A. Migdall, and H. P. Baltes, "Analytic representation of the Si absorption coefficient in the indirect transition region," *Appl. Opt.*, vol. 27, no. 18, pp. 3777–3779, 1988.

[34] K. H. Calhoun, C. Camperi-Ginestet, and N. M. Jokerst, "Vertical optical communication through stacked silicon wafers using hybrid monolithic thin-film InGaAsP emitters and detectors," *IEEE Photon. Technol. Lett.*, vol. 5, pp. 254–257, Feb. 1993.

[35] N. M. Jokerst, C. Camperi-Ginestet, B. Buchanan, S. Wilkinson, and M. A. Brooke, "Communication through stacked Si circuitry using integrated thin-film InP-based emitters and detectors," *IEEE Photon. Technol. Lett.*, vol. 7, pp. 1028–1030, Sept. 1995.

[36] O. Vendier, S. W. Bond, M. Lee, S. Jung, M. Brooke, N. M. Jokerst, and R. P. Leavitt, "Stacked silicon CMOS circuits with a 40 Mb/s through-silicon optical interconnect," *IEEE Photon. Technol. Lett.*, vol. 10, pp. 606–608, Apr. 1998.

[37] S. Bond, O. Vendier, M. Lee, S. Jung, A. Lopez-Lagunas, S. Chai, G. Dagnall, M. Brooke, N. Jokerst, D. S. Wills, and A. Brown, "A three layer 3D silicon system using through-Si vertical optical interconnections and Si CMOS hybrid building blocks," *IEEE J. Special Topics Quantum Electron. Smart Photonics Issue*, Mar. 1999.

[38] P. May, M. Lee, S. Wilkinson, O. Vendier, Z. Ho, S. Bond, D. Wills, M. Brooke, N. Jokerst, and A. Brown, "Design issues for through-wafer optoelectronic multicomputer interconnects," *IEEE J. Parallel and Distributed Computing, Special Issue on Parallel Computing with Optical Interconnects*, vol. 41, p. 3019, Feb. 1997.

[39] H. H. Cat, D. S. Wills, M. Brooke, and N. M. Jokerst, "A parallel processor with optical interconnect," in *Proc. Second Int. Conf. Massively Parallel Processing Using Optical Interconnections (MPPOI)*, Kaui, HI, June 1996.

[40] S. M. Chai, A. Lopez-Lagunas, D. S. Wills, N. M. Jokerst, and M. A. Brooke, "Systolic processing architectures using optoelectronic interconnects," in *Proc. Fourth Int. Conf. Massively Parallel Processing Using Optical Interconnections*, Montreal, Canada, June 1997, pp. 160–166.

[41] W. H. Robinson, D. S. Wills, M. A. Brooke, and M. N. Jokerst, "IRIS: An integrated, scalable focal plane architecture," in *Proc. 1998 11th Annual Meeting IEEE Lasers and Electro-Optics Soc., LEOS*, Orlando, FL, Dec. 1–4, 1998, Part 2 (of 2), pp. 184–185.

[42] O. Vendier, N. M. Jokerst, and R. Leavitt, "High efficiency inverted GaAs-based MSM photodetectors," *Electron. Lett.*, vol. 32, no. 4, pp. 394–395, Feb. 1996.

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