

Packaging Consideration for 1 Gbps Si CMOS Optical Driver

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Recently, attention has been given to using optical interconnection as a solution for overcoming the restrictions of electrical interconnections [1]. These restrictions arise increasing data rates and high density circuits. In optical interconnection systems, a laser driver is one of the key components needed to generate the high current, high speed pulses required for driving a transmitter.

To date, silicon (Si) CMOS drivers for bit rates up to several gigabits per second for low cost, low power consumption implementations have been reported [2]. However, the parasites of the packaging have not been considered in the design of these laser drivers, although they are bonded into a package. In the presence of parasites, the output of drivers can be corrupted. Thus, decoupling capacitors are needed near the power supplies to reduce the distortion due to the parasites. In this paper, a 1 Gbit/s laser driver is presented and the effect of parasites is discussed.

The CMOS driver circuit described herein was designed for operation at 1 Gbit/s. The driver consists of current mirrors and a current switch, as illustrated in Figure 1. A differential design was employed to reduce power supply ripples. The output

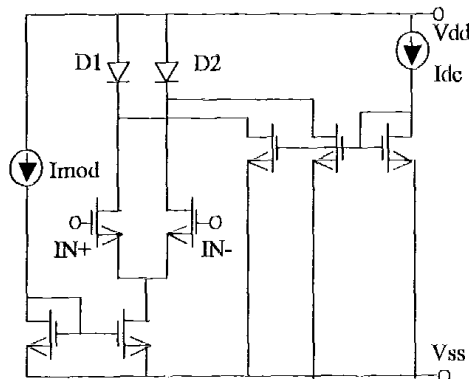


Fig. 1. Schematic of laser driver

current delivered to the laser diode was composed of I_{dc} for dc biasing the laser above the threshold current, and I_{mod} for the modulation current above threshold. In an integrated implementation, one of the diodes would be removed and a laser would be integrated instead of the diode.

The size of the transistors were optimized so that a 180 mA peak-to-peak modulation current and up to 30 mA of laser biasing current could be used. This driver was fabricated using standard 0.25 μm Si CMOS technology through the MOSIS foundry.

When a driver switches state from low-to-high and high-to-low, the output signal of the driver is degraded, since a sudden current ripple is produced. This current ripple appears in the interconnections to the power supply due to the parasitic inductance of the interconnections. A model of these packaging parasites is shown in Figure 2.

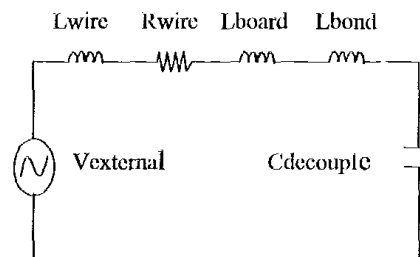


Fig. 2. A packaging parasites model

In Figure 2, L_{wire} and R_{wire} are the inductance and the resistance of wires from the external power supply to the internal power supplies (V_{dd} and V_{ss}) of the chip. L_{board} is the inductance of PCB (Printed Circuit Board), and L_{bond} is the inductance of the bonding wire. Due to these packaging parasites, decoupling capacitors are required for the reduction of switching. Thus, $C_{decouple}$ should be placed near the internal power

supply to provide charge during switching. The packaging model shown in Figure 2 was incorporated into the design of the driver circuit, and the circuit and packaging parasitics were simulated using HSPICE.

The performance of the driver and the packaging parasitics has been simulated. Pseudorandom input data at 1 Gbit/s with 1 volt peak-to-peak was used. First, the output data without parasitics is shown in Figure 3. This is the ideal situation, which is the goal of the properly decoupled packaged laser driver.

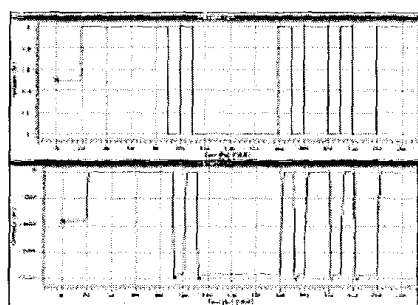


Fig. 3. Top: input signal; Bottom: output signal without parasitics

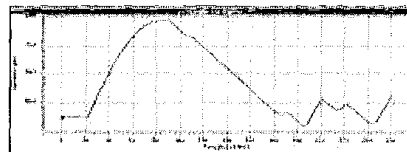
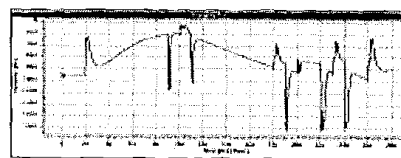


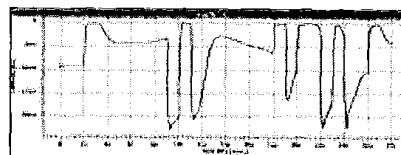
Fig. 4. Output signal with parasitics

Next, the output signal was corrupted by the packaging parasitics (as modeled in Figure 2), using typical values of 1nH for L_{bond}, 10nH for L_{board}, 185nH for L_{wire}, and 0.01 W for R_{wire}. The output result is shown in Figure 4. To reduce the effect of these packaging parasitics, various capacitance values were used to examine the effect of decoupling capacitors. These results are shown in Figure 5, indicate that larger capacitance values significantly improve the output signal. The minimum capacitance for a clear output waveform was 7 nF in this design, as shown in Figure 5c. Given this value, an on-chip capacitor can be embedded in the laser driver chip design. The fabricated laser driver with the on-chip capacitor is shown in the photomicrograph in Figure 6.

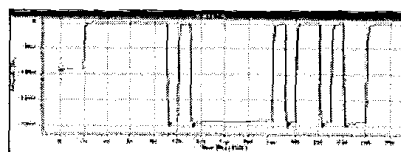
A high speed laser driver circuit has been designed and fabricated with an on-chip decoupling capacitor to prevent output distortion from packaging



(a) 10 pF capacitance



(b) 1 nF capacitance



(c) 7 nF capacitance

Fig. 5. Output signal with various capacitances

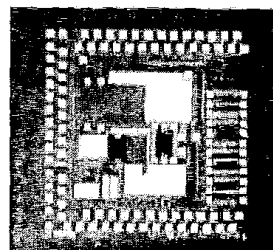


Fig. 6. Laser driver chip photograph.

parasitics. The suitability of a decoupling capacitor with a minimum capacitance of 7 nF was verified. In the near future, a laser will be integrated onto this driver chip for experimental verification of the design.

References

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