A Modulator Design for Smart Pixel Multispectral Imaging Arrays

Y. Joo, K. Lee, S. Seo, N. Jokerst, M. Brooke
School of Electrical and Computer Engineering
Georgia Institute of Technology, Atlanta, GA 30332-0250
Phone : 404-894-5250, Fax : 404-894-0222

Multispectral imagers have been heavily investigated for their application to target recognition, industrial gas pollutant monitoring, and biomedical imaging [1-3]. Direct conversion of pixel current to digital data using oversampling and a noise shaping modulator circuit enables advanced digital signal processing to reduce noise and enhance image quality [4]. This may be an important technology for noisy imaging detectors such as infrared or experimental UV detectors. However, when more than one detector is used with the modulator circuitry, as in multispectral imaging systems, frames rates drop dramatically. Using one modulator circuit per detector maximizes the frame rate possible and further reduces noise by eliminating analog signal distribution lines. We describe the design and simulation of a 0.25 micron CMOS modulator small enough to allow multiple modulators to reside beneath each pixel of an experimental multi-detector multi-spectral imager.

One implementation envisioned for a smart multispectral imager realizes the full registration of multicolor images through the integration of multiple thin film stacked co-located detectors onto Si CMOS analog to digital modulator circuitry, as illustrated (not to scale) in Figure 1. Foundry digital Si CMOS arrays of oversampling modulators, shown in a photomicrograph in Figure 2, serve as the integration host substrate for the thin film detector arrays. The Si CMOS modulators consist of two dedicated modulators per image pixel, and the circuits have been optimized for low noise transfer of data off of the focal plane, using per pixel digitization and filtering methods which can also be used to trade off frame rate and resolution. The GaN UV MSM and MCT MWIR pn photodetectors are independently grown and optimized, and are designed for thin film processing, integration, and stacking using metal/metal bonding [5].

The integration of image processing circuitry under the multispectral imaging detector arrays, or the realization of a "smart" multispectral imaging array, is an area of research under intense study. Through preprocessing of the raw image signal using on-focal-plane integrated circuitry, the fundamental bottleneck for large scale arrays, namely, the data transfer performance limitation of the imaging system, can be addressed. Conventional imaging systems use X-Y readout of the sensor array data followed by transportation of the data to an off-chip serial analog-to-digital converter (ADC). However, a parallel readout system is the best choice to accommodate ever-increasing data rates for off-chip data transfer [6]. This option performs the A/D conversion as early as possible in a signal chain to avoid processing and transportation of analog signals to minimize noise. The per pixel A/D conversion is the extreme of this solution, namely, association of one ADC with each pixel. The advantages to this approach are that no signal degradation occurs when digital data is read out of the detector array, and the incident signal on the detector can be sensed and electrically processed during the entire frame period.

In this application, a per pixel oversampling ADC is designed. The major difference between per pixel ADCs and a single-chip ADC is that, unlike the latter, a per pixel ADC must occupy a relatively small chip area. Oversampling ADCs show good robustness for component mismatch while their modulator components occupy a small chip area [6]. Oversampling converters trade speed for accuracy. Oversampling converters allow simple, compact digitizing units or modulators to be built, that, with DSP, achieve significant lower noise operation than other converters operating at the same effective original sampling rate.

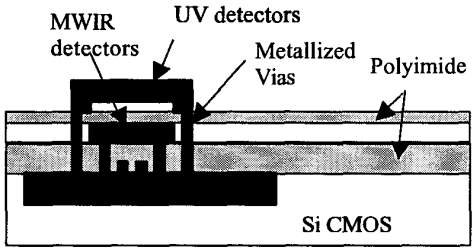

Figure 1. Schematic of integrated multispectral imaging array using 3D stacked detectors.

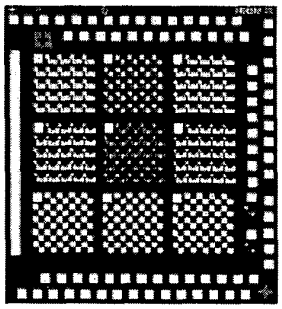

Figure 2. Photomicrograph of Si CMOS modulator circuits fabricated through the MOSIS foundry.

Oversampling ADCs consist of two major parts: the modulator, which samples analog input and develops a corresponding digital bit stream, and the digital signal processor, which compresses the bit stream into the Nyquist rate multi-bit codes and performs noise filtering. Only the modulator needs to be on the imaging array plane, which reduces the development problem of fitting the ADC into the allocated space. Therefore, the oversampling ADC is a promising approach for integration with an imaging array. By using an oversampling method, in-band noise can be reduced. In fact, the fixed pattern noise of the detector, threshold offset, and nonlinear gain are equivalent to DC (extremely low frequency content) noise and go to zero when they are differentiated [7]. Furthermore, white noise and *1/f* noise are attenuated by the oversampling technique.

Figure 3 shows a simplified block diagram of a current input oversampling modulator. The first stage is a current buffer that provides a low input impedance and stable bias to the detector. An integrator is realized us ing a floating capacitor because the integration value was current. The capacitor size is limited by the pixel size, maximum speed, and resolution of the imaging array system. The digital-to-analog (D/A) converter (DAC) is designed using a current mirror circuit with a feedback switch that is controlled by the output value. The DAC injects current pulses into the integrating capacitor and the terminal of this capacitor is the node where the system feedback loop is closed. A comparator is used for the quantization of the integrator output. Figure 4 shows a layout of the modulator circuits in 0.25 micron CMOS for the multispectral imaging system. The pixel pitch is 100 microns, there are 2 modulators per cell, with independent biasing and addressing for each o f two detectors in each cell, and the array size is 5x5. Figure 5 shows HSPICE simulation results with a 100Hz, 0.3 nA sinusoidal current input for each detector. Figure 5b shows the integrator voltage and Figure 5c shows the expected 1-bit output stream, thus demonstrating a functional multispectral smart pixel circuit design. Testing results of the multispectral imaging array circuit will be discussed in the presentation.

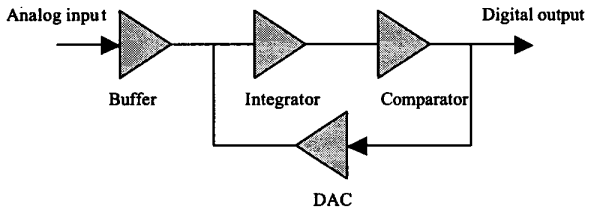

Figure 3. Oversampling modulator block diagram.

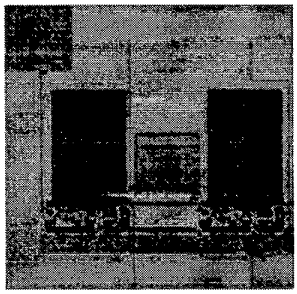

Figure 4. Layout of the pixels.
There are two modulators per pixel.

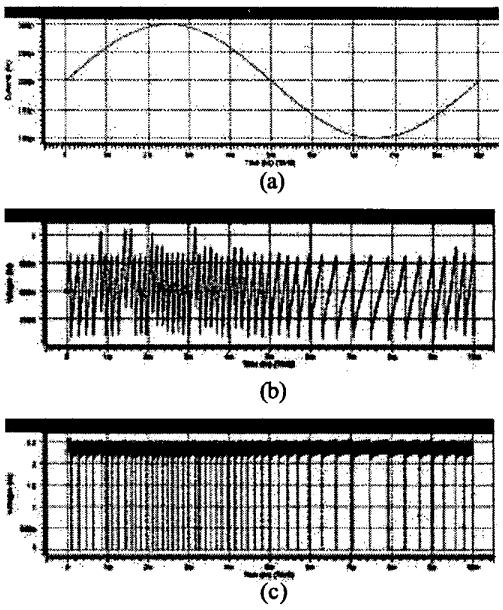

Figure 5. Simulation results: a) is the detector current, b) is the analog modulator voltage and, c) is the resulting digital output.

[1] L. Hoff, J. Zeider, C. Yerkes, *SPIE Signal and Data Processing of Small Targets* , vol. 1698, pp. 100-114, 1992.
[2] L.E. Hoff, J.R. Evans, and L.E. Bunney, *NOSC TR 1404*, Dec. 1990.
[3] F. Lopez, J. deFrutos, A. Gonzalez, A. Navarro, *Sensors and Actuators B*, vol. 6, pp. 170-175, 1992.
[4] J. C. Candy, G. C. Temes, *Proceedings - IEEE International Symposium on Circuits and Systems* , vol 2. pp. 910-913, 1990.
[5] K. Lee, S. Seo, S. Huang, Y. Joo, *IEEE/LEOS Summer Topical Meeting* , W1.1, 2000.
[6] Y. Joo, J. Park, M. Thomas, K. Chung, *IEEE Journal of Selected Topics in Quantum Electronics* , vol. 5, no. 2, pp.296-305, 1999.
[7] W. Mandl, Proceedings of SPIE - The International Society for Optical Engineering, vol. 2474, pp. 63 -71, 1995.