Design of a Smart Pixel Multispectral Imaging Array Using 3D Stacked Thin Film Detectors on Si CMOS Circuits

K. Lee, S. Seo, S. Huang, Y. Joo, William A. Doolittle, S. Fike, N. Jokerst, M. Brooke, A.Brown
School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332-0250
J.E. Jensen, T.J. de Lyon HRL Laboratories, 3011 Malibu Canyon Rd., Malibu, CA 90265-4799

Multispectral imagers have been widely investigated for their application to target recognition, particularly in clutter [1,2], industrial gas pollutant monitoring [3], and biomedical imaging [4]. For example, target recognition is a difficult task with passive detection of small targets embedded in infrared image data. This difficulty arises because in most cases the target exhibits only slight variation in temperature from the background clutter. When image data at multiple wavelengths is collected, the data can be processed to cancel the background clutter and improve the detectability of targets [1,2]. Many methods have been used to realize multispectral imaging, however, each has some significant difficulties [3,4] which can be resolved by using co-located detectors stacked in 3D on top of image processing circuitry [5,6,7].

Information processing using digital Si CMOS circuits is currently ubiquitous due to the increasing level of complexity of information processing demands and capabilities. Leveraging the high level of Si signal processing complexity by creating "smart" systems that use Si circuitry with enhanced added functions is an attractive system option. The most effective value-added components to add to Si CMOS are those that can be independently optimized, compromising neither the performance of the value-added devices nor the Si CMOS circuits. Herein, we discuss the design of a "smart" multispectral imaging system which can be fabricated with independently optimized detector arrays and Si CMOS circuits, which are stacked in three dimensions on top of one another for complete physical registration of the multispectral image. This smart multispectral imager, described herein, utilizes the heterogeneous integration of thin film GaN (UV), MCT (MWIR), and Si CMOS circuitry to create an outstanding example of the power of heterogeneous integration for enhancing optical systems using electronic signal processing capabilities.

The smart multispectral imager realizes the full registration of multicolor images through the integration of multiple stacked co-located detectors onto Si CMOS analog to digital converter (ADC) circuitry, as illustrated (not to scale) in Figure 1. A foundry digital Si CMOS array of sigma delta ADCs, shown in a photomicrograph in Figure 2, serves as the integration host substrate. These Si CMOS ADCs consist of one dedicated converter per image pixel, and the circuits have been optimized for low noise transfer of data off of the focal plane, using per pixel digitization and filtering methods which can also be used to trade off frame rate and resolution. The GaN UV MSM and MCT MWIR pn photodetectors are independently grown and optimized, and are designed for thin film processing, integration, and stacking using metal/metal bonding. This process is illustrated in Figure 3.

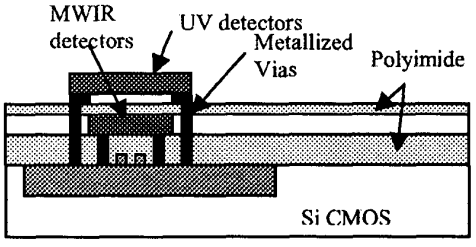


Figure 1. Schematic of integrated multispectral imaging array using 3D stacked detectors.

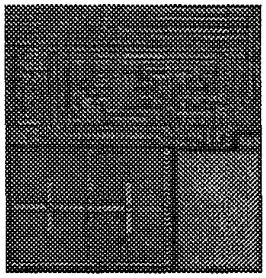


Figure 2. Photomicrograph of Si CMOS ADC circuit fabricated through MOSIS.

0-7803-6252-7/00/$10.00©2000 IEEE

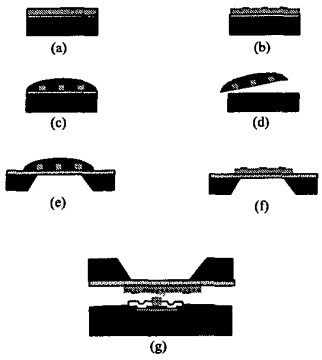
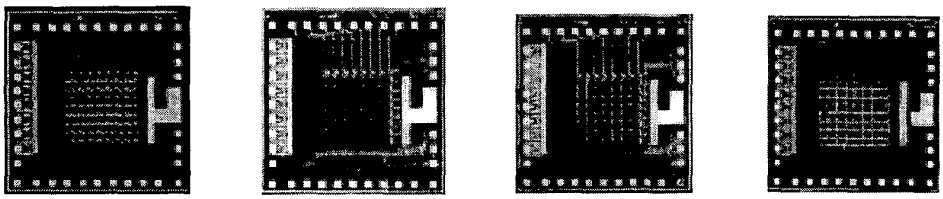


Figure 3. Thin film integration process.

In this integration process, a stop etch layer is grown lattice matched between the detector epilayers and the growth substrate (a). This stop etch layer can be removed, and does not degrade device performance. The devices are mesa etched for pixellization (a partial mesa etch for arrays, to maintain spatial registration during subsequent bonding processes) (b), and the devices are protected from the substrate removal etchant by a handling layer such as Apeizon W (c). The substrate is removed using a wet etch which selectively etches the substrate and not the stop etch layer (d), and the stop etch layer, with another etchant, can then be removed if necessary. The devices are then bonded to a transfer diaphragm (e, f), and are aligned and bonded to the host substrate (g) [5,6].

To realize these thin film photodetectors, the MCT MWIR pn detectors are grown on SOI, and the GaN UV photodetectors are grown on lithium gallate. These structures enable the selective chemical removal of the growth substrate, as illustrated in Figure 3, with details in the presentation. To integrate the Si CMOS host substrate circuit, it is planarized and isolated with polyimide, cured, vias are cut to the Si CMOS contact pads using a reactive ion etcher (RIE), and the vias are metallized for contact to the MCT (bottom layer) photodetectors. Note that the original top metallization of the photodetectors is inverted in the transfer process, and the devices are thus metal/metal bonded to the Si CMOS circuit, resulting in an excellent mechanical and electrical bond. As an example of this type of thin film detector array integration, Figure 4 is a photomicrograph of an 8x8 array of thin film GaAs P-i-N detectors bonded directly on top of Si CMOS circuits [7].



(a) (b) (c) (d)

Figure 4. Photomicrographs of 8x8 integrated array: (a) Si CMOS circuit; (b) thin film P-i-N detectors bonded to planarized/via cut/metallized circuit; (c) interstitial layer removed; (d) planarization/isolation, top via, and top metal contact completed.

Since the MCT MWIR detectors are only microns thick, they can be planarized with polyimide or BCB with subsequent top contact metallization (which can be utilized as a shared contact with the GaN). To fully separate the MCT and GaN contacts, the MCT top contacts can be isolated with polyimide and the top MSM contact metallization for the GaN UV photodetector array deposited. Next, the GaN thin film MSM detectors are bonded, with contacts facing down to the metallized MCT array, thus completing the imaging array. Processing details and projected performance of the integrated multispectral imaging array will be discussed in the presentation.

The authors would like to thank the Office of Naval Research for support of this work through the grant N00014-99-1-0974.

[1] L. Hoff, J. Zeider, C. Yerkes, *SPIE Signal and Data Processing of Small Targets*, vol. 1698, pp. 100-114, 1992.
[2] L.E. Hoff, J.R. Evans, and L.E. Bunney, *NOSC TR 1404*, Dec. 1990.
[3] F. Lopez, J. deFrutos, A. Gonzalez, A. Navarro, *Sensors and Actuators B*, vol. 6, pp. 170-175, 1992.
[4] R. Williams, J. Sanders, R. Driggers, C. Halford, *Proceedings. IEEE Southeastcon '92*, vol. 1, pp. 291-294, April 1992.
[5] C. Camperi-Ginestet, M. Hargis, N. Jokerst, M. Allen, *IEEE Phot. Tech. Lett*, Vol.3, No.12, pp.1123-1126, Dec., 1991.
[6] N. Jokerst, M. Brooke, O. Vendier, S. Wilkinson, S. Fike, M. Lee, E. Twyford, J. Cross, B. Buchanan, S. Wills, *IEEE Trans. On Comp., Pack., and Manfuac. Tech., Part B*, Vol.19, No.1, Feb.1996, □□□□□.
[7] S. Fike, B. Buchanan, N. M. Jokerst, M. Brooke, T. Morris, S. DeWeerth, *IEEE Phot. Tech. Lett*, Vol.7, No.10, pp.1168-1170, Oct. 1995.