Enhanced Imaging Arrays Using a Sigma Delta ADC in Si CMOS for Each Array Pixel

Martin A. Brooke
School of Electrical and Computer Engineering
Georgia Institute of Technology
Atlanta, Georgia 30332

Abstract

Recently we have demonstrated a compact current input oversampling modulator for a scalable high frame rate focal plane arrays [1] that enable frame rates over than 100kfps operating in continuous imaging mode. All the circuits including data lines and detectors were laid-out to fit into 125umX125um space using 0.8um CMOS technology. This compact converter also provides improvement in noise filtering performance over imagers that use capacitance at each pixel to convert detector current to voltage. This technique may allow noisy detectors to be used at high temperatures with good image quality.

1. Introduction

Current imaging systems implemented using charge-coupled device (CCD) technology with off-chip analog-to-digital data converters are limited in the amount of detector noise they can filter this causes problems with noise at high frame rates [2] or with noisy detectors (e.g. IR detectors) Focal-plane-array (FPA) technology [3] can reduce the noise added to the detector noise at each pixel by eliminating long analog signal paths, however if a capacitor is used to convert detector current to voltage, or a charge packet, at each pixel, this capacitor "samples" the noise in the detector before each readout permanently embedding it with the signal.

Recently to overcome the speed limitations of the conventional readout systems, we have developed fully parallel readout systems which need a compact ADC for each pixel [4][5]. Due to the small Si area available, a compact ADC with high speed and large dynamic range is necessary. A current input oversampling modulator was found to be a very compact candidate for this imaging application because it is immune to component mismatch, and through subsequent digital filtering of the output signals, a tradeoff between dynamic range and frame rate can be achieved. In addition, the digital filtering can remove high frequency noise from the image data, resulting in an improved signal to noise ratio for the ADC-based system.

2. Current input oversampling modulator

Modern short-channel CMOS processes offer a speed performance which far exceeds the requirements of most imaging systems. Since shorter channel lengths will be available in the future, this speed advantage will be further improved; however, accuracy and component matching are expected to become worse. It could be a serious problem for the fully parallel FPA readout system because there are thousands of ADCs working simultaneously, and needing good uniformity to get a good image. Hence, it is desirable to trade off speed for accuracy, and obtain accuracy advantages at the cost of speed reductions in the focal-plane-array ADCs. One of the ADC's which trade off speed for accuracy is oversampling ADC which is designed in this paper

3.1 Circuit and simulation results

Figure 1 shows the schematic of the combined modulator circuits. The output of the current buffer is connected to the D/A converter and integrator. The current integrator is implemented with a capacitor. The last stage is a comparator, which compares the integrator voltage and reference voltage then makes a one bit output data stream [6]. The comparator output is also fed back to the DAC to control the feedback current which makes the comparator output average track the input value.

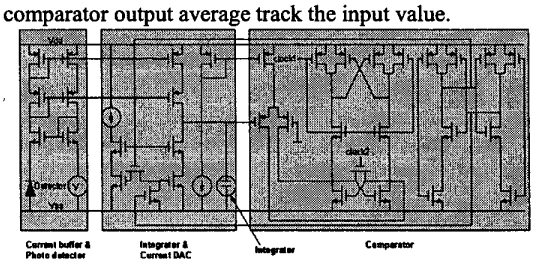

Figure 1. Current input oversampling modulator

Figure 2 shows SPICE simulation results with 50kHz 2uA sinusoidal input. Figure 2(a) shows the integrator voltage variation and the modulator output. The power density function (PDF) of the output code is shown in Figure 2(b). Since this spectrum is of a digital 1 bit

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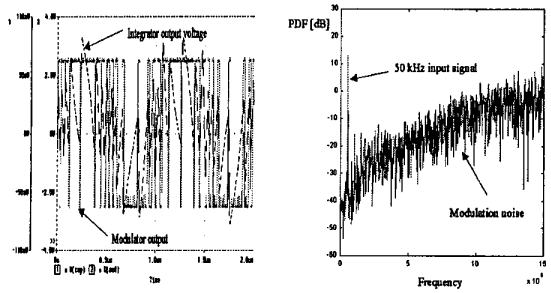
signal, the plot of the PDF shows that most of the digitization noise has been shifted to frequencies higher than the signal frequency. This will occur provided that the ADC operating frequency is much higher than the signal frequency (oversampling). Thus we can digitized the detector current, and almost arbitrarily reduce the amount of noise added in the digitization process by oversampling at higher and higher rates and then filtering out the high frequency noise with a DSP process (such as the FFT used to obtain Figure 2(b)).

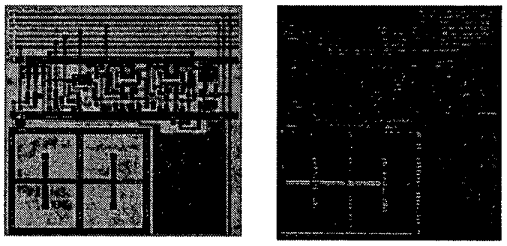


(a) Time domain (b) Frequency domain

Figure 2. Simulation results

3.3 Fabrication and Test Results

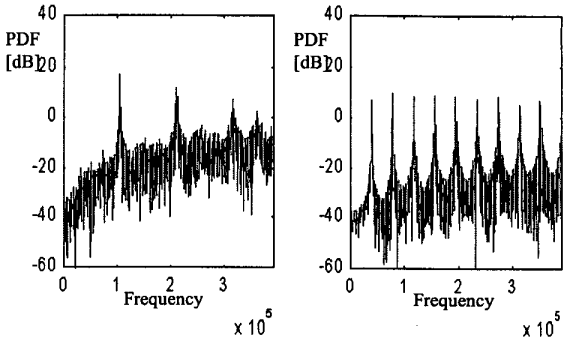
Figure 3 shows a layout and photomicrograph of the modulator circuits for FPA pixels. An 8x8 focal-plane-array system was tested using a 100 MHz system clock which means each pixel operates at 1.56MHz.



(a) Layout (b) Photomicrograhp

Figure 3. Modulator Layout and photomicrograph

Figure 4(a) shows the frequency response of the system. The noise is modulated and the in-band noise is decreased. Figure 4(b) shows a purely simulated result from the Matlab for comparison.



(a) Test result (b) Simulation result

Figure 4. PDF responses of the modulator

There are many pattern noises in the ideal simulation which can be removed by adding a white noise. Test results have less pattern noise because there are many noise sources which dither the input signal [7]. From the simulation and test results, it is not possible to distinguish the system noise from the quantization noise. Which means at an oversampling ration of 4096 no noticeable noise is added by our hardware. Thus only detector noise in the signal band would remain after filtering.

6. References

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