Compact Current Input Oversampling Modulator Design for a Scalable High Frame Rate Focal Plane Arrays

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Abstract

This paper demonstrates a compact current input oversampling modulator for a scalable high frame rate focal plane arrays. This smart pixel architecture with the proposed compact current input oversampling modulator is intended for scientific imagers with frame rates around 100 kfps operating in continuous imaging mode. All the circuits including data lines and detectors fit into a 125 micron x 125 micron cell using 0.8 micron CMOS technology. Test results on a 8X8 demonstration focal-plane-array show operation at over 100 MHz sampling rate which represents a 60 kfps 8 bit per pixel image capture rate.

1. Introduction

High speed imaging applications such as combustion imaging [1],[2], transMach fluid flow imaging [3], and aerooptic imaging [4] require high frame rate image acquisition systems with frame rates in excess of 100 kfps (frames per second). Currently, imaging systems implemented using charge-coupled device (CCD) technology with off-chip analog-to-digital data converters are limited to continuous frame rates of approximately 1 kfps [5]. In focal-plane-array (FPA) technology using on image plane circuitry for image processing, large imaging arrays have been demonstrated [6]. However, the combination of high resolution with the large number of pixels has resulted in data rates that can not be transmitted off the FPA through a one port readout system. To overcome the limitation of the conventional readout systems, a parallel readout system was introduced [7, 8]. This system achieves it's highest frame rates when a compact ADC is used with each pixel. Due to the small Si area available, a compact ADC with high speed and large dynamic range is necessary. Other advantages of pixelwise A/D conversion are that it performs the A/D conversion as early as possible in a signal chain, and avoids processing and transportation of analog signals, both of which help reduce added noise.

A current input oversampling modulator has been designed to meet these needs and implemented in a small demonstrated system. A oversampling modulator is a good candidate for this imaging application because it is immune to component mismatch, and through subsequent digital filtering of the output signals, a tradeoff between dynamic range and frame rate can be achieved. In addition, the digital filtering can remove high frequency noise from the image data, resulting in an improved signal to noise ratio.

2. Architecture of focal plane readout system

To achieve image processing systems that operate in real time, and on large images with frame rates in the high kHz or MHz, is beyond the capability of today's imaging systems. For example, a first-order sigma-delta analog-to-digital converter (ADC) converting 500x500 8 bit images at a frame rate of 100 kHz must be clocked at more than 655 GHz. Even when parallel ADC's are placed along the edge of the imaging array, the problem is only partially mitigated because the speed at which the ADC's must operate still increases with image size. To generate 500x500 8 bit images at a frame rate of 100 kHz, 500 ADC's need to be clocked at more than 1.31 GHz.

To overcome the serial and semi-parallel readout limitations, a focal-plane-array (FPA) is implemented using a fully parallel readout architecture. The fully parallel readout system is designed so that the pixels can be grouped into sub-arrays; whereby, each is served by one digital signal processing (DSP) unit to perform the conversion. Each pixel has its own ADC. To keep the area of the ADC circuitry small, a current input oversampling ADC is chosen. This type ADC is chosen because only the front end of the oversampling A/D converter need be implemented, on a per pixel basis. Since oversampling converters process only digital data after the front end, further noise, by shifting the digital data, can not be introduced to the signal. An integrated optoelectronic emitter on each sub-array allows through-silicon wafer output of digital image data from the focal plane to the processor stacked below each sub-arrays as

shown in Figure 1. This vertical coupling to the image plane allows the detector and processor arrays to be scaled while maintaining a fixed level of processing per pixel. Therefore, the processing rate does not depend on the array size anymore, consequently the readout system is scalable. The number of pixels included in the sub-array depends on the bandwidth of the DSP circuits. An example of the proposed processor is the SimPil processor [9]. If an 8x8 sub-array is used, the size of the processor and focal plane sub-array seem to match reasonably well. A 256×256 pixel 8 bits resolution focal plane could be achieved by a tiling 8x8 array processor working at 168 MHz.
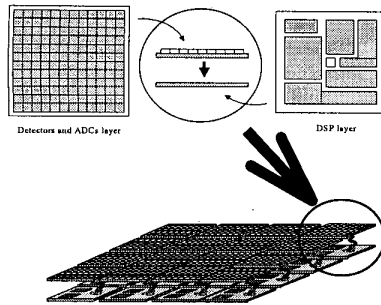

Detectors and ADCs layer   DSP layer

Figure 1. A stacked two layer focal plane system

3. The current input oversampling modulator

Modern short-channel CMOS processes offer a speed performance which far exceeds the requirements of the proposed system. Since shorter channel lengths will be available in the future, speed will be further improved; however, accuracy and component matching are expected to become worse. It could be a serious problem for the fully parallel FPA readout system because there are thousands of ADC's working simultaneously, and needing good uniformity to get a good image. Hence, it will be interesting to trade off speed for accuracy, and obtain some accuracy advantages at the cost of a speed limitation for the focal-plane-array ADC's. One of the ADC's which trade off speed for accuracy is oversampling ADC which is designed in this paper

3.1 Design features

There are several design features used to build a current input oversampling A/D modulator. The first design feature is to improve the oversampling loop linearity. Since a feedback structure reduce the effects of the nonlinearities of the elements following the gain block in its forward path, the architecture maximize the linearity of the entire system by putting most circuit elements inside the forward path of the feedback loop. The main function of the loop is to shape the quantization noise;

whereas, only the input stage is outside of the loop. The second design feature is that the amplifiers are removed from the feedback. Operational amplifiers are not required in the system, so the difficult problems of providing frequency compensation and reducing the settling time are avoided. The third design feature is that a linear D/A conversion is available; whereby, a single bit D/A converter has ideal linearity. In practice, however, when the D/A converter switch from one state to another, spikes are generated in its output waveform. The fourth design feature is that the modulator is working under continuous-time. The oversampling modulator is not realized as a switched capacitor (SC) network, so the problems associate with SC circuits, such as clock feedthrough and digital noise, are avoided.

3.2 Circuit configurations and simulation results

Figure 2 shows the schematic of the combined modulator circuits. The output of the current buffer is connected to the D/A converter and integrator. The detector bias is controlled by the V that is connected commonly with other pixels. The current source is also connected commonly with other pixels on the outside of the focal plane to save space and power. The current integrator is implemented with a capacitor whose value is determined by the input current size, readout speed, and noise. The last stage is a comparator, which compares the integrator voltage and reference voltage then makes a one bit output data stream [10]. The digital output of the comparator would be decimated and filtered by the filters that are programmed in the following DSP chip. The comparator output is also feedback to the DAC to control the feedback current which makes the comparator output average track the input value.

Figure 3 shows SPICE simulation results with 50kHz 2uA sinusoidal input, and is oversampled by 32. Figure 3(a) shows the integrator voltage variation and the modulator output. The power density function (PDF) of the output code is shown in Figure 3(b). It shows the well known oversampling properties, the noise is increased with high frequency area and decreased with low frequency area. The out-of-the modulator signal is decimated and low pass filtered to secure the binary code.
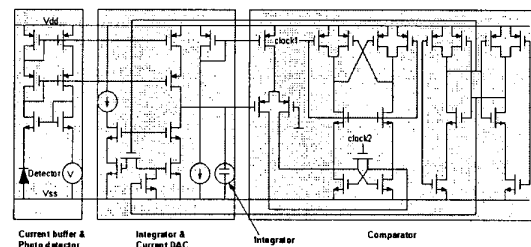

Current buffer &   Integrator &   Comparator
Photo detector   Current DAC   Integrator

Figure 2. Current input oversampling modulator

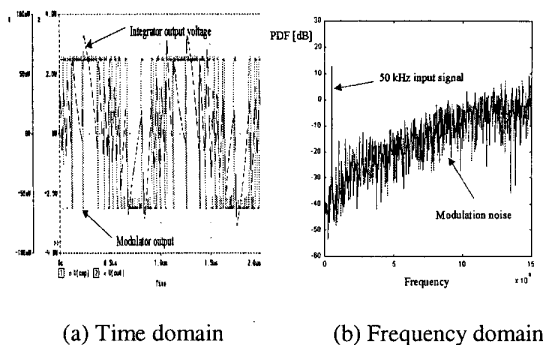(a) Time domain (b) Frequency domain

Figure 3. Simulation results

3.3 Layout

Figure 4 shows a layout and photomicrograph of the modulator circuits for FPA pixels. All the circuits including data lines and detector are laid-out to fit into 125umX125um space using 0.8um technology. To make a large detector, all efforts are applied to design a compact circuit. Input parts of the circuits are carefully designed not to overlapped with digital data lines. To reduce the offset and improve the switching time of the comparator, all the components are carefully laid-out to make a matched comparator. For the capacitor layout, metal 1 and metal 3 layers are connected to the GND to prevent the metal-substrate capacitor. The latch transistor size is optimized to drive a high capacitor load which is connected to several pixels through a long data line. All surfaces except the detector area are covered by metal 3 to prevent unnecessary light induced current through the circuit area.
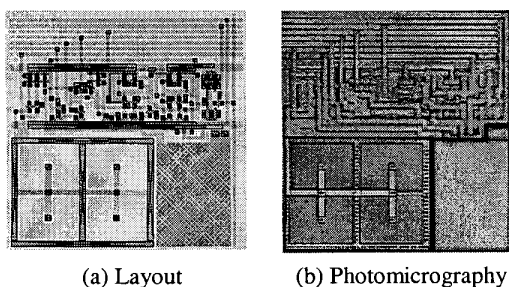

(a) Layout (b) Photomicrography

Figure 4. Modulator

4. Test Results

To achieve a 100kfps 8 bit image capture rate with the parallel readout system, 8X8 FPA's needs to operate with a 168MHz clock speed. In this case, each modulator under the pixel is operated at 2.6MHz to generate an 8 bit

image. This oversampling frequency is calculated from the oversampling ratio of 26 to get an 8 bit image.

For the first step of high speed testing, a single test pixel was tested at several different sampling rates with a constant illumination. Figure 5 (a) and (b) are the outputs of the modulator which using 2MHz and 4MHz sampling rates. There are some artifacts in the figures due to the use of a sampling oscilloscope (Tektronix 11403A) to measure the output. To get a 100kfps 8 bit image with an 8x8 FPAs required a modulator sampling rate of 2.6MHz. The maximum sampling with a varied output was 4MHz using this test environment. The actual FPA system has less load capacitance compared to the test structure. It also has a digital amplifier at the end of the column which promised a larger bandwidth.
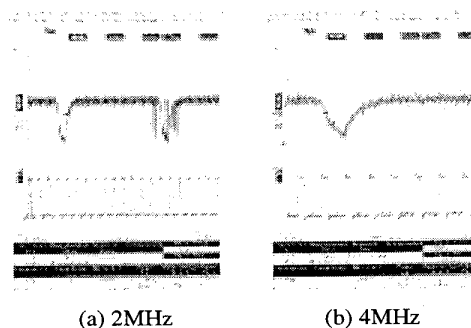

(a) 2MHz (b) 4MHz

Figure 5. Single test pixel test results

The 8x8 focal-plane-array system was tested using a 100MHz system clock frequency which meant each pixel was sampled at 1.56MHz. When the test frequency was higher than 100MHz, the non-overlapping clock signal failed and did not give a correct clock signals. Figure 6 shows the test results with different uniform light intensities. There are more 1's repeated with high light intensity.
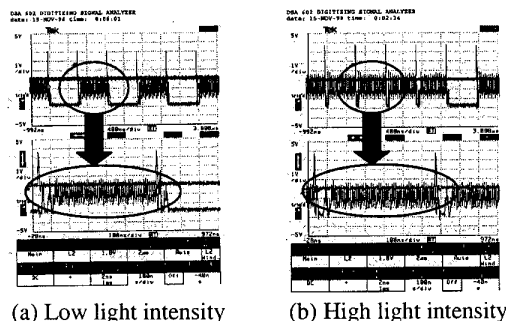

(a) Low light intensity (b) High light intensity

Figure 6. Whole system test results with 100MHz sampling rate

To estimate the noise added by the detectors and circuits we compared the test results with ideal Matlab simulation results. To do this the 100 MHz clock signal was generated by Data generator (DG2020A, Tektronix) and the output data from the test chip was read into the Logic analyzer (TLA704, Tektronix) for analysis. The maximum capacity of the logic analyzer is 262144 bits which means that for each of our 8x8 pixels we can store 4096 bits. After the data were acquired several times with several different light intensity, they were analyzed using a Matlab program. Figure 7 (a) shows the PDF of the test result. The noise is modulated and the in-band noise is decreased. Figure 7(b) shows the PDF of the ideal simulation result using Matlab program.

There are many pattern noises in the ideal simulation results which can be removed by adding white noise. Test results have less pattern noise because there are many noise sources which dither the input signal [11]. From the simulation and test results, we see that the system noise is almost indiscernible from the quantization noise at this oversampling ration. This indicates that the imager is performing very well from a noise stand point at this high frame rate.
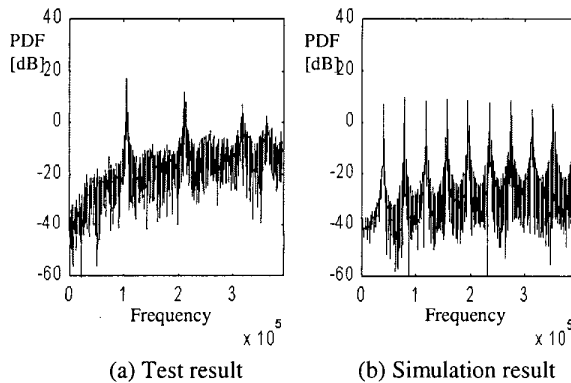

(a) Test result   (b) Simulation result

Figure 7. PDF responses of the modulator

5. Conclusion

In this paper, a new current input oversampling modulator for the scalable high frame rate FPAs was designed and tested. All the circuits including data lines and detectors were laid-out to fit into 125umX125um space using 0.8um technology. The 8x8 modulators with Si detectors was tested using a 100MHz sampling rates which is equal to 60kfps 8 bit per pixel image capture rate. The limitation of the highest testing results were not coming from the circuit but the test setup. The smart pixel architecture with the proposed compact current input oversampling modulator enables frame rates up to 100kfps operating in continuous imaging mode.

6. References

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