ISCAS 2000 - IEEE International Symposium on Circuits and Systems, May 28-31, 2000, Geneva, Switzerland

A Clock Extraction Circuit Using Passive Components-Free Filter in Standard Digital Process

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Abstract – **The necessity of passive components in analog circuit design such as Clock Recovery Circuits (CRC) or Phase Locked Loops (PLL) has been a main barrier to overcome especially when using a standard digital CMOS process. In addition to lack of support of high quality passives in digital CMOS, use of passive devices causes problems with area, thermal noise of resistance[1], process variation, mismatch of capacitances[2], and inability to scalable designs. Consequently current high speed clock recovery circuits are implemented mostly in bipolar technology or other passive friendly technology[3]. However, these technologies are not well-suited to the higher levels of integration needed for "systems on a chip". Also, current technology emphasis is shifting from increasing the operation speed of components to reducing their size, power consumption, and cost to eliminating the need for adjustment and trimming[4]. These goals can be achieved by using fully passive component-free monolithic CMOS circuits. In this paper, we present a method for implementing a passive component filter which can be used in clock recovery circuit or PLLs.**

I. Introduction

Recently, Fiber optic serial data communication networks are finding increased applications in traditional telecommunications, with the Synchronous Optical Network (SONET), and in Local Area Networks (LAN) such as Asynchronous Transfer Mode (ATM). This increased demand creates a need for small and easy-to-use fiber optic receivers[4]. Key elements of those receivers are the recovery of implicit clock signals embedded in the non-return-to-zero (NRZ) serial data stream, and the re-establishing of the synchronous timing data using the recovered clock as the reference. In most optical communication systems, the clock is not transmitted separately; therefore, it must be extracted directly from the input data stream[5]. The received signal in optical communication systems, which has been attenuated and degraded by noise and imperfections in the modulation and transmission process, must be reconstructed before further processing. To achieve this reconstruction, the signal is typically amplified, filtered, and sampled at a certain time in the bit slot where there is the lowest probability of error. The recovered clock plays an important role in determining this sampling timing.

Conventional method for clock recovery circuit is to use a high Q-filter (such as a SAW or tank filter)[3]. As shown in the figure below, the NRZ signal which has no clock frequency component goes through a nonlinear clock extraction circuit; whereby, creating a clock frequency which is selected in the following Band Pass Filter. Then, as the signal goes through a limiter (such as comparator or decision making circuit), the analog based data form is transformed into a digital format. Alternatively, a variable phase delay circuit can be used to establish and maintain the proper phase relationship between the data transitions and the filter output. This type of clock recovery circuit is known to have a low jitter performance but also have a drawback of large power dissipation.[6]

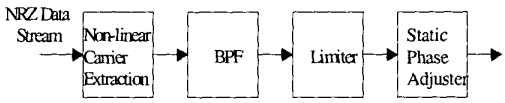

Figure 1: Typical Filter based Clock Recovery Circuit

II. Operational Function

The proposed filter design method does not utilize any passive components. Instead, it uses a delay line, and an analog summation circuit in an open loop. The open loop topology has simple and can be fully integrated because it

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doesn't contain any external or passive component[7]. First, since the incoming NRZ signal doesn't contain any components at frequencies that are integer multiple of recovering clock frequency. The received signal is sent to the delay circuit and the half bit delayed signal is applied to the XOR gate with original signal to have a clock frequency component[8]. This non-linear clock frequency addition circuit is shown in figure 5. To operate in a required speed range, the delay must be adjustable. Then, this doubled frequency signal goes through long series of delays which is mainly composed of multiple chain of inverters, then the outputs of each delay tap are summed or subtracted by summation circuit with an optimum choice of weight as shown in the Figure 2.

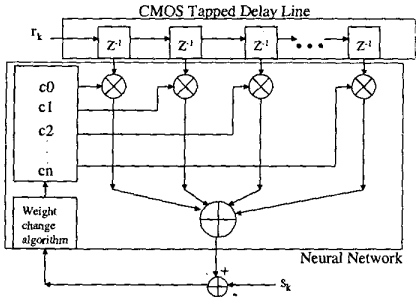

Figure 2: Proposed Method for Clock Extraction

To show the function of the filter, timing diagram is depicted in Figure 3. In this figure, unique weight to each tap for summation and subtraction has been applied, but it is possible to assign and adjust each weight as needed to recover any signal given enough taps and optimum choice of weights. The jitter existing in the numerical simulation was caused by the non-linearity of time.

It is known that one of hard tasks of clock recovery is to recover the clock when there is long consecutive identical signals, which means no data transition. In such a case, the length of filter should be longer than the normal length of consecutive identical signals. For example, in order to recover the clock from random data stream of 2^7-1, the length of delay in the tapped delay line must be longer than 8bits of signal to cover frequency band of incoming signal.

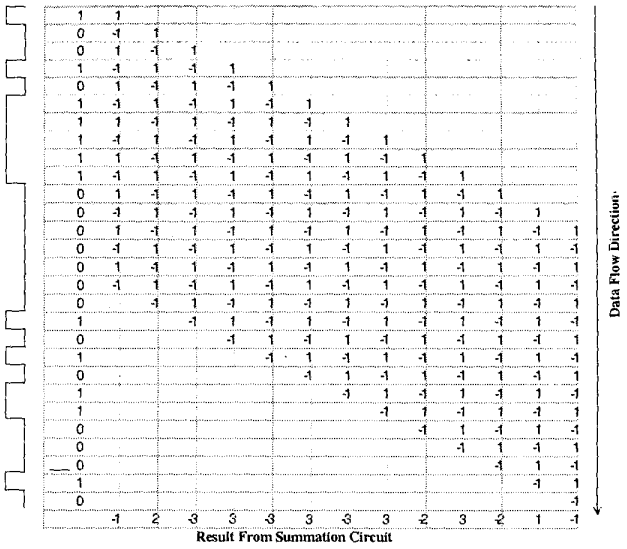

Figure 3: Timing diagram of filter and output

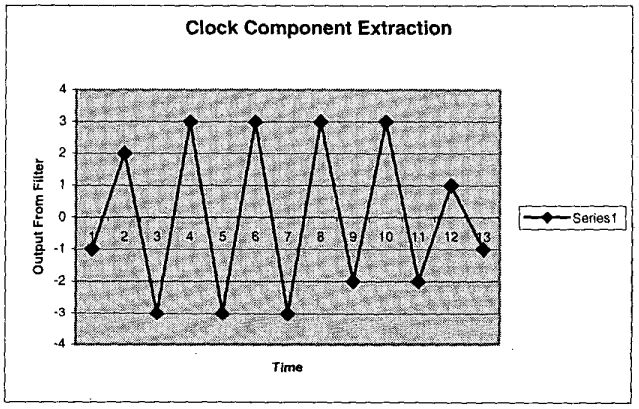

Figure 4: Simulated Output From Filter

III. Circuit Design

To operate in a certain speed range, each delay circuit's delay time must be controllable to have a delay time of half bit in the speed. To accomplish this goal, controllable delay circuit employing current control bias has been used as shown in figure 6.

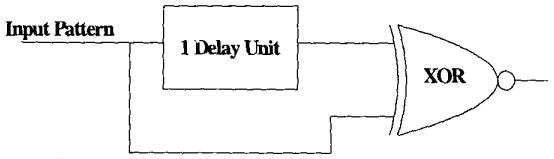

Figure 5: Frequency Doubler Circuit

Each delay unit delays the signal by one eighth. Then, one whole unit of signal is summed by summation circuit shown in figure 7. Former

4 delayed signal adds to the output and latter 4 delayed signal substracts from the output. In fact, this summation circuit with tapped delay line works as a low pass filter against frequency doubler circuit in the previous stage. The output of the filter needs to be fed into the comparator circuit to be used as a clock in the system, it also needs a phase adjuster.

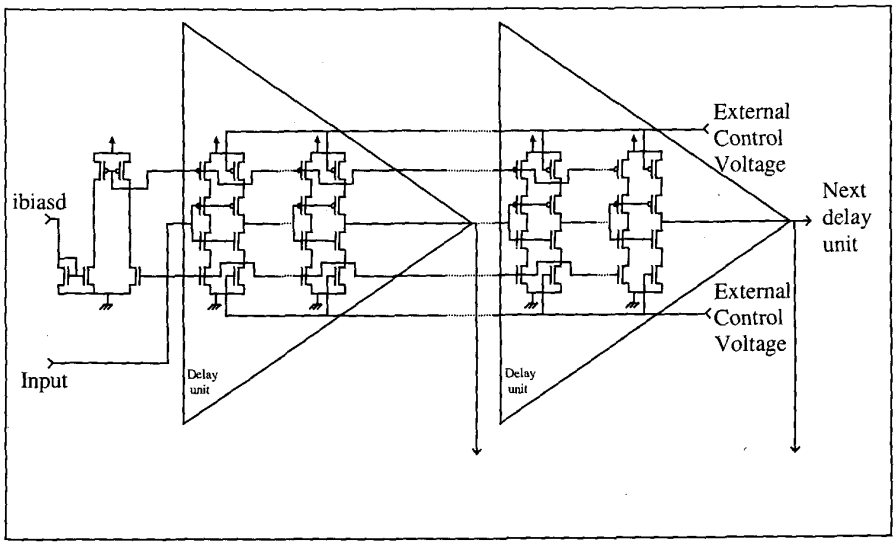

Figure 6: Controllable Delay Line of LPF

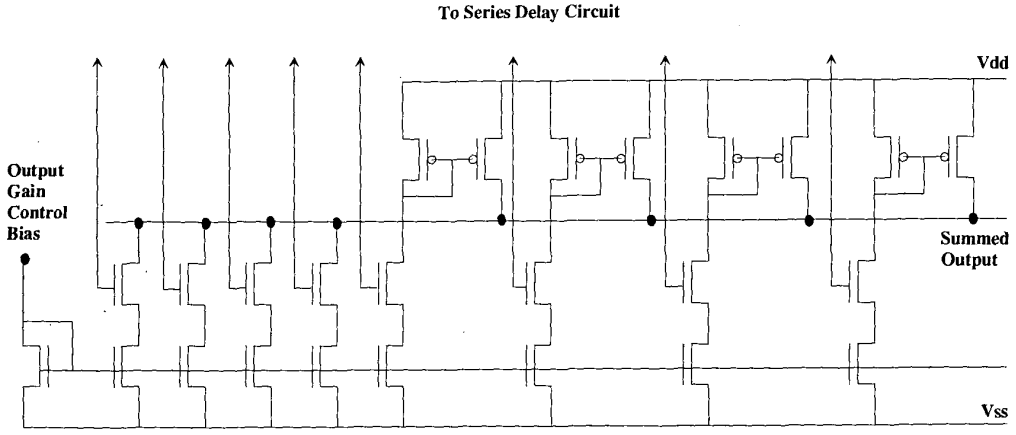

Figure 7: +/- Summation Circuit

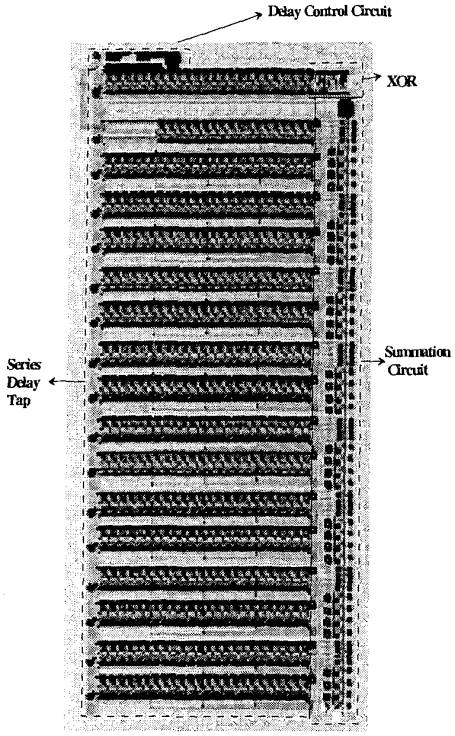

Figure 8: Layout of Clock Frequency Component Extraction Circuit

IV. Simulation Result

The SPICE simulation was performed using 2^7-1 recursive random data. As expected from the previous simulation result, when there's long stream of consecutive 0's or 1's, the amplitude of filtered output decreases. The amplitude has its maximum value when the signal changing its status frequently. In the following figure, top one shows the filtered output which contains clock frequency of random signal depicted in the middle figure and the bottom one shows the output from the XOR gate. Obviously, this signal contains the clock frequency component of incoming random signal. The controllable delay line has been verified in SPICE simulation in the speed range from 85Mbps to 155Mbps.

V. Conclusion

We have presented the method of passive component-free filter. This type of filter using multi-tap delay line can be used to implement any type of filter such as LPF and BPF. The idea has been verified by numerical simulation and circuit simulator (SPICE). Also, since this filter is not using any kind of passive component, design is to be scalable for any technology to adapt any appropriate speed range. The experimental result will be provided at the time of presentation.

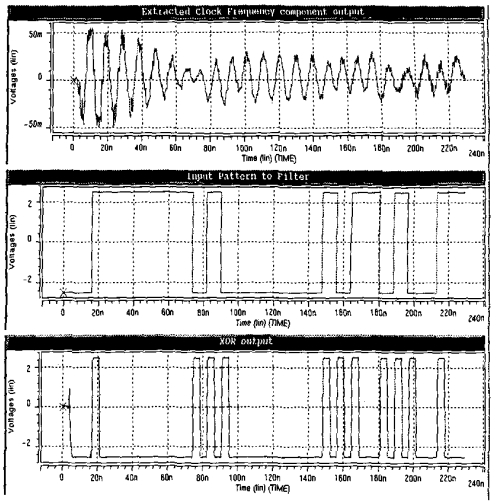

Figure 9: Simulation Result of Clock Extraction Circuit.

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