Statistical Analysis of Embedded Capacitors using Monte Carlo Simulation

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Abstract

In this paper we describe a method of accurately modeling new passive devices by deembedding the many building blocks, from which they are built, using just a few test structures. We use a nonlinear optimizer to find the optimal equivalent circuit models for the building blocks by fitting extensive high frequency measurements of the test structures behavior. We also demonstrate that the variation in the complete equivalent circuit models, based only on the circuit building blocks, can be used to predict such variations in actual fabricated devices.

Three sets of gridded parallel plate capacitor structures are fabricated on a Low Temperature Co-fired Ceramic (LTCC) process, using 2-layers of a 12-layer process. S-parameter measurements are taken and element values from Partial Element Equivalent Circuits (PEEC) deembedded using an HSPICE Optimization algorithm. Statistical variations in the deembedded element values of the structures building blocks are calculated and used in an HSPICE Monte Carlo Simulation tool. S-parameters are converted to y-parameters for convenience, and both measured and predicted y-parameters compared. The comparison between the Monte Carlo simulation results and the measured data, determines that the statistical variation of the component values provides an accurate representation of the overall capacitor performance.

The key results in this research are: the number of test structures needed is much less than the number of parameters and building blocks to be extracted; this methodology is much faster than other finite element like methods; and the equivalent circuit models and the process used to create them is accurate enough to also model the variations in the actual fabricated devices.

1. Introduction

As microelectronic technology continues to progress, there is a constant focus on higher levels of system integration and miniaturization. For example, in many applications it's desirable to package several integrated circuits (ICs) together in multichip modules (MCMs) to achieve further compactness and higher performance. Passive components (i.e., capacitors, resistors, and inductors) are an essential requirement for many MCM applications.[1] A significant advantage of MCM technology is the ability to embed a large number of passive components directly into the substrate at low cost; whereby, examination of component value statistical variation is crucial for designing and characterizing the performance of (MCM) substrates.

One technology that shows great promise for embedding passives in large area substrates is the multilayer low-temperature cofired ceramic (LTCC) approach.[2] The LTCC process can support well over thirty layers of metal, each on a thin ceramic tape substrate (several mils thick), with interconnectivity between layers achieved by the use of vias. It's also very attractive for the embedding of inductor and capacitor structures, and even resistors if a high resistivity material is used. As a result, LTCC technology demonstrates a significant potential as an enabling technology for the next generation of highly compact systems.

Successful design of passive structures in LTCC systems require that accurate models of the various components exist or can be easily obtained. However, for high frequency designs most LTCC passive structures are electrically long, and due to their full 3-dimensional geometries, have very complex field patterns. Standard modeling methods for microstrip or stripline based structures do not apply for these components. In order to successfully design LTCC structures for high frequencies, the behavior of the passive components that comprise the structure must be characterized accurately at those frequencies. Recently, computer-aided design tools such as HSPICE [3] have become indispensable in IC design; whereby, accurate circuit simulation using HSPICE is dependent on both the structural validity of the device models and the accuracy of the values used as model parameters. Therefore, the extraction of an optimum set of device model parameter values is crucial in characterizing the relationship between the model and the measured behavior.

Recently, several authors have investigated design and modeling issues for embedded passive components. Since Poddar et al. [4] presented building block based modeling of integrated passives, many other design and modeling schemes have been developed. For example Rao et al., who investigated electrical and mechanical modeling of embedded capacitors using the finite element method.[5] And Sood et al., who studied macro-modeling of embedded passive components in high performance LTCC packages using SPICE simulations.[6] And also Fathy et al., who presented modeling and design guidelines for embedded passives in LTCC on metal technology.[7]

In this paper, the building block modeling methodology created by Poddar et al. [4] is further investigated by focusing on the statistical variation of the deembedded element values of the building block models. We attempt to demonstrate that the variation in the complete equivalent circuit models, based only on the circuit building blocks, can be used to predict such variations in actual fabricated devices. The gridded parallel plate capacitor fabricated using LTCC substrate technology will be the device under inspection.

We start by fabricating three sets of integrated gridded parallel plate capacitor structures of sizes 3x3, 5x4, and 9x6,

using two layers of a 12-layer LTCC process. Scattering parameter measurements ranging in frequencies from 50MHz to 5GHz were taken from all the gridded capacitor structures. The measured s-parameter data from each size capacitor was used to deembed the element values of the partial element equivalent circuit (PEEC) of that size capacitor, using a non-linear optimization algorithm in HSPICE. This process yielded a unique equivalent circuit model for each of the three size gridded capacitor structures.

Using the unique equivalent circuit models from each structure obtained from HSPICE, mean and absolute deviation was calculated for each component of each device model in each set. A Monte Carlo Analysis for one of each size capacitor structure was then performed using HSPICE, yielding a range of 500 s-parameter curves per capacitor size. However, for these capacitor test structures y-parameters are more informative than s-parameters (especially the input admittance, $Y_{in} = y_{11}$), and based on the input admittance the accuracy of the s-parameter measurements could be verified; therefore, y-parameters for the three sets of test structures, both measured and predicted, were calculated.

The measured input admittance curves from each complete test structure were then compared to the curves generated by the Monte Carlo analysis, to determine if the measured input admittance curves reside in the range of curves generated by the Monte Carlo analysis. By inspection, it was noted that the admittance curves from the fabricated devices are in fact contained in the range of admittance curves produced by the Monte Carlo simulations. By means of comparison between the Monte Carlo results and measured data, it will be shown that the statistical variations of the component values provide an accurate representation of the overall capacitor performance.

2. Test Structure Description

The test structures were fabricated in a 12-layer LTCC process; whereby, the top metal layer was on layer 10, the bottom metal layer on layer 11, and the ground connections on layer 12. The metal thickness used was 10 mils for both plates, and the grid size was held constant, with grid "holes" of 30 x 30 mils. All capacitor structures were two layers, with a separation distance of one layer of ceramic tape in order to maximize capacitance. The upper and lower conductors were completely coincident so that the metal lines of the top conductor completely overlapped the metal lines of the lower conductor. All connections to the devices were made using a ground-signal-ground probe pad pattern on the top layer, with connections made to the devices using stacked vias and interconnect. All interconnect to and between structures was drawn on a single layer.

The first test structure consisted of probe pads connected to a 3 x 3 grid square parallel plate capacitor, and is pictured in Figure 1. The probe pad was designed such that the interface was on the top of layer for probing, with 12-layer deep via stacks for connecting probes to the ground plane, and 11-layer deep via stacks for connecting the signal probe to the interconnect layer. The second structure tested consisted of probe pads connected to a 5 x 4 grid square parallel plate capacitor, and the third test structure was probe pads connected to a 9 x 6 grid square parallel plate capacitor (both pictured in Figure 2). These test structures allowed modeling of probe pads, interconnects, and one square of the gridded parallel plate capacitor (consisting of four vertical parallel line segments), while taking into account fringe effects and coupling to the ground layer.

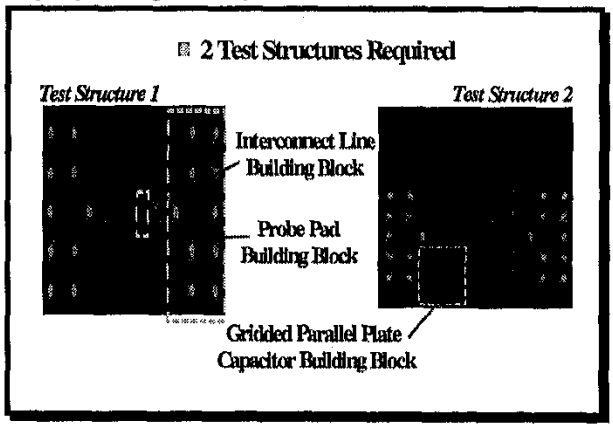

Figure #1: Probe Pad, Interconnect Line, and 3x3 Gridded Parallel Plate Capacitor

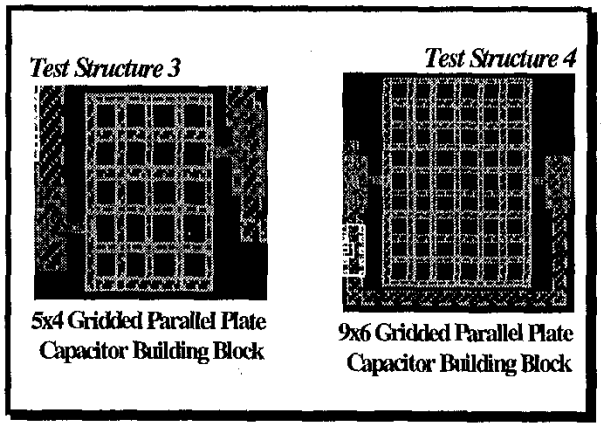

Figure #2: Probe Pad, Interconnect Line, 5x4 and 9x6 Gridded Parallel Plate Capacitor

3. Processing and Measurement

The LTCC structure was physically designed using integrated circuit design tools within the Cadence *Virtuoso* design environment. A custom technology file for a 12-layer process was developed, and a process design rule-compliant test structure coupon was produced. The design was fabricated at the National Semiconductor Corporation LTCC fabrication facility. The size of the completed coupon was approximately 2.25" x 2.25". The design utilized 12 layers of ceramic tape with a dielectric constant 7.8. Each layer of tape was 3.6 mils thick. Metal lines were drawn 10 mils wide, and the vias had a diameter of 5.6 mils. Interconnectivity between layers was achieved using stacked vias. The embedded structures were interfaced accessed using ground-signal-ground probe pads on the exposed top layer, with signals

reaching the embedded layers through vias. The complete test structure coupon is shown in Figure 3.

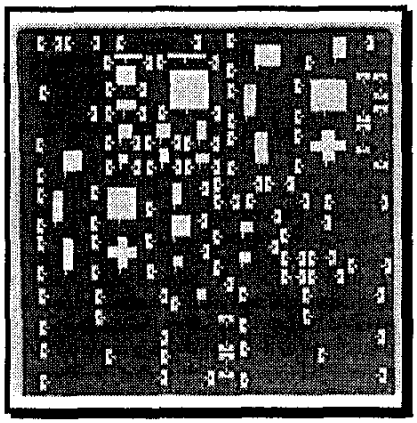

Figure #3: Test Structure Coupon

The test structures were measured using network analysis techniques. Since very low loss metal was used in the manufacturing process, DC resistance measurements were unreliable and not used. For high frequency measurements, an HP 8510C network analyzer was used in conjunction with a Cascade Microtech probe station and ground-signal-ground configuration probes. Calibration was accomplished using a supplied substrate and the application of the line-reflect-match (LRM) calibration method. Data was gathered for each of the test structures at over 200 frequency points between 45MHz and 5GHz and stored by means of data acquisition software.

4. Modeling Scheme

4.1 Capacitor Modeling Procedure

A novel method of full 3-D embedded gridded parallel plate capacitor modeling and simulation will be utilized, and is based on the generation of passive circuit element models.[8] The fundamental idea behind this modeling procedure is that passive structures are comprised of several key geometrical building blocks. The building block equivalent circuits are derived from fabricated test structures and measurements using optimization and extraction routines. Passive RLC models for each embedded building block are extracted and take into account effects of processing fluctuations and nonideal material properties. The objective here is to predict the electrical behavior of arbitrary geometry passive devices in a standard circuit simulator; therefore, providing a major speedup over methods that do not utilize lumped elements.

The steps involved in the modeling procedure for the gridded parallel plate capacitor are described in a brief outline below:

1. The nine structures were physically designed (12-layer LTCC process) and fabricated. National Semiconductor Corp granted LTCC process access. High frequency s-parameter measurements of the devices were taken by on-wafer ground-signal-ground probing.
2. The measured data was used in a circuit optimization input file to deembed the element values for the three sets of structures (3x3, 5x4, 9x6). Initial guesses used in the HSPICE Optimizer were made based on DC measured results for each structure. Once optimization for one structure was completed, the results were used for the remaining optimizations.
3. Circuit models of the different size capacitors were obtained.
4. A Monte Carlo analysis was performed on each of the three size capacitors.

Figure 4 shows the building blocks, the equivalent circuits, and some of the element values generated from the HSPICE Optimizer.

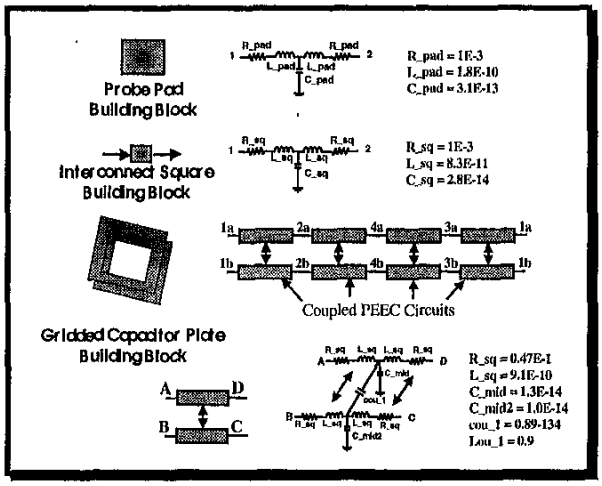

Figure #4: Building Blocks and Equivalent Circuits

LTCC technology is very well suited for the fabrication of large valued two-layer metal-insulator-metal (MIM) capacitors for use in applications such as power supply decoupling and filtering. However, metal is screen-printed onto the ceramic tape substrates creating limitations with respect to metal coverage. As a result, a specified design rule that limited the guaranteed unbroken metal coverage area to be relatively small, limited the dimensions of the solid parallel plates that might be used for the design of a standard solid-plate parallel plate capacitor. In order to overcome the metal area design rule and still be capable of generating large area capacitors, a design was developed which replaced the solid parallel plates of the capacitor with gridded plates. It was estimated that due to the many fringing fields, the gridded parallel plate capacitor might approximate the actual capacitance achieved by the use of solid plates. The gridded parallel plate capacitor would also be quite difficult and time consuming to model using standard numerical techniques, and is therefore a good test for the modeling method described above.

4.2 Parameter Extraction

After s-parameters for the test structures were measured, circuit models were extracted for the various building blocks. The fundamental circuits used were based on the partial element equivalent circuit (PEEC) [9] which has been used extensively for interconnect analysis [10] and general 3-D high frequency structural simulation.[11] The overall

equivalent circuits are comprised of a combination of these building blocks with modifications that take into account building block topology and various coupling phenomena. Figures 5 and 6 show the PEEC combinations that make up the single gridded parallel plate capacitor square.

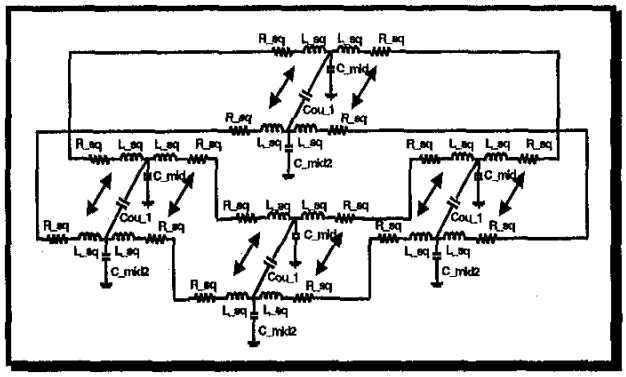

Figure #5: PEEC Circuits for One Gridded Capacitor Square

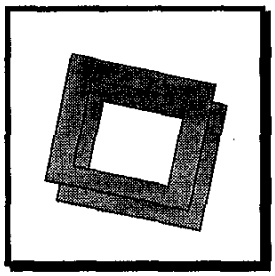

Figure #6: Gridded plate capacitor Square

The extraction of the circuit model parameters was achieved in several steps. Due to the highly nonlinear nature of the system equations with respect to circuit parameter values, a procedure for hierarchical optimization with respect to measured s-parameter data was chosen. The optimization algorithm was the Levenberg-Marquardt (LM) method [12], which is a combination of steepest descent and the Gauss-Newton method. Steepest descent is used initially to approach the solution, and then the Gauss-Newton method is used to refine the solution. The objective function of LM algorithm is:

$$F_o(X)\Big|_{X=(x_1,x_2,\ldots,x_n)} = \sum_{i=1}^{m}\left[w_i \frac{f_i(X) - F^i_{meas}}{F^i_{meas}}\right]^2 \qquad (1)$$

where X = (x_1, x_2, ..., x_n) are the component values to be extracted, n is the total number of parameters, F^i_{meas} is the measured value of the ith model parameter, m is the total number of measurements, $f_i(X)$ is the simulated value of the ith point, and w_i is a weight factor for the ith measured data point (used for giving higher significance to a given data point). Using the LM procedure, the HSPICE optimizer finds the vector X of the device model parameters that minimizes $F_o(X)$.

All simulations were performed using the HSPICE circuit simulator on Sun SPARC 20 series workstations. The starting point or initial guess of the values of circuit parameters was crucial for correct optimization results, and were approximated directly from measured data.

Three sets of test structures were optimized with respect to measured s-parameter data, and their individual building block equivalent circuit model parameters extracted. However, for these capacitor test structures, y-parameters are more informative (especially the input admittance, $Y_{in} = y_{11}$) than s-parameters, and based on the input admittance, the accuracy of the s-parameter measurements could be verified. Therefore, y-parameters for the test structures were calculated using the following parameter conversion equations [13]:

$$y_{11} = \frac{1}{Z_o}\left[\frac{(1+s_{22})(1-s_{11})+s_{12}s_{21}}{(1+s_{11})(1+s_{22})-s_{12}s_{21}}\right] \qquad (2)$$

$$y_{12} = \frac{1}{Z_o}\left[\frac{-2s_{12}}{(1+s_{11})(1+s_{22})-s_{12}s_{21}}\right] \qquad (3)$$

$$y_{21} = \frac{1}{Z_o}\left[\frac{-2s_{21}}{(1+s_{11})(1+s_{22})-s_{12}s_{21}}\right] \qquad (4)$$

$$y_{22} = \frac{1}{Z_o}\left[\frac{(1+s_{11})(1-s_{22})+s_{12}s_{21}}{(1+s_{11})(1+s_{22})-s_{12}s_{21}}\right] \qquad (5)$$

The measured versus optimized results for the three test structures are shown in Figures 7-9. As seen in these plots, very good agreement has been obtained for both Y_{in} (mag) and Y_{in} (Phase) for the three test structures. In addition, the extracted circuit model parameters are shown in Table 1.

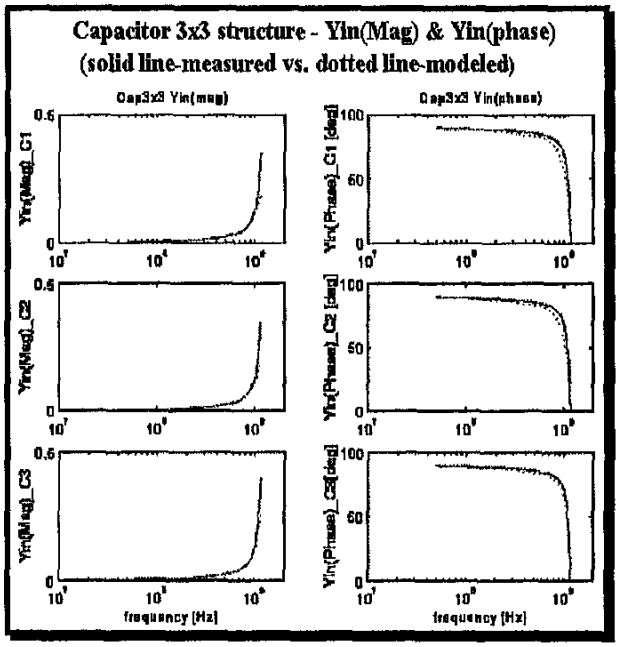

Figure #7: 3x3 Capacitor Measured vs. Predicted Y-Parameters

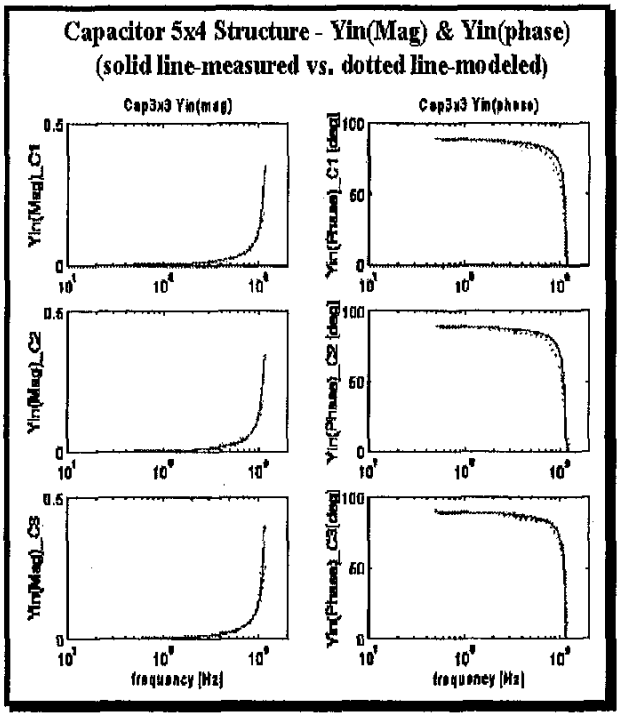

Figure #8: 5x4 Capacitor Measured vs. Predicted Y-Parameters

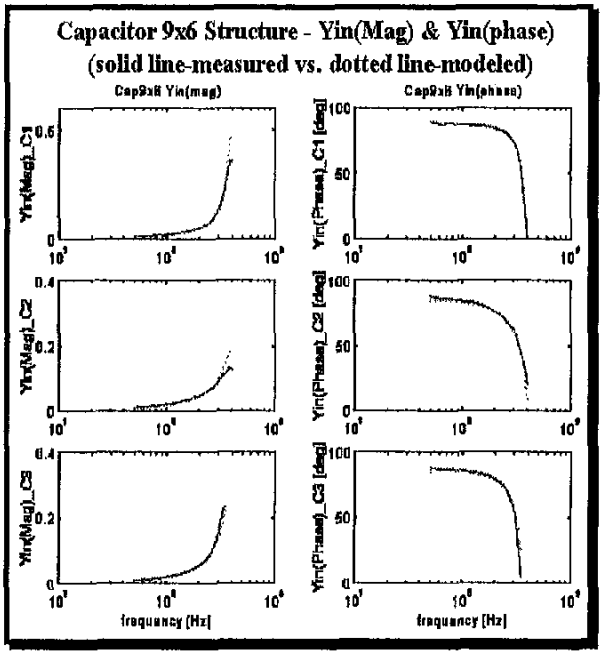

Figure #9: 9x6 Capacitor Measured vs. Predicted Y-Parameters

	C3x3_ c1	C3x3_ c2	C3x3_ c3	C5x4_ c1	C5x4_ c2
Rg1	1.00E-08	5.59E-07	1.00E-08	1.00E-08	1.00E-08
Rg2	1.56E+11	5.30E+09	9.01E+11	5.15E+10	1.58E+10
Rg3	1.24E+05	1.65E+06	9.61E+06	3.29E+06	2.27E+06
Rg4	6.27E+04	2.74E+04	2.06E+05	1.69E+07	2.34E+06
R_pad	1.00E-06	2.05E-07	1.00E-06	1.00E-06	1.00E-06
L_pad	5.83E-10	9.25E-11	1.15E-09	3.23E-10	4.81E-10
C_pad	8.63E-13	3.96E-13	1.00E-15	1.86E-12	1.52E-12
cou_l	1.00E-03	9.57E+00	2.19E-01	2.81E+00	5.77E+00
R_sq	3.98E+00	4.36E+00	3.75E-01	3.58E+00	2.68E+00
L_sq	1.02E-25	2.82E-24	2.23E-24	5.97E-10	2.77E-10
C_sq	1.34E-13	1.41E-13	1.86E-13	1.14E-13	1.13E-13
c_mid	1.14E-14	2.73E-14	1.26E-14	2.37E-14	2.33E-14
c_mid2	2.64E-16	1.96E-14	1.29E-15	6.80E-16	1.69E-14

	C5x4_ c3	C9x6_ c1	C9x6_ c2	C9x6_ c3
Rg1	1.00E+08	1.00E+08	1.00E+08	1.00E+08
Rg2	2.62E+10	1.16E+11	1.65E+06	1.44E+10
Rg3	7.08E+05	8.37E+07	1.35E+06	2.20E+07
Rg4	1.02E+06	3.46E+06	6.79E+05	4.48E+05
R_pad	1.00E-06	1.00E-06	1.00E-06	1.00E-06
L_pad	1.40E-11	8.53E-10	1.00E-15	1.22E-09
C_pad	1.18E-12	1.30E-12	1.49E-12	1.06E-15
cou_l	1.03E+00	6.38E-03	1.93E+01	9.43E+00
R_sq	2.39E+00	2.94E-05	1.18E+00	1.19E+00
L_sq	3.14E-09	8.83E-10	4.50E-10	2.37E-10
C_sq	1.18E-13	1.23E-13	1.15E-13	1.14E-13
c_mid	8.39E-15	7.98E-15	1.29E-14	1.49E-14
c_mid2	3.75E-15	3.26E-14	8.99E-14	2.47E-14

Table #1: Extracted Circuit Model Parameters

4.3 Monte Carlo Analysis

After circuit model parameters were extracted, the summary statistics (i.e., mean and standard deviation) from 9 sets of extracted model parameters (3 test structures of each size) were computed. These summary statistics are specified in Table 2. Based on these statistics, a Monte Carlo analysis for the capacitor structures was then performed using HSPICE. A Monte Carlo simulation with a Gaussian parameter distribution was generated for 500 sets of circuit model parameters. Following the simulations, the output response (i.e., y-parameters) for each test structure was obtained and compared with actual measured data to determine if the statistical variation of the model parameter values was in the range of Monte Carlo output.

	Mean (Avg)	Standard Deviation (STD)	Mean Absolute Deviation (MAD)	Percent Deviation (PD)
Rg1	9.51E+07	1.483E+07	8.79E+06	924.73%
Rg2	1.43E+11	2.893E+11	1.71E+11	11993.14%
Rg3	3.76E+07	7.594E+07	5.22E+07	13899.98%
Rg4	2.80E+06	5.425E+06	3.29E+06	11753.43%
R_pad	9.12E-07	2.651E-07	1.57E-07	1723.05%
L_pad	5.24E-10	4.675E-10	3.80E-10	7247.70%
C_pad	9.56E-13	6.844E-13	5.77E-13	6035.01%
cou_l	5.35E+00	6.506E+00	5.04E+00	9426.12%
R_sq	2.19E+00	1.583E+00	1.33E+00	6099.25%
L_sq	6.21E-10	9.929E-10	6.19E-10	9969.08%
C_sq	1.29E-13	2.353E-14	1.67E-14	1296.01%
c_mid	1.58E-14	7.120E-15	5.95E-15	3760.74%
c_mid2	1.55E-14	1.490E-14	1.24E-14	8031.61%

Table #2: Summary Statistics for Extracted Circuit Model Parameters

5. Results and Discussion

A total of nine gridded parallel plate capacitors, ranging in size from 3x3, to 5x4, to 9x6, were fabricated and s-parameter measurements taken. The measured s-parameter data from one of each size capacitor was used to extract the element values of the partial element equivalent circuit of that size capacitor. This process yielded a unique equivalent circuit model for each size capacitor. After s-parameter data was obtained, the magnitude and phase of the input admittance was calculated.

Once the extraction process was completed, a Monte Carlo analysis was performed on each of the three size test structures using the equivalent circuit models. The summary statistics (i.e., mean and standard deviation) extracted from the nine capacitors were used in the Monte Carlo simulations to create a range of 500 input admittance curves (both magnitude and phase) for each test structure. The measured input admittance curves from each complete test structure were then compared to the curves generated by the Monte Carlo analysis to determine if the measured input admittance curve resided in the range of curves generated by the Monte Carlo analysis. The results of this analysis for each of the three test structures are shown in Figures 10a-12a.

As seen in these plots, for even the small number of test structures investigated, the measured input admittance curves from the fabricated devices were in fact contained in the range of input admittance curves produced by the Monte Carlo simulation. However, in the higher frequency region, the admittance curves from the actual devices were on the borderline of the results of Monte Carlo simulation.

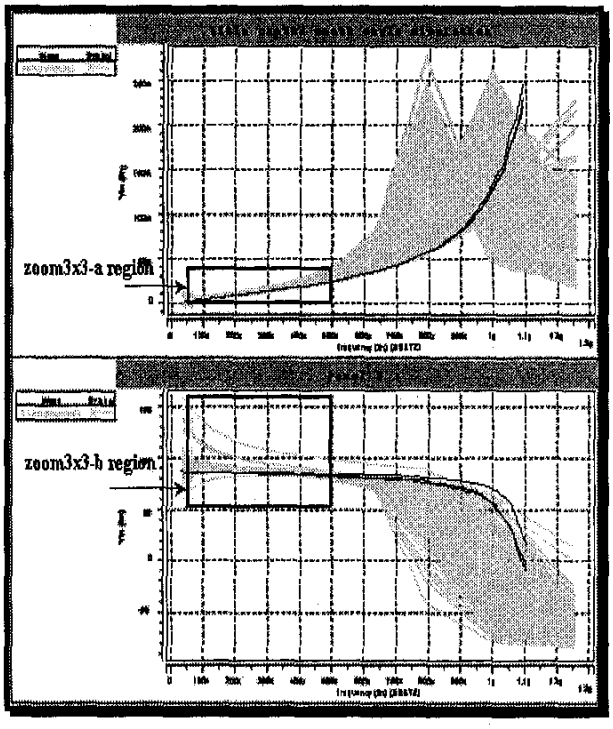

Figure #10a: Measured vs. Range of Predicted Y-Parameter Curves for 3x3 Gridded Parallel Plate Capacitor

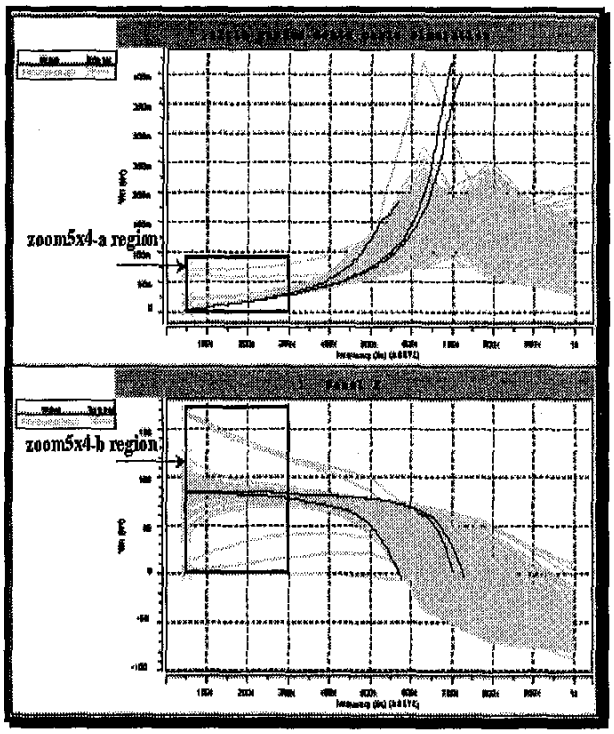

Figure #11a: Measured vs. Range of Predicted Y-Parameter Curves for 5x4 Gridded Parallel Plate Capacitor

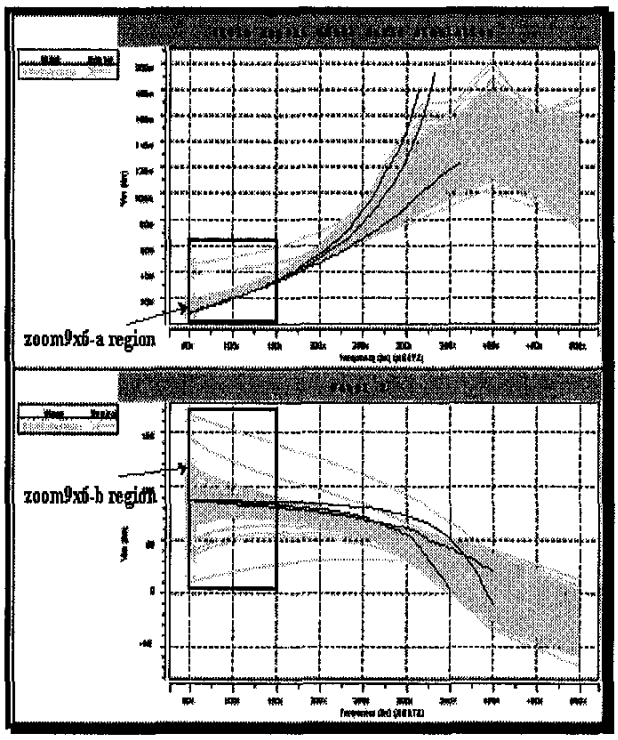

Figure #12a: Measured vs. Range of Predicted Y-Parameter Curves for 9x6 Gridded Parallel Plate Capacitor

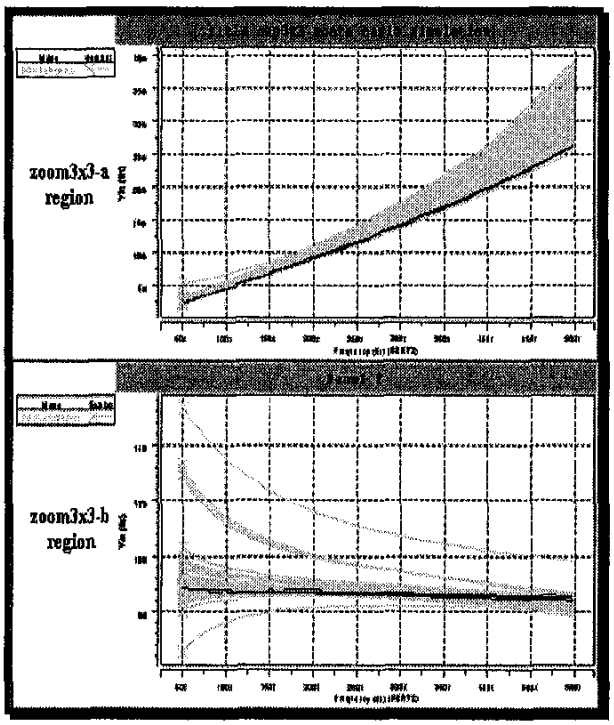

Figure #10b: Measured vs. Range of Predicted Y-Parameter Curves for 3x3 Gridded Parallel Plate Capacitor

Most circuit designers are interested in the region where component performance is critical for the capacitance value specified for a given design (shown in Figures 10b-12b). When a capacitor structure is fabricated, a circuit designer is mostly concerned about the region where the structure behaves strictly as a capacitor. Beyond this region, the structure does not behave as a capacitor because other parasitic effects are involved. For instance, consider the 3x3 capacitor test structure shown in Figure 10a. This structure behaves as a capacitor in the frequency ranges between 100 MHz and 700 MHz. Beyond 700 MHz, the test structure fails to behave like a capacitor due to inductive and other parasitic effects at the higher frequencies.

Using these comparisons of measured vs. Monte Carlo results, it has been demonstrated that the variation in the entire capacitor equivalent circuit models based only on the circuit building blocks can be used to predict such variations in actual fabricated devices.

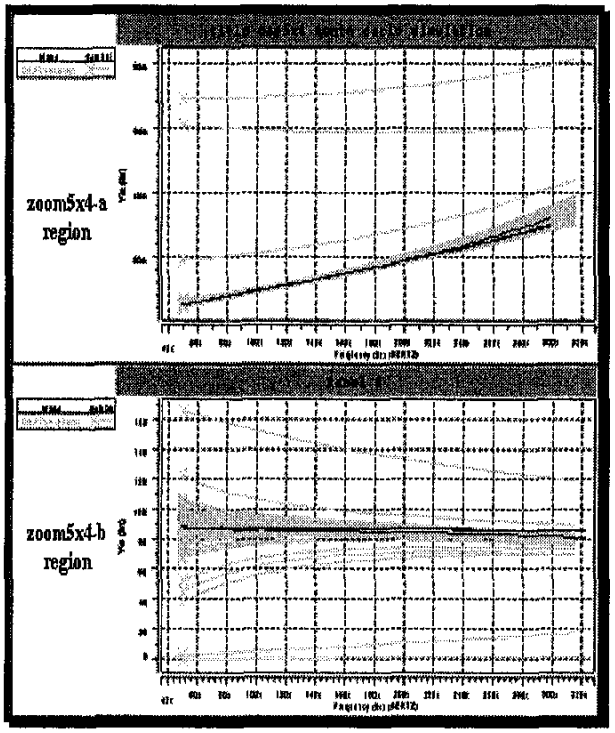

Figure #11b: Measured vs. Range of Predicted Y-Parameter Curves for 5x4 Gridded Parallel Plate Capacitor

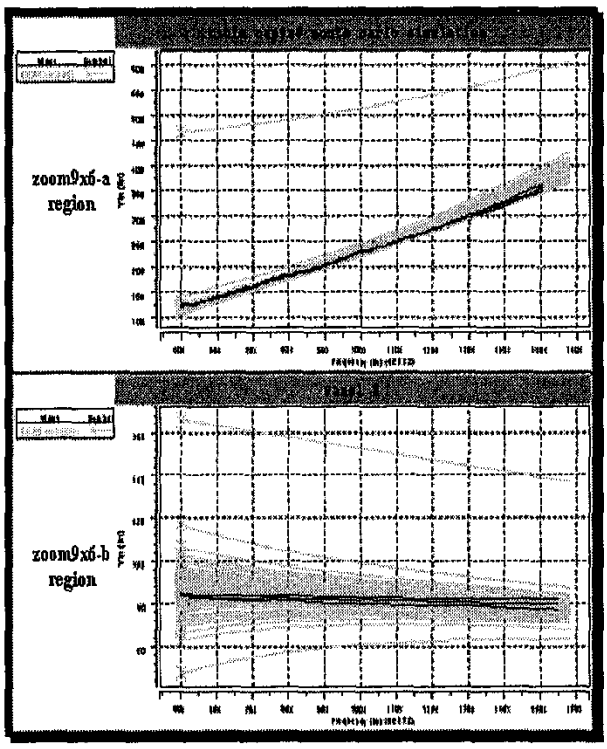

Figure #12b: Measured vs. Range of Predicted Y-Parameter Curves for 9x6 Gridded Parallel Plate Capacitor

6. Conclusion

In this paper, an investigation of the statistical variation of gridded parallel plate capacitors manufactured in a multilayer LTCC process has been presented. A total of nine gridded capacitors ranging in size from 3x3, to 5x4, to 9x6 were fabricated and s-parameter measurements taken. Statistical variations in the deembedded element values of the PEECs between all nine devices were calculated. Applying these statistical variations to the HSPICE Monte Carlo simulation tool created a range consisting of 500 s-parameter curves per capacitor size.

A comparison of the Monte Carlo simulation results to actual measured data revealed that the behavior variations in the fabricated structures were a subset of the predicted variations obtained from the Monte Carlo results. This means that the building block equivalent circuits formerly proven to model the entire capacitor structure are also accurate enough to model the variations, created by process fluctuations and non-ideal properties, between devices. It has therefore been determined that the statistical variation of the component values provides and accurate representation of the overall capacitor performance. This modeling methodology's potential could be extended to allow circuit designers the ability to predict performance and parametric yield of a given circuit containing such devices.

Acknowledgment

The authors would like to thank the National Science Foundation and the Georgia Tech Packaging Research Center (NSF Grant No. EEC-9402723) for support of this research.

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