Bidirectional Single Fiber Low-Cost Optoelectronic Interconnect for Automotive Applications

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***Abstract*—Current trends in vehicular technology reflect an increase in the number of electronic modules, leading to more complicated and expensive wiring. The use of optic fibers offers a low-cost alternative to traditional copper-wire harnesses. This paper presents a bidirectional, alignment-tolerant optoelectronic interconnect for automotive applications. The proposed interconnect offers a low manufacturing potential cost because it uses inexpensive alignment tolerant large core plastic fiber for ease of connector alignment. The optoelectronic interface chip uses time-division multiplexing to combine several information sources into a serial data stream that can be easily decoded by a microcontroller. By using a colocated small emitter in the middle of a large detector, the system achieves both bidirectional communication on a single fiber and alignment tolerant capabilities. Results show that this optoelectronic interconnect is a feasible replacement for wire harnesses in automobiles.**

***Index Terms*—Alignment tolerant link, bidirectional single fiber links, large core plastic optic fibers, low-cost automotive link, optoelectronic interconnect.**

I. Introduction

THE INCREASE in the number of electronic modules in automobiles has introduced more complicated and expensive wire harnesses with multiple connector types. Manufacturing and design costs have also increased because it is difficult to secure space for the harness installation. Reliability in these complex wiring harnesses is also problematic, and catastrophic and intermittent electrical faults in wiring harnesses constitutes one of the highest causes of service in the first five years of automobile ownership [1]. Separating the wires into signal and power lines, and multiplexing the signal lines reduce the number of wires in the harness. However, an added design difficulty is the increasingly hostile electromagnetic interference (EMI) environment in vehicles as the complexity and speed of automotive electronics increases. Unfortunately, copper wires offer low-noise immunity and are susceptible to EMI. In contrast, optical fiber is immune to EMI. When multiplexing multiple signals into a single wire, the data rate must increase to maintain a reasonable performance. These higher data rates increase EMI interference in the harness.

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Optoelectronic interconnects with plastic optical fibers can provide significant advantages in cost, weight, and EMI over existing copper wire harnesses. Many applications of fiber optics use expensive single or multimode glass fibers with a core thickness ranging from 3 μm (single mode) to 50–62.5 μm (multimode) and a numerical aperture less than 0.2. Alignment tolerance improves with larger cores, but glass fibers with core sizes larger than 100 μm are expensive when compared to plastic fibers [2]. Furthermore, glass fibers have a large bend radius, usually larger than 30 mm, making them less attractive for automotive applications. Finally, glass fibers provide extremely high bandwidth that is not necessary for automotive applications [3].

Inexpensive large core plastic fibers, typically on the order of a millimeter core diameter have been used in automotive applications [2], [4], [5]. Plastic fibers are better suited for automotive applications because they offer a larger core diameter, low connection loss, larger numerical aperture (NA), and are resilient to bending stresses. Although signal attenuation is higher in plastic fibers, the relatively short dimensions of a car make them better suited than glass fibers.

Because signal attenuation varies with temperature, different types of fibers are used for passenger and engine compartment applications [6]. Research at Georgia Tech is focused on designing a low-cost system combining integrated optoelectronics and optical fibers for automotive applications. The optoelectronic interconnect prototype can use fibers suited for either the engine (–40 to 125°C) or passenger (–40 to 85°C) compartments because the communications link optical budget can accommodate the relatively high losses of heat-resistant plastic fibers. However, the higher loss in these high-temperature fibers does reduce the optical link budget, resulting in either a decrease in the alignment tolerance, an increase in bit error rate, or an increase in link power consumption.

Using a single substrate for digital, analog, and optoelectronic the chip count, and reduces the parasitics associated with the system integration components offers a compact, integrated system with a potential for high reliability and lower manufacturing costs. This contrasts to hybrid approaches proposed in [3]–[5] that require multichip systems to achieve the same functionality. Integrating all components into a single also minimizes the required shielding. Shielding is necessary at electro-optical junctions to protect though the fiber medium is not affected by EMI noise, the sensitive receiver circuits that are susceptible to noise. A single-chip approach reduces the possibility of noise because the detector and amplifier are colocated on a single chip.

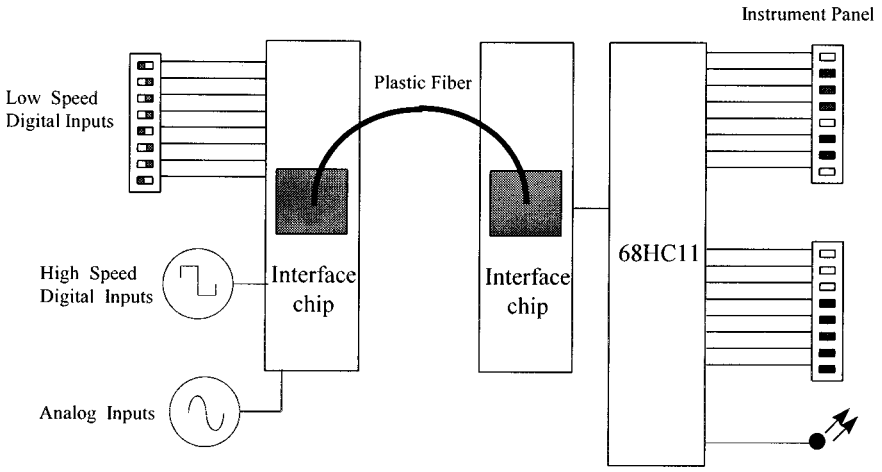

Fig. 1. Block diagram of a data-gathering optoelectronic link.

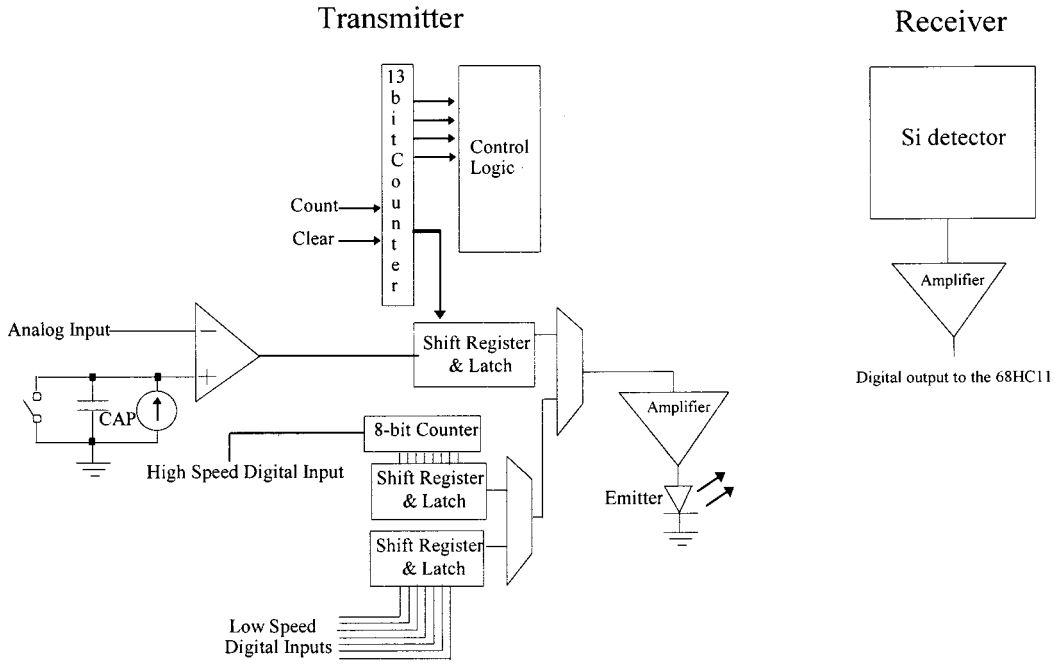

Fig. 2. Block diagram of the interface chip.

The design incorporates a colocated emitter and detector pair that allows a single fiber to communicate bidirectionally. A large silicon detector (1 mm^2) simplifies the alignment of the detector to the fiber. The large core plastic fiber can be attached to the chip using a transparent potting adhesive.

This paper describes this system in detail. Section II introduces the overall system and its major components. Section III describes the test setup and addresses the experimental results. Section IV discusses an additional enhancement to the existing system. Section V presents the conclusions and future work on this project.

II. System Overview

The silicon CMOS VLSI interface chip was designed for both transmitting and receiving information, using the same chip design at both ends of the communications link. At one end of the link, a microcontroller is employed to monitor the automobile and engage the appropriate actuators or present such information to the driver based on the information from the sensors. Fig. 1 shows a data-gathering optoelectronic link; in this case, several information sources from the engine compartment are sampled and displayed in the instrument panel.

The optoelectronic interface chip consists of analog interface circuits, an LED driver, a silicon detector and amplifier. The driver, integrated LED, detector, and amplifier are from a transceiver capable of bidirectional communication using a single plastic fiber. The interface chip collects information from different sources and then encodes it into a serial data stream. The system employs a framed return to zero protocol that is decoded at the receiving end by a 68HC11 microcontroller [7]. Fig. 2 shows a block diagram of the system.

The encoded data stream is sent to an LED, that transmits the information through a large core plastic fiber. On the other end

Partition 0	Partition 1	Partition 2	Partition 3	END OF FRAME
A/D Analog input shifted out Discharge cycle	A/D Offset sampled High speed digital input shifted out	A/D Offset shifted out Discharge cycle	A/D Analog input sampled Low speed digital input shifted out	1

Fig. 3. Data frame format.

of the fiber, the receiver in another interface chip gathers the data stream using the silicon detector. The information received by the detector is decoded by the microcontroller. Both the digital and analog circuits are implemented in 1.2-μm Si CMOS technology and were fabricated by the MOSIS [8] foundry.

Most automotive applications deal with analog and digital inputs. Depending on their rate of change, the digital inputs can be either high or low speed. The interface chip considers these different sources of information by providing an analog input, a high-speed digital signal, and seven low-speed digital signals. An 8-b A/D on-chip converter is used to transform the analog signal into an 8-b digital value. The following paragraphs describe the control circuitry and the optoelectronic subsystem.

A. Control Circuitry

The digital circuitry is responsible for sampling, assembling and encoding the three information sources into a serial data stream of digital signals. The design uses time-division multiplexing to combine the data. Although frequency-division multiplexing uses the communication channel more efficiently, it does require analog encoding and decoding circuitry at both ends of the link [5], making it more expensive. Since the data stream is going to be processed by a microcontroller, it was decided to use time-division multiplexing on the digital signals.

The data stream is packaged into frames, each with four 8-b partitions. Each partition contains the sampled data from the information sources. More resolution and flexibility are achieved in the A/D converter by using two 8-b data partitions, one for the digital value of the analog signal, and the other for a reference voltage that takes into consideration any offset on the analog signal. Fig. 3 shows the data frame format.

The end of a data frame is identified by the last bit of the third partition. This bit is not encoded by the return to zero protocol, allowing the software in the microcontroller to detect that a frame has ended. To accommodate this bit in the last partition, only seven low-speed digital inputs are sampled. More inputs can be sampled by either extending the number of partitions in a frame, or by increasing the number of bits in each partition. The high-speed digital input is for those signals that change at a higher frequency than the sampling rate of the interface chip. To measure their logical values, a counter is used to store the time between logic changes. This technique converts the time between signal changes into an 8-b value, assigning smaller values to those signals with higher frequency. The slow-speed digital signals are sampled only on the third partition of the frame. It is assumed that they will remain at the same value for several frames.

The analog input and reference voltages are converted into digital numbers by using an A/D conversion scheme based on an analog comparator and a counter. Please refer to Fig. 2 in the following description. At the beginning of the conversion the capacitor is fully discharged and the counter begins its count from zero. The capacitor charges using a constant current source. When the voltage at the capacitor matches that of the input signal, the analog comparator sends a pulse to the digital circuit which in turn stops the counter, and the count value is then stored into a register. The stored value indicates the digital equivalent of the analog voltage. The current source is set to allow a full count over the voltage range of 0–5 V. Analog signals are sampled on every other 8-b partition allowing for discharge periods in between conversions, guaranteeing that the capacitor is fully discharged before the next conversion begins.

B. Optoelectronic Subsystem

A large silicon detector (1 mm^2) is implemented as an array of parallel bipolar junction transistors with the base current controlled by the input optical signal. This Si CMOS detector is capable of absorbing wavelengths below one micron. The silicon photodetectors, consist of a small n-type central emitter diffusion, a large p-type base diffusion, and a ring electrode n-type collector. A receiver amplifier takes the output of the silicon detector, amplifies it, and then produces a 1-b digital signal. The overall gain of the silicon detector and amplifier is approximately 10^6. The shallow diffusion depth available in Si CMOS, coupled with the low-absorption coefficient of Si, results in a detector with a low responsivity. However, when the CMOS detector is embedded in a BJT structure, the BJT gain can be accessed. The measured Si CMOS BJT responsivity for these detectors is 0.87 A/W $\pm$ 0.08 A/W.

The emitter device is a double heterostructure thin-film GaAs-based emitter which emits light at 870 nm (infrared). The device measures 250 μm $\times$ 250 μm $\times$ 2 μm thick and is bonded into the center of the silicon detector. The silicon detector contains a 300 μm $\times$ 300-μm hole in the center, with an overglass cut to a pad on the Si CMOS circuit for the bottom contact to the emitter. Thin-film integration [9] is used to optimize the fabrication processes for the emitter. This process involves emitter device top contact deposition and patterning, mesa etching, growth substrate removal, bonding to a transfer diaphragm, and subsequent metal/metal bonding to the Si CMOS circuit. [8]. The metal/metal bonding of the emitter to the pad in the center of the Si CMOS detector is a critical aspect of the reliability of this system. Thin-film integration using metal/metal bonds produces a bond which is electrically conductive, mechanically stable under thermal cycling, and thermally conductive, which is in contrast to contact bonding. This type of bonding also enables partial test of the devices before rapid thermal annealing, which enables the replacement of the emitter if necessary. After bonding the emitter to the Si CMOS circuit, the chip was isolated with polyimide, and a top contact from the emitter to the circuit (shown as a metal link to the left of the emitter in Fig. 4) is deposited. The integration of the emitter to the Si CMOS circuit is then complete [8]. The light-emitting diode emitters have high reliability and high lifetime compared to lasers, but also have lower efficiency [9]. The drive current to the emitter was typically in the range of 60–100 mA at approximately 2 V and was modulated from zero mA to the maximum current. The same emitter structure

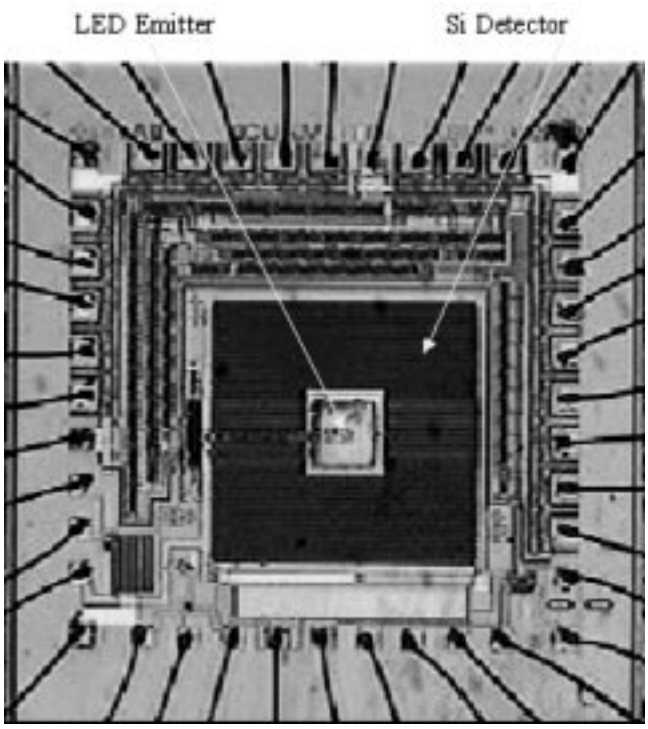

Fig. 4. Photomicrograph of the interface chip with integrated emitter.

integrated onto metal contact pads demonstrated an external quantum efficiency of 1.4%. The heat dissipation associated with this emitter did not affect the Si CMOS detector or circuit in part because the emitter was not integrated on top of circuitry. Arrays (8 × 8) of emitters bonded directly on top of Si CMOS driver circuits running in continuous mode did not affect the Si CMOS transmitter operation due to heating [10]. A more detailed description of the optoelectronic subsystem can be found in [11].

An emitter driver capable of providing the necessary current to operate the device using a digital input signal is also implemented. The driver uses two gain stages with an overall gain of 100, and it is capable of supplying an output current to the emitter of up to 10 mA at a speed of 1 MHz. Fig. 4 shows a photograph of the interface chip with the integrated emitter in the center of the silicon detector. The circuitry in the periphery are the digital and analog components of the system.

III. System Evaluation

Research in this project consists of both modeling and implementation of the optical link. This section briefly describes the results of the modeling effort and the implementation of the interface chip.

A. Modeling

Alignment tolerance is crucial for reducing manufacturing costs and increasing the reliability of the overall system. Alignment tolerance can be expressed as the ratio of the power coupled with misalignment and the power coupled without misalignment. There are two types of misalignment, longitudinal and lateral, shown in Fig. 5. Because of the large size and sensitivity of the detector, the large diameter of the fiber, and the positioning of the small emitter in the center of the detector, the fiber can have large longitudinal and moderate lateral misalignments while still maintaining the integrity of the communications link. This feature relaxes the constraints of fiber termination and coupling processes, allowing less expensive packaging techniques [12].

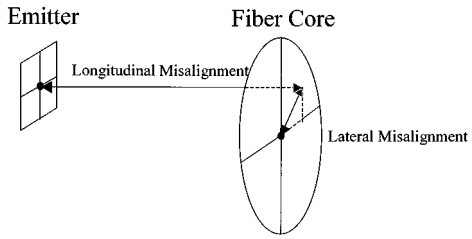

Fig. 5. Illustration of longitudinal and lateral misalignment between the emitter and fiber.

A fast technique for computing the coupling efficiency between the emitter and the step-index optical fiber is reported [13]. In that work, Fourier series representations of the LED and the fiber core geometries enable a 100-fold reduction in the computational load in the classical geometrical optics solution. In [13], the dependence of coupling efficiency on lateral and longitudinal misalignment, emitter area and directivity, and fiber numerical aperture and core radius is shown. These results match experimental measurements in which longitudinal and lateral misalignments of up to 1.5 and 0.4 mm, respectively, produce a loss of less than 3 dB [14]. This wide margin for misalignment allows an expedient assembly of the optical link without expensive equipment.

B. Implementation

The dies received from the MOSIS foundry were integrated and bonded into a 40-pin dual in-line pin (DIP) ceramic package. Two separate test fixtures were assembled to test the chips, one for each end of the communication link. Each fixture generates all the required signals (both analog and digital) for the proper operation of the interface chip. The fixtures only require an external 5-V power supply. One of the test fixtures includes a 68HC11 microcontroller used to decode the data stream sent from the other fixture. The program that decodes the information was stored in the EEPROM of the microcontroller. Fig. 6 shows a picture of the test fixture.

Using two optical XYZ stages, a 1-mm-large core plastic fiber was positioned above the emitter and detector on each chip, roughly centered above each detector/emitter pair. After the microcontroller decodes the data stream, it presents the information in three indicators in the test fixture. These experiments were done at data rates of up to 8 Kb/s. The maximum operation frequency of the system is 50 kHz and is most likely limited by the slew rate of the large-gain low-bandwidth detector amplifier. For 1 M of ESDA EH4001 large core (1-mm core) diameter fiber, the total fiber input coupling and attenuation loss was measured to be −8.1 dB, and the fiber to detector coupling loss was measured at −4.2 dB. Note that the power throughput from the optical fiber to the detector is limited to 87% since the emitter area does not contribute to detection. A theoretical analysis of the link budget gives a fiber attenuation for 1 M of this

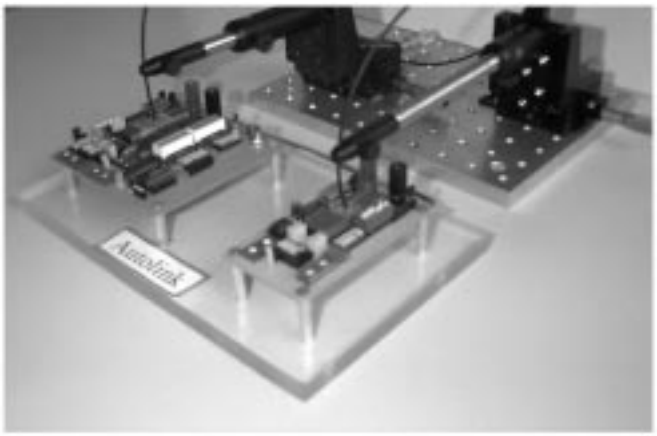

Fig. 6. Photograph of test fixture.

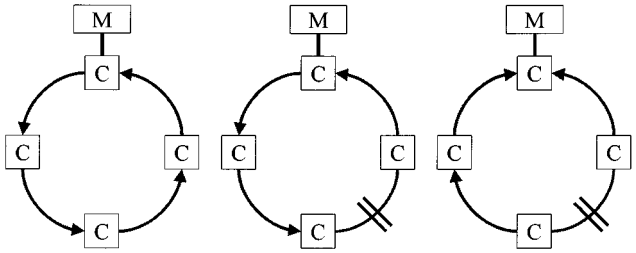

Fig. 7. Fault tolerance in a ring topology constructed with reconfigurable bidirectional links.

ESDA fiber of –2.5 dB at $\lambda = 870$ nm, and the theoretical link coupling efficiency was –5.5 dB for the emitter/fiber and –4.1 dB for the fiber/detector.

The demonstrated system operates as a unidirectional link (e.g., a microcontroller decodes the data stream at one end of the fiber). Colocation of emitter and detector allows the implemented system to transmit in either direction and this capacity was tested [11]. Bidirectional communication can be supported (with an additional microcontroller) using a half-duplex protocol. This minimizes crosstalk resulting from reflections of emitted light of the fiber surface onto the detector (near end crosstalk).

IV. System Enhancements

The full implementation of reconfigurable bidirectional communication provides additional functionality and fault tolerance. For sensor-controller communication, configuration and self-test information can be transferred to the sensor module before the sensor data stream is initiated. A query protocol (as opposed to continuous protocol implemented here) can also be realized.

A demonstration chip for bidirectional communication between the sensor/actuator and control units has been implemented with a small modification of the unidirectional data frame format. The protocol for data transmission, illustrated in Fig. 8, is query based, so the sensor/actuator unit does not transmit data until a request is received from the controller. To initiate a bidirectional transmission sequence, the control unit sends a long "on" pulse followed by the first data frame. The sensor/actuator unit detects the long pulse, receives the

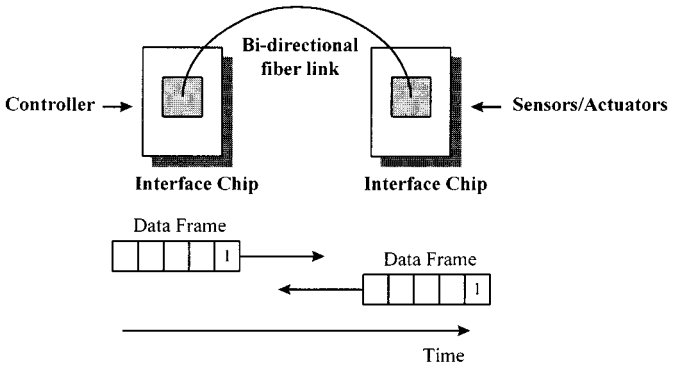

Fig. 8. Data frame time multiplexing for bidirectional transmission.

controller data frame, and then transmits its data frame back to the controller. The controller receives the sensor/actuator data frame to complete sequence. The controller data frame can include self test and configuration information.

Two additional circuits are included to handle the bidirectional transmission. The first detects a long pulse and initiates the query sequence. It charges and discharges an RC network. The second circuit is a state machine that handles the receive and transmit mode of the chip. When the long pulse is detected, the circuit forces the chip to begin receiving the controller data frame, and then transmits the sensor/actuator data frame back to the controller.

A test chip designed to implement this advanced protocol has been fabricated and electrically tested and is currently being optically tested.

Bidirectional communication can also be profitably incorporated for controller–controller communication. General bidirectional intercontroller communication can be supported with an arbitrating protocol. A simpler reconfigurable unidirectional ring topology (built with bidirectional links) can provide a recovery mode if a fiber link is broken. As illustrated in Fig. 7, all controllers (C) can pass data to the master (M) using a unidirectional ring. When a link fails, the working links can be reconfigured to provide an alternative path to the master. This fault tolerance is critical in automotive applications where single-link failures could otherwise lead to a potentially dangerous situation.

V. Conclusions and Future Work

This paper presents an automotive interconnect system design that incorporates plastic optical fiber, optoelectronic devices, and digital control circuitry. The design is focused on a potentially low-cost solution and provides tight coupling between the optoelectronic and electrical interface. Manufacturing and assembly costs are reduced using integrated optoelectronics and hybrid CMOS designs by integrating all of the components of the communications link into a single-chip substrate.

This interconnect systems includes colocated emitter and detector devices that allow a very alignment tolerant connection. Modeling and experimental results show a significant allowable longitudinal and lateral misalignment of the plastic fiber. This design permits the fiber core to be aligned expediently by hand during assembly without precision equipment.

In addition, the colocated optoelectronic subsystem allows a bidirectional data transmission using only a single fiber. This enhancement requires a minor modification to the unidirectional circuitry and transmission protocol. This research work will continue with improved circuitry and optoelectronic devices to increase the link bandwidth and reduce the error rate. New prototypes are being implemented with a thin-film emitter that operates in the range of 650–670-nm (red) wavelengths. The attenuation in the fiber is decreased at these wavelengths leading to greater alignment tolerance and improved performance of the link.

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