

## Smart Photonics: Optoelectronics Integrated Onto Si CMOS Circuits

Nan Marie Jokerst, Martin A. Brooke, Joy Laskar, D. Scott Wills, April S. Brown, Olivier Vendier, Steven Bond, Jeffrey Cross, Michael Vrazel, Mikkel Thomas, Myunghee Lee, Sungyung Jung, Yoong Joon Joo, Jae Joon Chang  
Georgia Institute of Technology

Interconnections are a limiting cost and performance factor in present electronic systems, and become even more critical as wiring, processing densities, and speeds increase. Historically, optical interconnections have been most successful in long haul applications where relatively few optoelectronic interfaces are necessary, and costly optoelectronic (OE) interfaces were justified. With the meteoric rise of datacom, which includes medium distance (e.g., "campus" and LAN), short haul (e.g., small office and home), and the ultra-short chip to chip interconnections referenced in the SIA Roadmap, which projects Si ICs facing interconnection bottlenecks before 2010, optical interfaces and interconnections optimized for shorter distances are under intense development. Optoelectronics (OE) can significantly impact the performance of these interconnections, however, the implementation of optoelectronics has, to date, been prohibitively expensive in most cases. To achieve increased OE implementation, cost reduction is critical. Smart photonics, or the integration of OE devices and links with circuitry such as Si CMOS VLSI, can yield both advanced optical links and possibly integrated solutions for optoelectronic interfaces and interconnections to standard electronic systems. Coupled with alignment tolerant designs, these implementations may yield cost effective solutions which are compatible and integrable with electronic systems. For many years, the optics community viewed silicon as the competition. However, silicon is the material of choice for electronics, and only recently has the optical community begun to view silicon as a prime target for OEIC circuitry, rather than as a competitor.

Using thin film OE and electronic device integration coupled with alignment tolerant optical designs, optical interconnections can be used for system applications such as automotive wiring harnesses, smart imaging, and Si CMOS parallel multi-processor 3D interconnections. Hybrid integration, or the bonding of two independently fabricated devices/circuits to form a hybrid system, eliminates difficulties associated with monomaterial integration (all GaAs electronics and optical devices lead to performance trade-offs and lower yields) and with direct growth of compound semiconductors onto silicon (lattice mismatch and coefficient of thermal expansion mismatch limits material quality). Through hybrid integration, independently optimized devices/circuits can be joined to form an integrated system with reduced parasitics in comparison to hybrid, individually packaged devices. For example, in a bonded system, the receiver input resistance is not set to 50 ohms, but may be increased to achieve lower noise operation.

Alignment tolerance and hybrid integrated packaging parasitic reduction are critical design elements which can decrease the cost and improve the performance of optoelectronic interfaces and interconnections. The heart of this work is to blur the boundaries between the package and the system, particularly in the area of interconnection, and to provide to circuit and substrate designers the building blocks with which they can access high quality optoelectronic interfaces and interconnections. This access to optoelectronics offers to the system designer performance enhancements which include increased number and speed of interconnects, decreased packaging parasitics, lower latency, increased parallelism, improved heat dissipation, smaller interconnection footprints, lower power consumption, and three dimensional interconnections. Also enticing is the development of OE "building blocks" with digital input/output and purely electrical characteristics, for engineers who are uncomfortable with optical analysis.

To achieve alignment tolerant optoelectronic receivers, we utilize inverted MSM (I-MSM) photodetectors, which are thin film detectors with fingers on the bottom of the device. These detectors are high speed, large area photodetectors with excellent responsivity, and, for the same capacitance, MSMs are larger in surface area than p-i-n detectors, hence, the MSMs are more alignment tolerant. The bonded integration of these I-MSMs with Si CMOS receivers has yielded 155 and 250 Mbps in 0.8 and 0.6  $\mu\text{m}$  CMOS, with current integration toward 1 Gbps in 0.35  $\mu\text{m}$  CMOS. Integration with GaAs circuits have yielded a 2.4 Gbps receiver, and we are currently integrating a 10 Gbps OEIC receiver (InP/InGaAs I-MSM on a GaAs traveling wave amplifier circuit). These circuits, combined with thin film emitters and Si detectors, have been used to demonstrate optical links which include co-located, bi-directional fiber links for the automotive/avionic industry, as shown in Figure 1, and 100-400 Mbps links for in-home fiber networks. Optoelectronic link and system circuit and alignment tolerance optimization can be approached through optoelectronic link modeling coupled with experimental model verification. The complex design space of OE systems, which includes power, speed, efficiency, heat dissipation, alignment tolerance, bit error rate, crosstalk, noise, and size, has begun to be investigated. To achieve higher speeds, the integration of thin film OE components and high speed electronic components such as RTDs and HBTs will also be discussed.

For image processing and generation, arrays of devices can be integrated onto Si CMOS circuits, with each thin film device interconnected directly to the circuitry underneath the pixel, as shown in Figure 2.

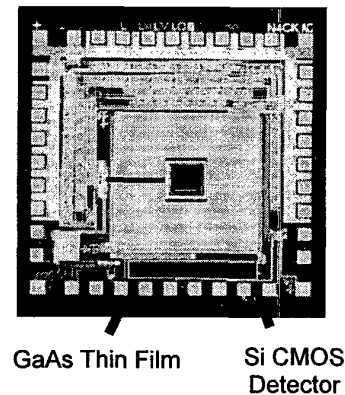


Figure 1. Single fiber bi-directional optical link.

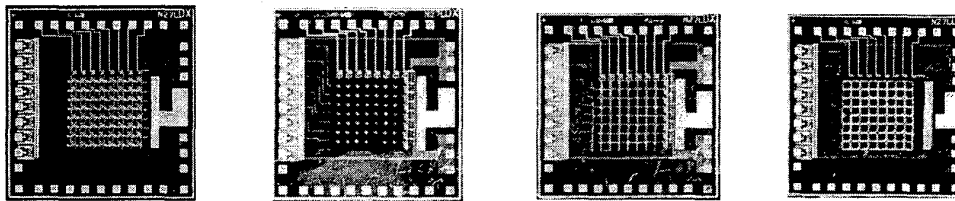


Figure 2. Integration process for thin film GaAs P-i-N devices onto Si CMOS circuitry.

Finally, the prospects for integration in three dimensions (3D) is enticing, whether in the stacking of thin film circuits, active, and passive devices, or in the vertical optical interconnection of Si CMOS circuits using through-Si optical signals to which the Si CMOS is transparent, as shown in Figure 3. Both of these options will be explored in the context of hybrid thin film integration and packaging. Applications which will be examined are parallel Si CMOS multiprocessor systems, smart focal plane arrays, and co-located multispectral detector arrays.

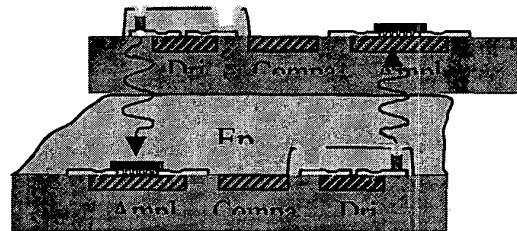


Figure 3. Schematic of stacked Si CMOS circuits with through-Si vertical optical interconnections.