Smart CMOS Focal Plane Arrays: A Si CMOS Detector Array and Sigma–Delta Analog-to-Digital Converter Imaging System

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***Abstract*—This paper evaluates the potential for the real-time utilization of high frame rate image sequences using a fully parallel readout system. Multiple readout architectures for high frame rate imaging are compared. The application domain for a fully parallel readout system is identified, and the design for a fully parallel, monolithically integrated smart CMOS focal plane array is presented. This focal plane image processing chip, with an 8×8 array of Si CMOS detectors each of which have a dedicated on-chip current input first-order sigma–delta analog-to-digital converter front end, has been fabricated, and test results for uniformity and linearity are presented.**

***Index Terms*—Imaging, smart focal plane array.**

I. Introduction

IMAGING detector arrays and image processing circuits are critical components in many consumer, industrial, and military focal plane imaging array systems. System specifications emphasize different aspects of imaging array technology, including high frame rate, large array size, high fill factor, and high pixel resolution. Over the past several years, significant advances in focal plane array (FPA) development have been achieved. The number of pixels has increased to several thousand on a side, and the number of bits per pixel of the arrays has also increased [1]. The combination of higher bits per pixel with a larger number of pixels has resulted in data rates that can not be transmitted off of the FPA through a one-port readout system. This data bottleneck is exacerbated when the application demands high frame rates, which further challenges the data transfer rate off of the FPA. Important emerging high speed imaging applications include combustion, trans-Mach fluid flow, and aerooptic imaging, which require high frame rates that cannot be handled by conventional image data transfer methods [2]–[4].

In addition to enhanced detector array performance, the integration of image processing circuitry on the focal plane, or the realization of "smart" focal plane arrays, is an area of research under intense study. Through preprocessing of the raw image signal using on-focal-plane integrated circuitry, the data transfer performance limitation of the imaging system can be addressed. Conventional imaging systems use X–Y readout of the sensor array data followed by transportation of the data to an off-chip serial analog-to-digital (A/D) converter (ADC). On-chip A/D conversion is potentially a superior choice for an integrated imaging/preprocessing smart imager, since it can reduce the cost, complexity, weight, and noise pickup of the FPA system. Three different on-chip readout systems have been developed. The first is a serial readout system, involving X–Y multiplexing of sensor data to a single on-chip ADC [1]. The second approach is a semiparallel readout system with an ADC for each image column [5], [6]. The third option is a parallel readout system with an ADC dedicated to a pixel or group of pixels and 3-D interconnect off the back of the focal plane [7].

The parallel readout system is the best choice to accommodate ever increasing data rates for off-chip data transfer. This option performs the A/D conversion as early as possible in a signal chain to avoid processing and transportation of analog signals, and instead, utilizes the digital processing capability of modern CMOS processes. The per pixel A/D conversion is the extreme of this solution, namely, associating one ADC with each pixel. The advantages to this approach are that no signal degradation occurs when digital data is read out of the detector array. When this parallel readout architecture is combined with a three-dimensional (3-D) through-Si vertical optical communication link, a truly fully parallel readout system can be realized. Using this architecture, a virtually unlimited scalable high speed readout system for a FPA system can be demonstrated.

This paper explores the design and implementation of a smart FPA using an integrated detector array and signal processing circuitry. Si CMOS detectors have been used for the imaging detector array, which are integrated directly with per-pixel Si CMOS sigma–delta ADC's, which preprocess the detected image signals. Performance data for this integrated smart FPA is included herein. In a future system, these FPA signals can be passed down through the Si CMOS using an integrated CMOS emitter driver which has been integrated onto the imaging chip for 3-D vertical through-Si data transfer to a second chip containing an image processor. The design of the smart FPA is explored in the context of the final two layer image processing system.

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II. Architecture

To achieve image processing systems that operate in real time, on large images with frame rates in the high kilohertz or megahertz, is beyond the capability of today's imaging systems. For example, a first-order sigma–delta ADC generating a sequence of 500 × 500 8-bit images at a frame rate of 100 kHz must be clocked at more than 655 GHz, which is currently far from practical. Even when parallel ADC's are placed along the edge of the imaging array, the problem is only partially mitigated because the speed at which the ADC's must operate still increases with image size. To generate 500 × 500 8-bit images at a frame rate of 100 kHz, we need 500 ADC's, on the same die, clocked at more than 1.31 GHz [7]. It is beyond any current technology to make that many high speed ADC's on one die. Thus, serial ADC's are inadequate for this task, and highly parallel ADC's must be examined for evolving high data rate systems.

In this paper, a fully parallel readout system is designed as a scalable FPA readout system. This readout system provides a scaleable solution to the real-time high frame rate image capture problem when it is coupled to a massively parallel optically interconnected processor. To keep the design scaleable, the processors must reside beneath the imaging chip, which, in the final system, will use a through-Si vertical 3-D optoelectronic interconnect for parallel connection to the detector plane. This is a scaleable design, since, as the image size increases, the number of parallel vertical optical 3-D links and the number of processors in the array can increase accordingly, thus maintaining the frame rate. The system design, using a through-Si integrated parallel optical data link, is illustrated in Fig. 1.

The fully parallel readout system was designed so that each pixel has an associated ADC, and subarrays of these pixels/ADC's are served by one vertical optical link and one digital signal processing (DSP) unit to perform image processing. To maximize the imager fill factor, it is necessary to minimize the area of the ADC circuitry. Thus, only the front end of the sigma–delta ADC was implemented on a per pixel basis in the detector array, and a first-order current input sigma–delta oversampling ADC was chosen because it is the smallest of the sigma–delta front ends. The advantage of this architecture is that the sigma–delta ADC front end produces digital data, so further noise cannot be introduced to the signal by shifting the digital data. This is in contrast to analog signals, which are the format used in all conventional FPA links. An integrated optoelectronic emitter on each subarray allows through-silicon wafer output of digital image data from the focal plane to the processor stacked below each subarray, as shown in Fig. 1.

An integrated optoelectronic emitter on each subarray allows vertical through-Si output of digital image data from the focal plane to the processor stacked below each focal plane imager. These integrated through-Si vertical optical data links have been demonstrated using stacked foundry Si CMOS circuits [8], [9] and are a viable technology for 3-D system integration. This 3-D vertical coupling to the image plane allows the detector and processor arrays to be scaled while

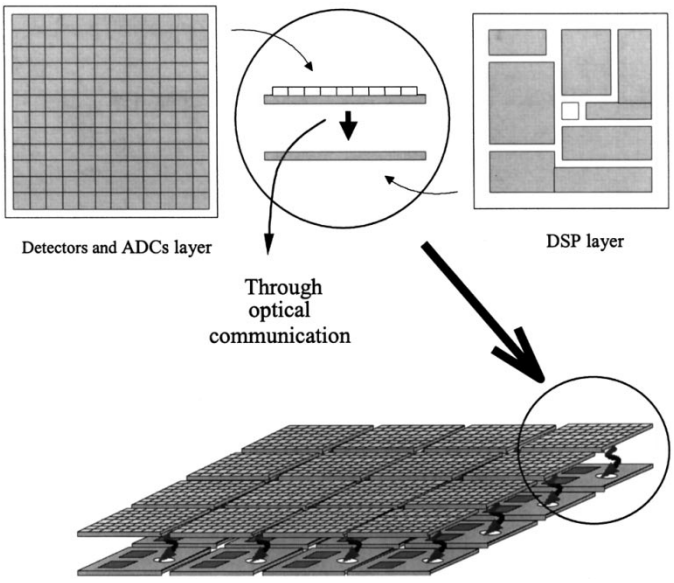


Fig. 1. A stacked two-layer focal plane processor.

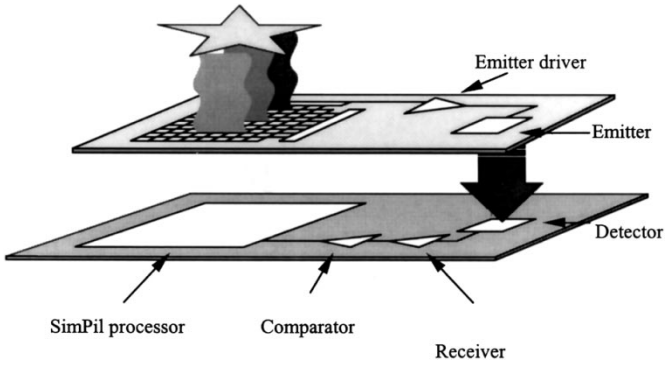


Fig. 2. Signal flow of the FPA subarray.

maintaining a fixed level of processing per pixel, as shown in Fig. 1. Thus, the processing rate is independent of the total imager array size, resulting in a scalable readout system. The ideal number of pixels in the subarray depends upon the processing required and the bandwidth of the associated processor circuitry. For the SIMPil processor used in this design, if an 8 × 8 subarray is used, the size of the processor and focal plane subarray match reasonably well. At the target frame rate, an 8 × 8 subarray of detectors produces data rate matching the computational throughput capacity of a single SIMPil processor [10]–[12]. For example, a 256 × 256 pixel imaging array with 8 bits of resolution operating at a 100-kHz frame rate could be realized by tiling an 8 × 8 array of these 8 × 8 imager and processor subunits each operating at a speed of 167 Mb/s.

An 8 × 8 image sensor subarray of detectors and per pixel sigma–delta ADC's has been designed, fabricated, and tested in digital Si CMOS. Fig. 2 is an illustration of the implemented image sensor subarray. Each subarray consists of an array of 8 × 8 multiplexed pixel blocks, each consisting of a photodetector and a single sigma–delta ADC front end. Each pixel block was connected to a bit line using a pass transistor. The bit lines are read using an eight-row address decoder and

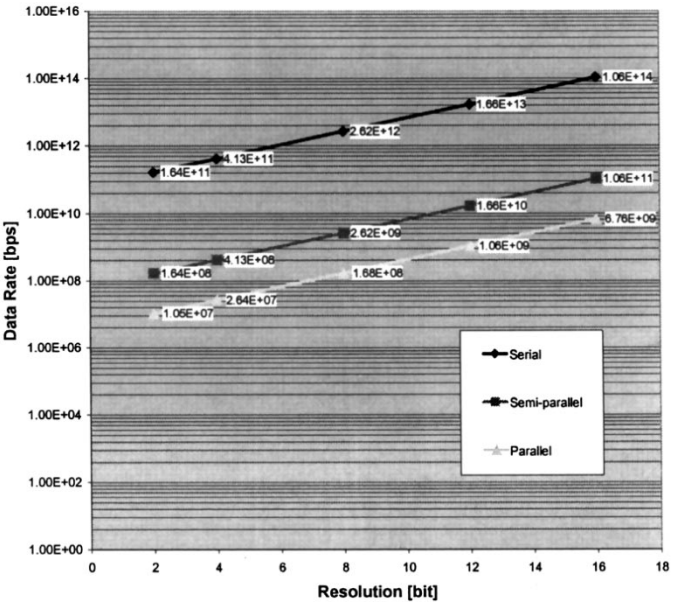
an array of eight digital sense amplifiers. Each pixel block converts the analog light intensity into a digital signal. The entire system is synchronous, and after each clock pulse, every pixel block produces one bit of data. This generates a two dimensional array of bits. All of the generated digital output signals are amplified by the emitter driver to drive an integrated optoelectronic emitter on each subarray, optically interconnecting the imaging/preprocessing array to the SIMPil processor on the second level of circuitry.

On the bottom level of the system, the optical signal is received by an integrated detector, producing a small analog signal. This signal is amplified and synchronized by a clocked comparator. The digital output of the comparator is serially transferred to the SIMPil processor. The signal path from image detector to signal processor is shown in Fig. 2.

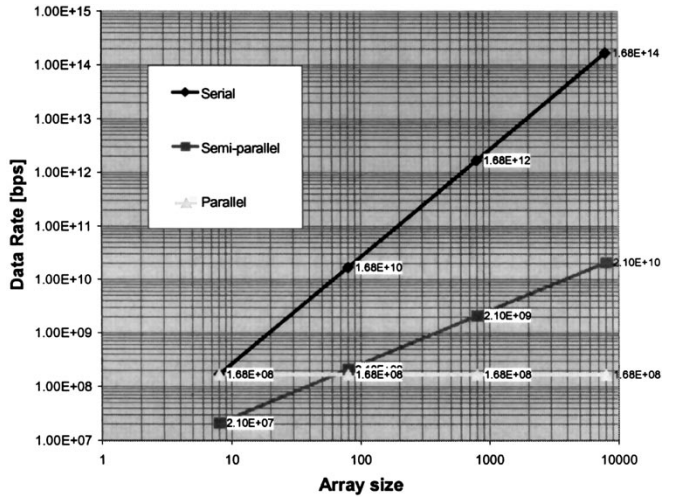
A readout speed comparison for different architectures is instructive. Fig. 3 shows simulation results of the readout data rate as a function of bits per pixel resolution and array size for the three different FPA architectures: serial, semiparallel, and fully parallel. Fig. 3(a) shows how scaling of the bits per pixel resolution affects data rate. It was derived using the following assumptions: the array size was 1000×1000; the frame rate of the system was 100 kf/s; and 8×8 detector arrays were used for processor subarrays in the fully parallel system. For 8 bits per pixel, these assumptions dictate the readout rate of the first-order sigma–delta ADC: 167 Mb/s for a parallel system, 2.62 Gb/s for a semiparallel system, and 2.62 Tb/s for a serial readout system. For all systems, the data rate increases when the bits per pixel goes to 12 bits, however, the fully parallel system rate is approximately 1 Gbps, compared to 16 Gb/s for semiparallel, and 16 Tb/s for serial readout.

Fig. 3(b) shows the effect of scaling imager size on data rate, assuming a fixed 8-bit resolution, 100-kHz frame rate, and different array sizes. The bandwidth of the parallel system is independent of the array size. However, the semiparallel and serial readout system bandwidths exponentially increase with array size. From the simulation results, the semiparallel readout system had superior bandwidth compared to the parallel readout system when it was smaller than a 64×64 array size. However, beyond that array size the fully parallel system is superior. For the case of $10\,000 \times 10\,000$ images (a goal of many scientific imaging systems), there is a 100 times improvement in data rate for the fully parallel system over the semiparallel system, and a million times improvement over the serial system.

To compare the bandwidths of the readout systems, it was assumed that the same type of A/D converter was used for different readout systems. This assumption would not produce an optimal system if there were no area and power consumption restrictions. For the semiparallel readout system, it is a more optimal solution to use second-order sigma–delta ADC's rather than first-order sigma–delta ADC's so long as a large area is available. By using second-order sigma–delta ADC's, the oversampling ratio can be decreased significantly [13]. Likewise, for serial readout systems, there is no limitation in choosing an ADC type. In the following simulations, a second-order sigma–delta A/D converter was used in the semiparallel and serial FPA's for comparison. All of the other assumptions were the same as previously stated.



(a)

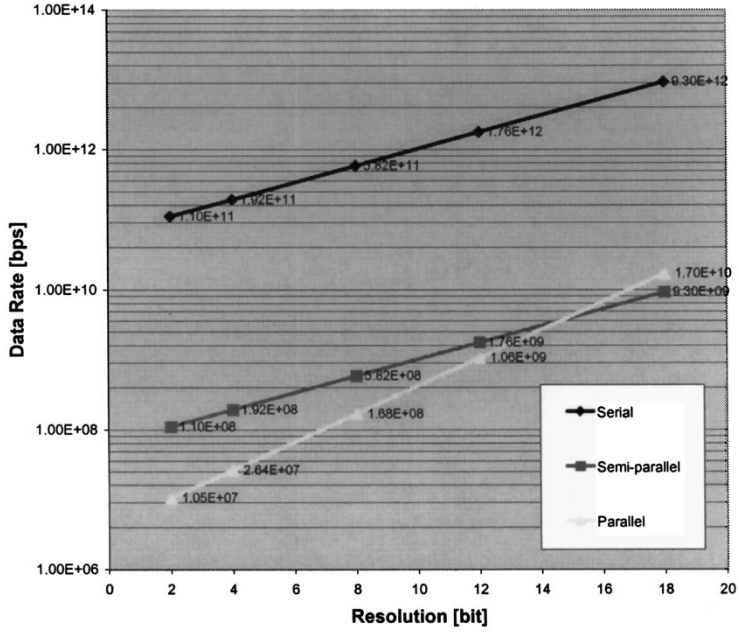


(b)

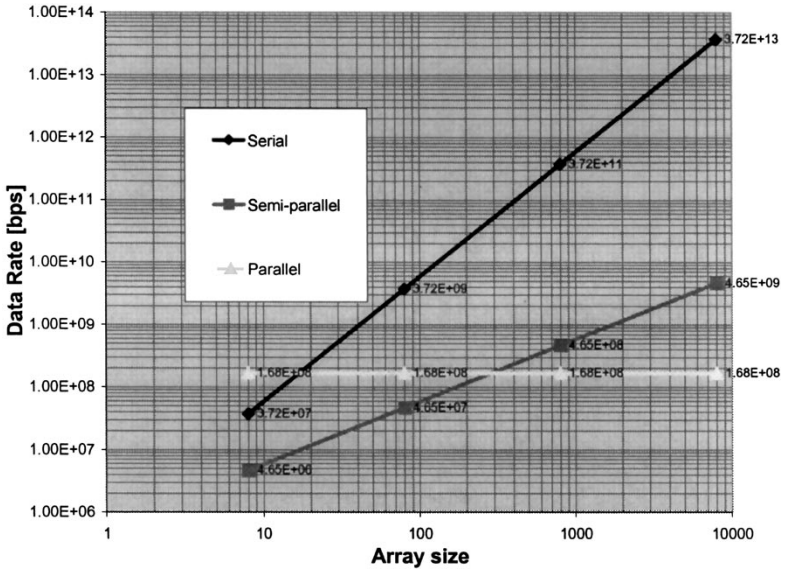
Fig. 3. Readout system bandwidths. (a) Data rate versus resolution. (b) Data rate versus array size.

Fig. 4(a) is an interesting simulation result showing bandwidth as a function of resolution for a 1000×1000 pixel imager. At resolutions over 15 bits, the semiparallel readout system with the second-order converter resulted in less bandwidth compared to the parallel readout system with the simple first-order converter (although the 4-GHz bandwidth required in the semiparallel case demands a currently impossible ADC design at 15-bit resolution). Fig. 4(b) shows another interesting simulation result: the semiparallel readout system is better for array sizes under 288×288 provided that a signal processor supports each row.

Thus, for low resolution and large image arrays, the parallel readout system has the best performance for relatively low resolution (8 bit) and large image arrays. In the next sections, the design, implementation, and test results from an 8×8



(a)



(b)

Fig. 4. Readout system bandwidths with different ADC's. (a) Bandwidth as a function of resolution. (b) Bandwidth as a function of array size.

Si CMOS integrated detector/sigma–delta ADC array will be presented.

III. Sigma–Delta ADC's

Modern short-channel CMOS processes offer a speed performance which is often far beyond system requirements. Speed will continue to improve as shorter channel lengths are available in the future. Accuracy and the component matching, however, are expected to become worse with decreasing line width. For a fully parallel FPA system, this is a potentially serious problem because there are thousands of ADC's working together, which necessitates good device uniformity to produce a uniform image. Hence, it is an advantage to tradeoff speed for accuracy, thus resulting in a flexible system which enables access to higher accuracy at the cost of speed degradation. This tradeoff can be realized using an oversampling converter, which is an ADC that trades off speed and component mismatch. An example of one such ADC is a sigma–delta current input first-order modulator. The simplified architecture of this ADC is shown in Fig. 5. The blocks that make up the system will now be briefly described.

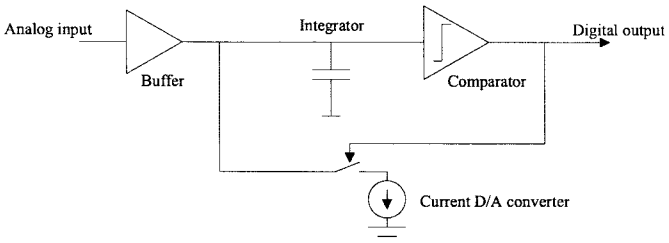


Fig. 5. First-order oversampling modulator.

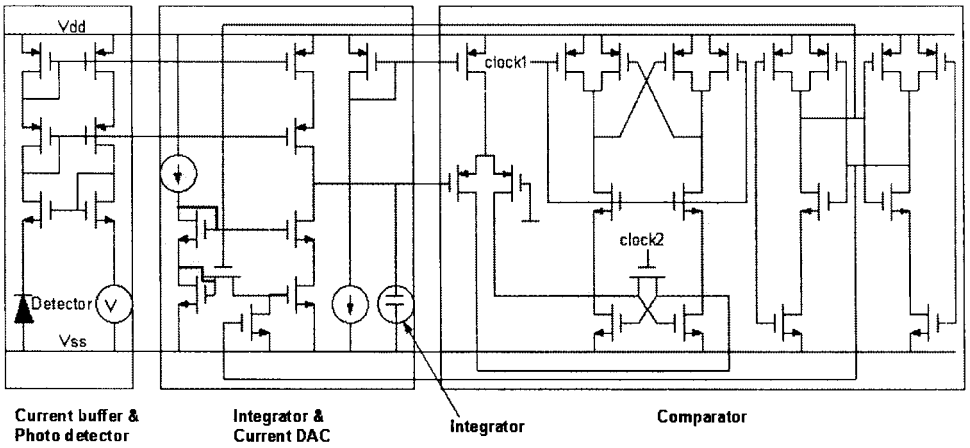


Fig. 6. First-order oversampling modulator with current buffer.

In the smart FPA application discussed herein, a current buffer is needed between the photodetector and oversampling modulator. The proposed parallel readout system uses a current buffer as the front end of the readout circuit to provide low input impedance and a stable bias to the detector. A current buffer typically must provide a low-input impedance to reduce the effects of the nonzero output admittance of the detector. It must also supply a specified dc bias voltage for the input device to improve the linearity of the detector. The output of the current buffer is connected to a current integrator (capacitor) and to a one bit digital-to-analog (D/A) converter (a current source and a switch). The integrator output (voltage) is fed to a clocked comparator that produces the digital output of the front end, and operates the D/A converter to maintain the level of the integrator below the comparator threshold. A simple understanding of the operation of the front end can be achieved when one realizes that the output is a pulsewidth modulated version of the analog input and can be digitally filtered to recover the analog value. However, the spectral properties of this particular pulsewidth modulated output are such that the quantization noise is predominantly at higher frequencies, so that higher bandwidth filters can remove it, which is in contrast to a signal produced by, for example, a dual slope converter. This results in higher data rate operation for the same resolution. In addition, the output digital value is set only by the value of the input and the D/A current source, not the capacitor, and this makes the converter immune to process variations in the capacitor value.

Fig. 6 shows the detailed schematic of the first-order modulator circuitry. The detector bias is controlled by the bias voltage source "V," and this is shared with the other pixels. The current source "I" is generated from a current mirror also shared by all of the other pixels. The current buffer uses a feedback loop to maintain the detector bias at the same value as the voltage source "V." The current DAC converter is realized with a current mirror and two switch transistors that enable or disable the current mirror. The current integrator is implemented with a capacitor whose value is set to prevent nonlinear clipping at desirable maximum input signal sizes and minimum operating speeds. The comparator, which compares the integrator voltage and a reference voltage, produces the one bit output data stream [14]. The two clocks determine the comparison time and the time at which data is valid. The comparator consists of a positive feedback differential amplifier and a data latch. The digital output of the comparator would be decimated and filtered by the subsequent signal processor on the next layer of the 3-D stack. The comparator output is also fed back to the DAC to control the DAC feedback current, which makes the comparator output average track the input.

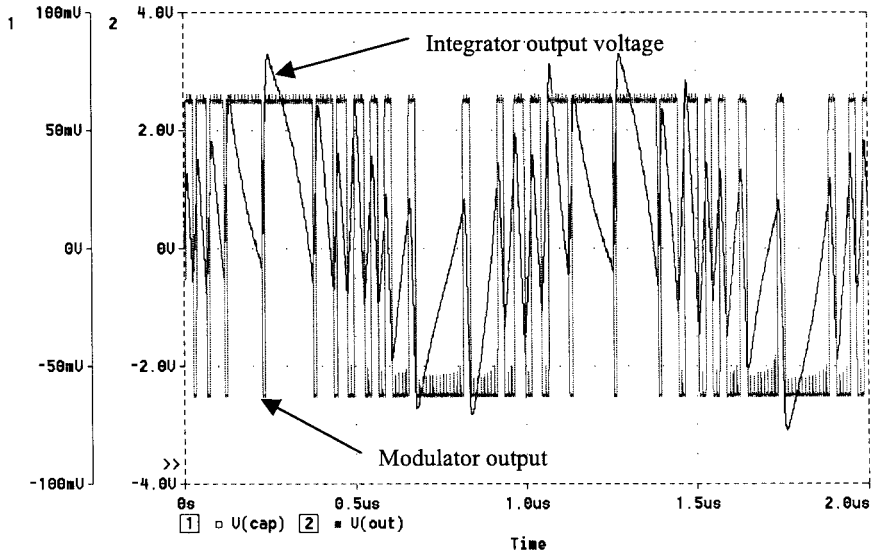
Fig. 7 shows SPICE simulation results with a 50-kHz 2-μA sinusoidal input. The comparator clocks are running at 1.6 MHz for an oversampling ratio of 16 times the Nyquist rate. Fig. 7(a) shows the integrator voltage and the modulator digital output. The integrator voltage does not exceed 800 mV and did not saturate with maximum input current, indicating that the 800 fF used is a good capacitor value choice. When the integrator voltage crosses 0 V, the comparator switches state on the next clock signal. This turns on the DAC current, which stays on for as many clock cycles as is required for the integrator voltage to cross zero again.

The power density function (PDF) of the output digital data is shown in Fig. 7(b). Consistent with sigma–delta modulator properties, the quantization noise is "bunched" at higher frequencies. The 50-kHz sine wave signal can be clearly seen in the binary data stream and is more than 40 dB above the adjacent noise, which is equivalent to more than 6 bits of resolution.

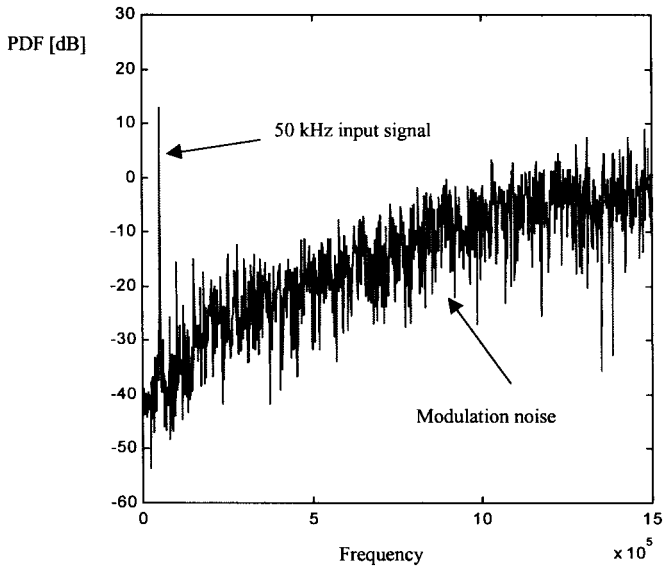
Fig. 8 shows the layout and photomicrograph of the modulator circuits for each FPA pixel. All of the circuits, including the data lines and detector, were laid out to fit into a 125 μm $\times$ 125 μm area. The design of compact circuits was essential so as to enable a large detector and capacitor. All surfaces except the detector were later covered by metal to prevent extraneous current generation in the circuit area.

IV. CMOS Image Sensor

To integrate the detector imaging array onto the silicon circuitry, there are two options that can be explored: a hybrid integrated detector array [15] and a monomaterial detector [16]. The advantages of the hybrid detector are a higher fill factor since the detectors can be integrated directly on top



(a)



(b)

Fig. 7. First-order oversampling modulator simulation results. (a) Integrator and output nodes voltages. (b) Power density function.

of the circuitry, and independent optimization of the detector and the circuitry. Thus, the performance of the array can be significantly improved, but the system cost is higher since there is an assembly cost associated with the hybrid integration. The other image sensor that can be used accesses monomaterial integration for the detector, i.e., implementing the detector directly in the Si CMOS. The responsivity and wavelength of operation are limited, as is the fill factor, however, for many applications, the use of Si detectors is adequate. CMOS-based image sensors offer the potential opportunity to integrate a significant amount of VLSI electronics on chip, and reduce component and packaging cost. A number of types of Si CMOS photodetectors have been reported in the literature including photodiodes and phototransistors. In this paper, a photodiode was used for the photodetector instead of a phototransistor because the photodiode has better linearity and speed, although it is less sensitive [17].

The photodiodes were realized using a standard 0.8-μm n-well CMOS process through the MOSIS foundry. The physical size of the photodiode was restricted to 60 μm $\times$ 77 μm, because the pixel space was shared with the circuits and data lines. To increase the speed of the detector, four parallel photodiodes were used rather than one larger photodiode to reduce the parasitic capacitance. The schematic, cross section, and layout of the photodetectors are shown in Fig. 9.

V. System Test Results

To verify that the system was working properly, a test image with a laser source was used to project a simple image onto the FPA's. The He:Ne laser output was focussed by a lens onto the 8 $\times$ 8 detector array FPA chip, and the position of the spot was varied by changing the chip position. Data from the system was collected using a 16-bit ISA data acquisition card in two different systems. A 50-MHz 486 PC acquired

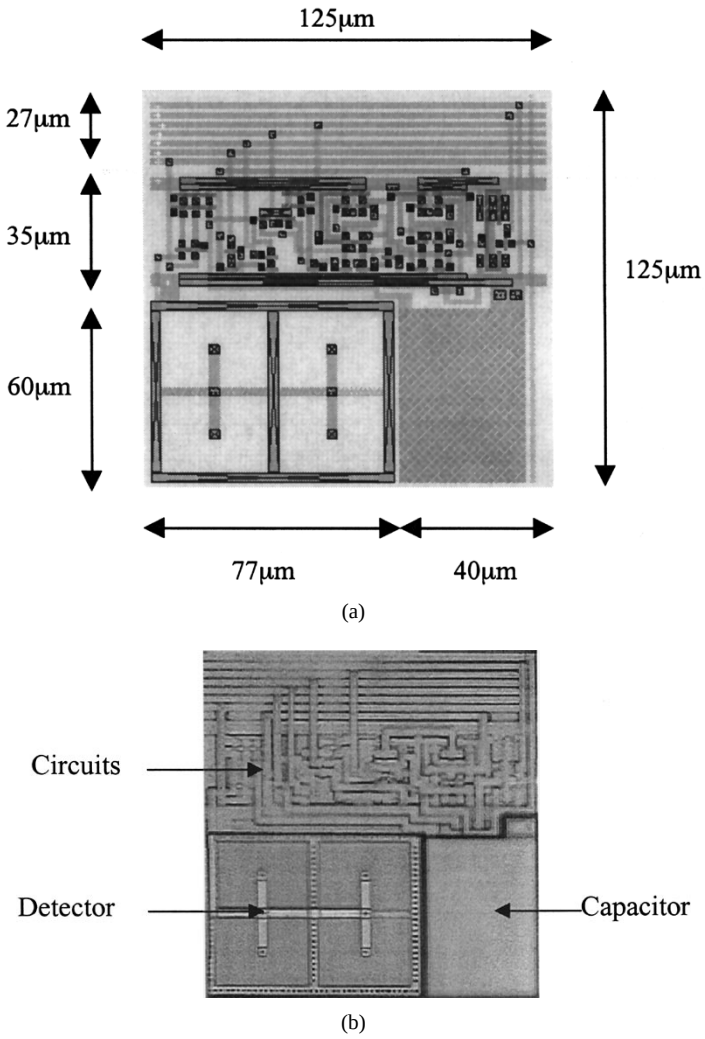


Fig. 8. Layout and photomicrograph of a single integrated detector/ADC pixel. (a) Single integrated detector/ADC pixel: Layout. (b) Single integrated detector/ADC pixel: Photomicrograph.

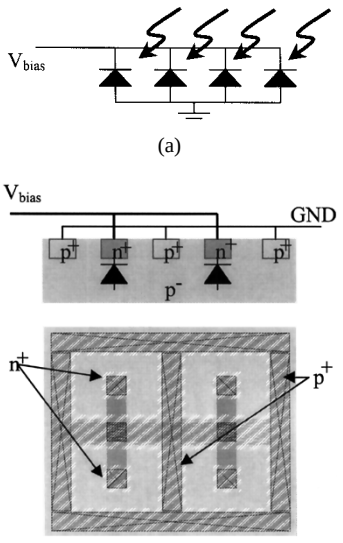


Fig. 9. Monolithically integrated Si CMOS photodetectors. (a) Schematic of each photodetector pixel. (b) Layout.

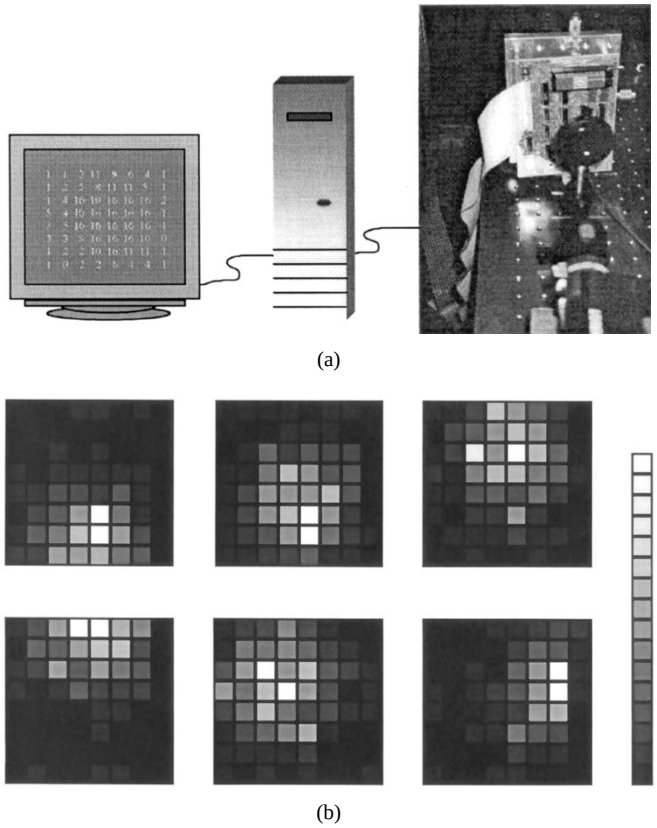


Fig. 10. FPA functional test. (a) Test setup. (b) Computer screen images (resolution: 4 bits; frame rate: 3.9 kf/s).

data at 200 kHz, while a 233-MHz Pentium acquired data at 1 MHz. The focal plane array operation frequency was limited by the acquisition rate of the test system.

Fig. 10(a) is an— illustration of the data acquisition system with a photograph of the test setup. In the photograph at right, the laser, lens, and a patterned image are shown. The chip could be translated in the x, y, and z directions. The output was displayed on the monitor after averaging the output data. The averaging is a function of the filter implemented on the DSP, and can be varied to tradeoff resolution and speed. This adaptability is a particular strength of sigma–delta ADC's. Fig. 10(b) shows several images taken with a 1-MHz clock rate, and the PC filtering by averaging 16 samples to get 4-bit resolution at a frame rate of 976 Hz. The data on the screen, as shown in Fig. 10(a), were numerical values with an approximately linear relationship between the detected optical intensity and the numerical value. In Fig. 10(b), data are presented for the laser spot in various spatial locations on the FPA. The most highly illuminated pixel was colored white, and the darkest pixel was colored black, with gray scale between the two extremes of illumination.

Uniformity is one of the important characteristics of an imaging system. To get a good quality image with a minimum of correction needed, all detectors and their associated circuitry need to respond to optical input uniformly. To measure the uniformity of the system described herein, a test was run with the readout system running at 1 MHz, and the PC filtering the data by averaging 64 images (the maximum possible at 1 MHz without PC interrupts due to Windows 95 operation) resulting

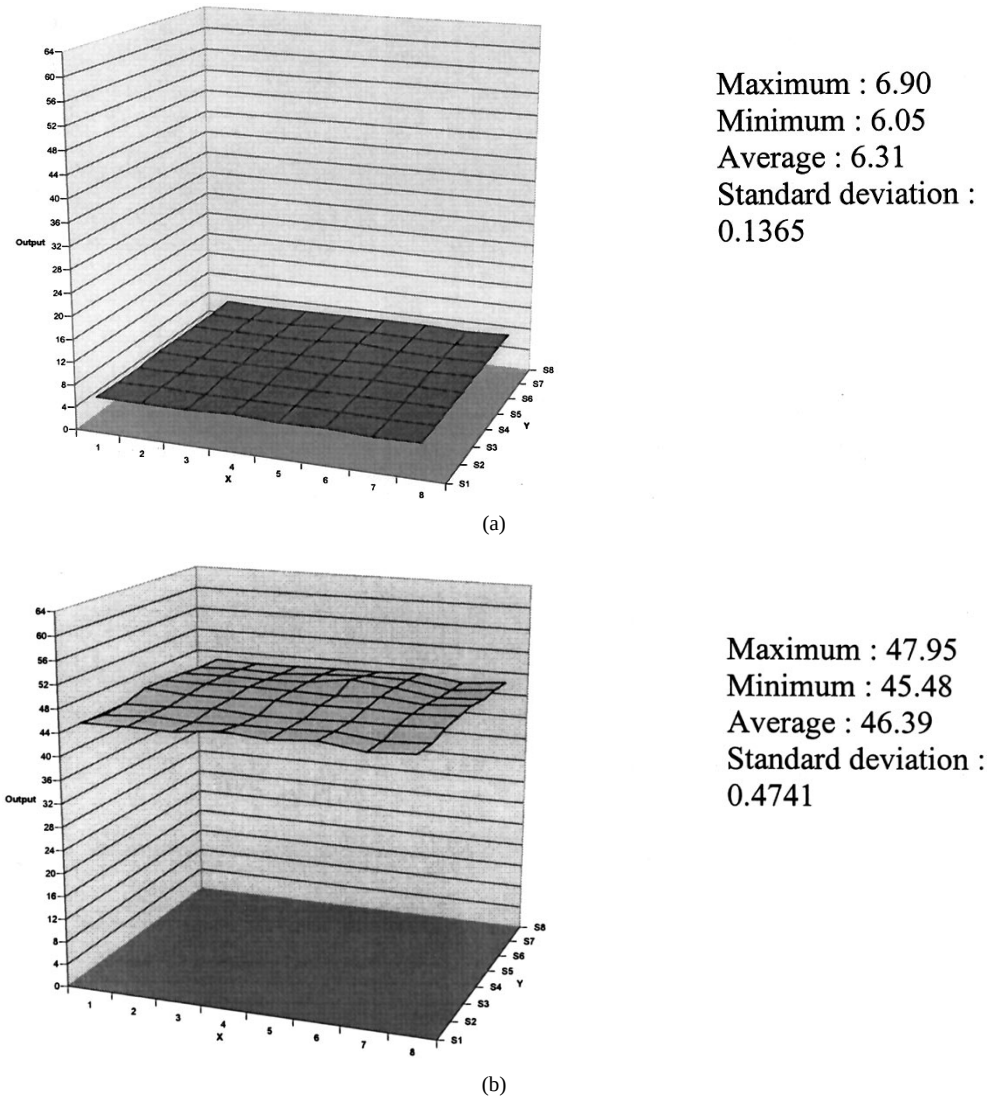


Fig. 11. Uniformity test results. (a) Low optical input intensity. (b) High optical input intensity.

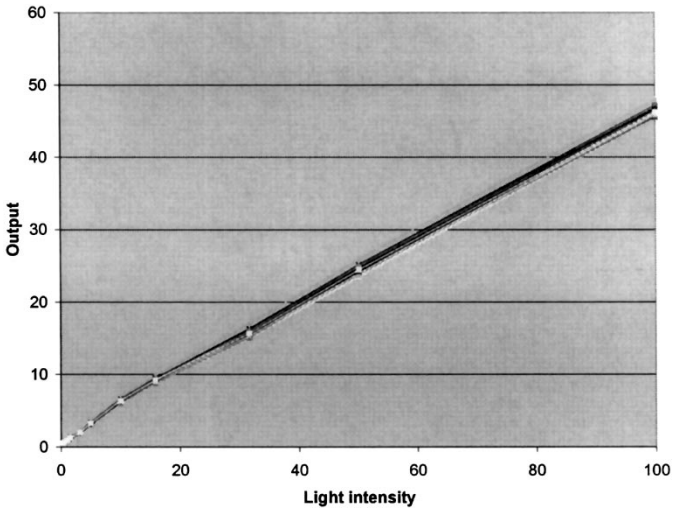
in 6 bits maximum achievable resolution, (i.e., quantization noise will limit the resolution to 6 bits). An uncalibrated halogen light source which was large in comparison to the FPA size was used to illuminate the FPA from a distance of 3 m to produce a uniform intensity across the FPA.

Fig. 11 shows the test results of FPA uniformity for (a) low- and (b) high-light intensity. The standard deviation among the pixels was calculated to measure the uniformity. Twelve different light intensity values were used to measure the uniformity, and all showed good standard deviation across the array. Table I shows the measured standard deviation for all 12 different optical input intensities. The test results included all noise sources from the detector and circuits. These test results show that the standard deviation increases as a percentage of full scale with increasing input intensity. However, since the standard deviation is always less than 0.74% of full scale, this indicates a probability of better than 97.7% of 6 bits of accuracy in the output (the maximum achievable), assuming normally distributed pixel variations. The optical intensity was controlled using neutral density filters to generate outputs between 0–64. The last test result in Table I was not meaningful because the circuit was saturated (too much photocurrent). The optical input intensity is reported as a percentage of the maximum incident optical input. When the optical input was more than 15% of maximum, the output was saturated.

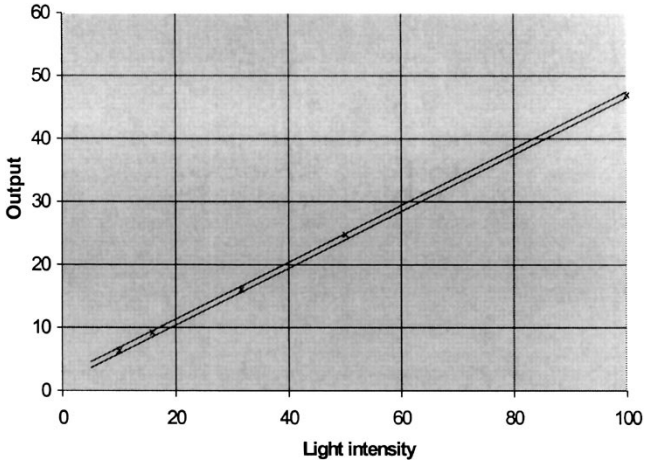
Photodetector linearity was tested with the halogen optical source and four neutral density filters. By combining the four optical filters, 16 different optical input intensities were measured. However, the circuit was saturated with 5 out of 16 light intensities, and they were removed from the evaluation. Fig. 12(a) shows the linearity of all 64 of the pixels and Fig. 12(b) shows a single pixel and 6-bit resolution lines. Over the majority of the range of the input optical intensities, 6-bit linearity was achieved, as expected.

VI. Conclusion

In this paper, a scalable fully parallel optical readout system for focal plane arrays is proposed. System level simulations indicate that the proposed readout system has an advantage over semiparallel or serial readouts when it is used for high



(a)



(b)

Fig. 12. Linearity test results. (a) Data from all 64 pixels. (b) Single pixel, with 6-bit resolution lines.

TABLE I
UNIFORMITY UNDER DIFFERENT OPTICAL INPUT INTENSITIES

Light Intensity	Maximum pixel output (max = 64)	Minimum pixel output (max = 64)	Average pixel output (max = 64)	Standard Deviation	Standard Deviation % of full scale
0.0316%	0.62	0.48	0.52	0.0217	0.03%
0.0501%	0.66	0.52	0.56	0.0225	0.04%
0.1%	0.96	0.74	0.79	0.0343	0.05%
0.158%	1.38	1.12	1.18	0.0390	0.06%
0.316%	2.22	1.85	1.95	0.0579	0.09%
0.501%	3.55	3.02	3.18	0.0854	0.13%
1%	6.90	6.05	6.31	0.1365	0.21%
1.583%	9.90	8.74	9.11	0.1965	0.31%
3.16%	16.97	15.02	15.68	0.3385	0.53%
5.01%	25.95	23.46	24.44	0.4273	0.67%
10%	47.95	45.48	46.39	0.4741	0.74%
*15.83%	62.83	62.29	62.56	0.1073	0.17%

* Saturated

frame rates (100 kf/s or more), large image array sizes (more than 256 $\times$ 256), and medium resolution (less that 15 bits per pixel). To achieve a 100 kf/s, 10 000 $\times$ 10 000 8-bit imager, the fully parallel system can run nearly 30 times slower than a semiparallel realization, and more than 2000 times slower than a serial imager.

To realize this parallel readout system, a compact size first-order current input sigma–delta modulator has been designed that will fit in each pixel in an imaging array. An 8 $\times$ 8 detector array section with an ADC front end dedicated to each pixel has been implemented and tested in Si CMOS. Test results on the FPA tile indicate good array uniformity and linearity.

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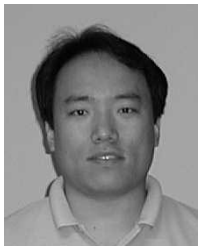

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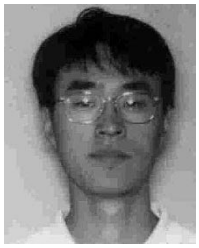

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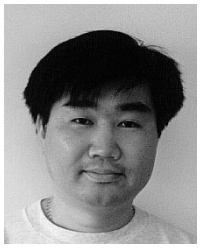

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Martin A. Brooke (S'85–M'86), for a biography, see this issue, p. 285.

Nan Marie Jokerst (S'83–M'88–SM'98), for photograph and biography, see this issue, p. 144.

D. Scott Wills (S'80–M'83–SM'98), for photograph and biography, see this issue, p. 285.