

A Three-Layer 3-D Silicon System Using Through-Si Vertical Optical Interconnections and Si CMOS Hybrid Building Blocks

Steven W. Bond, Olivier Vendier, Myunghee Lee, *Member, IEEE*, Sungyong Jung, Michael Vrazel, *Student Member, IEEE*, Abelardo Lopez-Lagunas, *Member, IEEE*, Sek Chai, Georgianna Dagnall, Martin Brooke, *Member, IEEE*, Nan Marie Jokerst, *Senior Member, IEEE*, D. Scott Wills, *Senior Member, IEEE*, and April Brown, *Fellow, IEEE*

Abstract— We present for the first time a three-dimensional (3-D) Si CMOS interconnection system consisting of three layers of optically interconnected hybrid integrated Si CMOS transceivers. The transceivers were fabricated using 0.8- μm digital Si CMOS foundry circuits and were integrated with long wavelength InP-based emitters and detectors for through-Si vertical optical interconnections. The optical transmitter operated with a digital input and optical output with operation speeds up to 155 Mb/s. The optical receiver operated with an external optical input and a digital output up to 155 Mb/s. The transceivers were stacked to form 3-D through-Si vertical optical interconnections and a fabricated three-layer stack demonstrated optical interconnections between the three layers with operational speed of 1 Mb/s and bit-error rate of 10^{-9} .

Index Terms— Optical interconnect, 3-D integration.

I. INTRODUCTION

ONE LIMITATION in the development of sophisticated smart pixel systems lies with the interconnection of the pixels to advanced processing circuitry. Often, the limited Si area under or surrounding each pixel is insufficient for high levels of VLSI signal processing. One possible solution is to increase the die size and maintain the pixel dimensions to allow more processing on the same circuit plane as the pixel array, but this approach is unacceptable because it decreases the fill factor of the associated image array. A better solution would be to develop three-dimensional (3-D) interconnections from the image array to subsequent advanced processing layers. This is essentially an interconnection problem, which also plagues electronic systems.

Manuscript received November 5, 1998; revised April 9, 1999. This work was supported by the Army Missile Command under Contract DAAH01-92-D-R005, by the National Science Foundation (NSF) under Contract ECS9422452, by the NSF Packaging Research Center under Contract EEC9402723, and by the Air Force Office of Scientific Research under Contract F49620-95-1-0246.

S. W. Bond was with the School of Electrical and Computer Engineering, Microelectronics Research Center, Packaging Research Center, Georgia Institute of Technology, Atlanta, GA 30332-0269 USA. He is now with Lawrence Livermore Laboratories, Livermore, CA.

O. Vendier, M. Lee, S. Jung, M. Vrazel, A. Lopez-Lagunas, S. Chai, G. Dagnall, M. Brooke, N. M. Jokerst, D. S. Wills, and A. Brown are with the School of Electrical and Computer Engineering, Microelectronics Research Center, Packaging Research Center, Georgia Institute of Technology, Atlanta, GA 30332-0269 USA.

Publisher Item Identifier S 1077-260X(99)06062-1.

Research into the next generation of Si CMOS electronic systems, termed giga-scale integration (GSI), has suggested that the operational speed of CMOS-based systems will be limited not by the devices, but instead, by the interconnections between devices [1]. Furthermore, the Semiconductor Industry Association (SIA) Roadmap for 1997 identifies CMOS interconnection technology for the year 2009 and beyond as a critical technology to develop to continue traditional performance scaling of CMOS technologies, but they do not identify a current technology which will satisfy the interconnection need [2]. The Roadmap goes on to suggest 3-D devices and architectures, and employing on and off-chip optical interconnects as possible solutions to the communication bottleneck anticipated at CMOS linewidths below 70 nm.

The 3-D CMOS architectures with optical interconnections enable the development of advanced smart photonic systems and can alleviate the electrical interconnection limitations of future CMOS technologies [3], [4]. Although materials research is providing improvements in electrical interconnects by utilizing advanced materials (aluminum and standard SiO_2 are being replaced with copper and titanium nitride [5]), optical interconnections can provide high-speed low-loss massively parallel crosstalk resistant communication, enabling 3-D processing system topologies suitable for chip-to-chip, chip-to-board and board-to-board applications [6], [7].

Massively parallel applications such as image processing, image generation, and routing can be mapped into architectures which are well suited to 3-D interconnection structures. These architectures, which utilize multiple processors, are systems that could benefit from 3-D interconnections, as illustrated in Fig. 1. The latency associated with planar high density interconnections does not scale as the size of the system increases; latency problems are exacerbated with increasing system size. If a large number of processors on a planar substrate [$32 \times 32 \times 4$ shown in Fig. 1(a)] were arranged into a 3-D topology using vertical optical interconnections, as shown in Fig. 1(b), the interconnection power dissipation and communication delay (latency) between subsections would be substantially decreased [8]. Another system that can benefit from vertical optical interconnections is a highly parallel image processor discussed in [9]. This system utilizes an offset cube topology of 4096 similar processors vertically

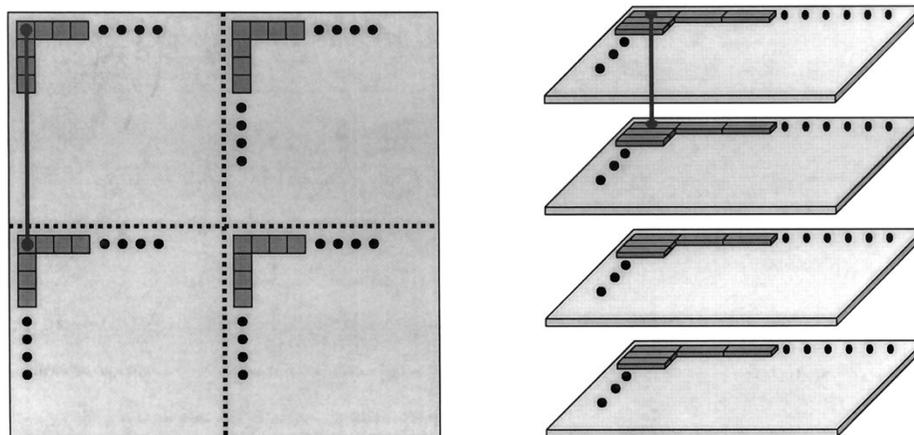


Fig. 1. System which could benefit from through-Si vertical optical interconnections.

interconnected to processing planes above and below the processor. Simulations of a $16 \times 16 \times 16$ system indicate that it could perform image computations with an aggregate data throughput of 819.6 Gb/s.

Vertical electrical interconnection of circuitry has been investigated using Al thermomigrated feedthroughs through Si substrates to connect the front and back of each substrate [10]. These Si substrates, which included functional circuitry, were then stacked and connected using microbridges that connected the facing wafer planes. Heat dissipation limited operation to a single layer in the demonstrated five-layer stack. This heat dissipation problem is alleviated when optical interconnections are used, since simple point-to-point optical interconnections are unaffected by the flow of either liquid or gaseous coolant. The index of refraction changes caused by mixing and convection will not significantly refract the beam path, however, large index of refraction changes caused by gas bubbles should be avoided in the flow. Thus, vertically optically interconnected 3-D electrically connected systems, since the optically interconnected systems need not be mechanically linked for electrical conduction between the layers.

Vertical optical communication through Si circuits for 3-D interconnections was first posited using an external solid-state laser operating at $\lambda = 1.3 \mu\text{m}$. Since then, three different demonstrations of vertical optical communication through stacked Si substrates have been reported in the literature [12]–[14]. The first technique utilizes advanced GaAs-based emitters flip-chip bonded to the Si circuits. Unfortunately, optical absorption for this through-Si link is high because the emission energies of these devices is larger than the bandgap of Si, ($E_g(\text{Si}) = 1.0 \text{ eV}$, $\lambda_g = 1.1 \mu\text{m}$) [15]. To achieve low-loss propagation in this system, the use of laser drilled free-space waveguides through the host substrates is required [12]. The second demonstration utilizes three GaAs-based vertical-cavity surface-emitting lasers (VCSEL's) ($930 \text{ nm} < \lambda < 950 \text{ nm}$) for multiple wavelength reconfigurable communication to three separate substrates containing flip-chip bonded multiple-quantum-well (MQW) detectors. The emitters in this demonstration are all located at the same plane and operate at wavelengths that experience absorption through the substrate. The novelty of this system is that it allows a single

source plane and the option to choose the individual receiver plane by choosing the wavelength [13]. The third method utilizes integrated InP-based optoelectronic devices operating at $\lambda > 1.2 \mu\text{m}$ bonded directly to Si circuits. This technique has been used to produce two layer through-Si CMOS vertical optical interconnections [14], [16], [17].

To access high-yield low-cost VLSI for complex signal processing functions, the development of CMOS analog optoelectronic (OE) interface building blocks and the integration of OE devices with digital CMOS VLSI are critical. Parallel CMOS receivers have been demonstrated with electrical gigabits per second operation (not integrated with OE devices) [18]. Optoelectronic device integration with foundry digital Si CMOS, and the independent optimization of the CMOS and the OE devices, have been attempted with both monomaterial and hybrid integrated approaches. Si optoelectronic devices for monomaterial integration have been studied and are under development, however, Si CMOS detectors operate at short wavelengths (below $\lambda = 950 \text{ nm}$) with low responsivity or low speed, and emitters have only been demonstrated with weak optical emission through defect centers [19]. Efficient through-Si optical interconnections require technologies that allow independent optimization of long wavelength optoelectronics and CMOS processing circuitry, which obviate the use of currently reported Si optoelectronic devices.

One method of combining optoelectronic (OE) materials with highly integrated circuits utilizes hybrid epitaxial growth of III–V optoelectronic materials directly onto Si circuitry. These devices reported in the literature suffer from short lifetimes and low efficiencies due to mismatches in lattice constants and coefficients of thermal expansion [20], or the CMOS is damaged by the growth process [21], although there have been reports of hybrid growth success for modulators on Si substrates [22]. Other hybrid integration technologies, such as flip-chip bonding or thin-film integration, enable the independent optimization, fabrication, and testing of the optical and electronic components prior to bonding. Flip-chip technologies align and attach optical substrates to Si substrates using metal (usually indium-based) bump bonds, but retain the substrate (and the optical losses associated with the substrate), and have limited scalability in the vertical

dimension. The assembly for mixing and matching individual devices or small areas of devices on circuits using bump bonding is also problematical. In contrast, thin-film hybrid integration enables independently optimized devices (typically less than $5\ \mu\text{m}$ thick) to be selectively aligned and bonded to the host substrate using a transparent transfer diaphragm [23]. This results in a virtually planar hybrid integrated optoelectronic circuit (OEIC), and enables vertical scalability, the mixing and matching of independently optimized multiple OE devices with circuits, and the use of standard microfabrication techniques. Recent results also indicate that thin-film hybrid integration using metallic bonding (in this case, bump bonding) yields high levels of hybrid integration [24].

The 3-D optical links described herein can be used to implement a true 3-D computational mesh, which may ultimately yield effective massively parallel computational systems. For example, a $32 \times 32 \times 4$ processor system using the simple LED link described in this paper would yield a 12-in² module. The transmission media latency, based upon the speed of light, is less than 3 ps (negligible) for adjacent processor/processor communication from layer to layer in any size system. The transceiver circuits and emitter/detector delay will dominate the optical link latency. However, the power consumed in the LED-based network is prohibitive. With LED's, the theoretical $32 \times 32 \times 4$ system would use 60 kW of power for interconnect alone [25]. Although longer wavelength ($>12\ \mu\text{m}$) VCSEL's are in their infancy, one can, based upon GaAs-based VCSEL's, forecast that, using a 20- μm diameter 1-mA-threshold VCSEL that a nearly 14 times improvement in the coupling efficiency is predicted. Reasonably assuming operation at 600 Mb/s with a power dissipation of 5 mW per link, and by conservatively assuming a factor of 10 improvement in the coupling efficiency, the optical interconnect power for the $32 \times 32 \times 4$ processor system drops to approximately 250 W with VCSEL's [25]—a factor of 240 times improvement over the LED-based system, and a power dissipation level that can easily be handled with standard ethylene glycol liquid coolant.

In this paper, the development of hybrid integrated optoelectronic transmitter and receiver building blocks in digital Si CMOS with operational speeds up to 155 Mb/s is reported. These building blocks are individually characterized and assessed for implementation in a three-layer system. The hybrid Si CMOS optoelectronic transceivers are then physically stacked into a three-layer system to demonstrate the first 3-D vertically optically interconnected CMOS three-layer communication system using through-Si vertical optical long wavelength interconnections.

II. SYSTEM DESIGN

To demonstrate a 3-D CMOS system with vertical optical interconnections requires careful selection of suitable subsystem components for operational speeds to 155 Mb/s. The analog CMOS receiver and transmitter circuits used scalable designs for implementation in digital Si CMOS processes and were optimized for minimum power dissipation at the operational speed. Long wavelength InP-based optoelectronic

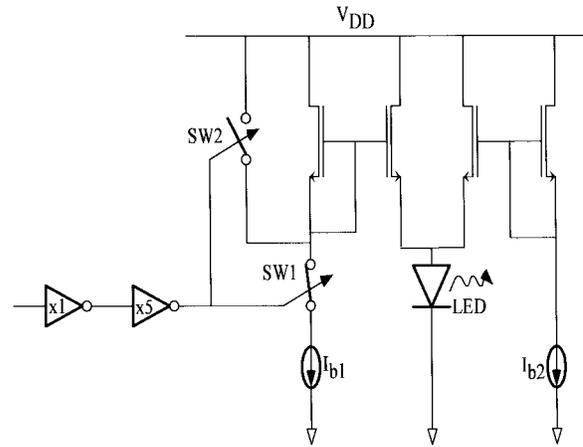


Fig. 2. Single-ended CMOS transmitter design.

devices with various sizes and configurations were used to enable characterization of the devices integrated with the CMOS analog interface circuitry. This section describes the design of the analog circuitry and optoelectronic components. The next section presents the measured characteristics of the different integrated designs that were used to determine the best system combination for the through-Si optical interconnection.

A. Analog Optoelectronic Interface Circuit Designs

1) *Transmitter Design:* The digital CMOS transmitter circuit described herein was optimized to meet the SONET OC-3 speed specification of 155 Mb/s while minimizing power consumption. The driver circuit was also designed to provide up to 80 mA of output current to the emitter, and consists of two tapered inverters, a current switch, and a current mirror, as illustrated in Fig. 2. The transmitter was fabricated through the MOSIS foundry in a 0.8- μm standard digital Si CMOS process. The two-stage tapered buffer input is designed to minimize power consumption at high speeds and begins with a minimum geometry inverter used to drive a current switch. The inverter multiplication ratio is dictated by the tradeoffs between speed, power, and chip size. The maximum speed is obtained when the ratio is 3, but this results in high-power dissipation. However, if the ratio is changed from 3 to 5, there is a slight decrease in the speed, but also a significant decrease in power dissipation.

To avoid large voltage spikes and signal distortion in the output, the current switch was not used in the final stage of the amplifier. Instead, the current switch was connected before the power transistor stage to produce fast rise and fall times. The output stage did, however, include a current mirror for dc biasing of the emitter. Normal operation of the circuit begins with the emitter off, when switch SW1 is open (on) and SW2 is closed (off). To modulate the emitter to the on state, SW1 is closed and SW2 is opened. For fast circuit recovery to the emitter off state, node N2, which has a large capacitance due to the size of the power transistors (M1 and M2), is quickly discharged through SW2. Careful layout of this circuit was necessary to minimize series resistance in the output power transistors, to minimize noise introduced onto the input signal,

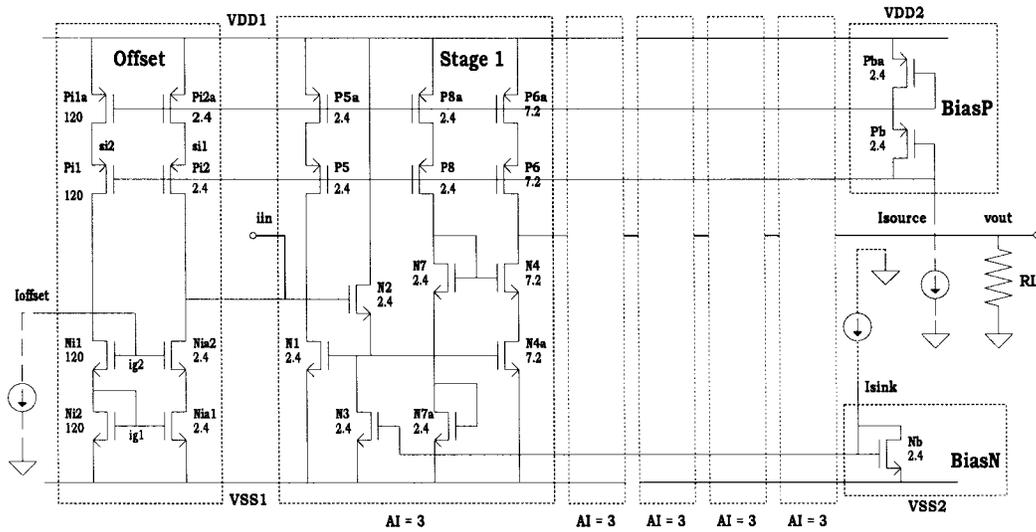


Fig. 3. Five-stage single-ended CMOS receiver design.

and to ensure the use of metal lines that were large enough to prevent thermal problems and electron migration.

2) *Receiver Design*: The transimpedance amplifier was designed for scalability and fabricated through the MOSIS foundry in a $0.8\text{-}\mu\text{m}$ standard digital Si CMOS process [26]. For wide bandwidth, a multistage low-gain-per-stage open-loop configuration was used [27]. The amplifier circuit, shown in Fig. 3, consists of five identical stages, an offset circuit, and a comparator. Each stage has a current gain of 3, which gives a total amplifier current gain of 243. The input offset correction circuitry is a current attenuator, which allows very small currents to be applied to the input of the amplifier to correct for current offset. The complete amplifier circuit was designed to drive an on-chip clocked comparator to convert the analog amplifier output to a digital signal [28].

B. Optoelectronic Device Design and Integration with CMOS Circuits

1) *Emitter Design*: The optimal emitter for a through-Si link is a device capable of high-output powers, high speed, and low divergence angle. VCSEL's would be an optimal choice, however, long-wavelength VCSEL's are still in development, with the first continuous-wave (CW) demonstration in 1995 [29]. Light-emitting diodes (LED's) have demonstrated high reliability, are low cost, and simple to fabricate, and can operate at the desired modulation speeds (155 Mb/s) with good internal quantum efficiency. Although the divergence angle of LED's is large, which implies reduced coupling under the condition of no misalignment, this large divergence also results in a high level of alignment tolerance for the packaged through-Si link.

Three LED designs were integrated onto Si CMOS transmitter circuits and evaluated for use in the three-layer through-Si interconnection system. To minimize absorption loss within the Si, all designs centered on a wavelength of $\lambda = 1.3\ \mu\text{m}$, at energies smaller than the Si bandgap. The first design, E1, was a $250\ \mu\text{m}$ on a side square device implemented in the InGaAlAs–InP material system. It was designed for high

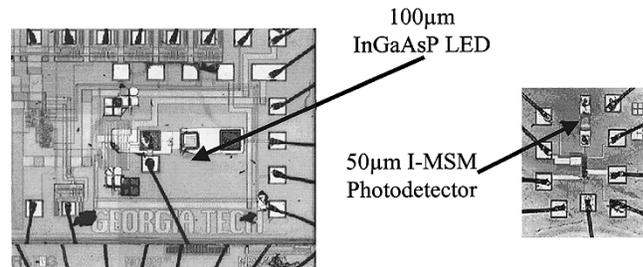


Fig. 4. Integrated optoelectronic receiver and transmitter.

speed by utilizing high doping in a thin active layer [30], [31]. The wafer was grown by MBE on an n-type $\langle 100 \rangle$ InP substrate and consisted of an InGaAs stop etch layer (100 nm, $n = 2 \times 10^{18}\ \text{cm}^{-3}$), followed by InAlAs ($1.9\ \mu\text{m}$, $n = 2 \times 10^{18}\ \text{cm}^{-3}$)/InGaAlAs ($0.45\ \mu\text{m}$, $p^+ = 1.2 \times 10^{19}\ \text{cm}^{-3}$)/InAlAs ($0.98\ \mu\text{m}$, $p = 3 \times 10^{18}\ \text{cm}^{-3}$)/InGaAs (10 nm, $p = 1 \times 10^{19}\ \text{cm}^{-3}$). The second and third designs, E2 and E3, were grown by metal–organic chemical vapor deposition (MOCVD) in the InGaAsP–InP material system. The InGaAsP material consisted of an n-type $\langle 100 \rangle$ InP substrate and InGaAsP (200 nm, $n^+ = 1 \times 10^{19}\ \text{cm}^{-3}$, $\lambda = 1.2\ \mu\text{m}$)/InP ($1.0\ \mu\text{m}$, $n = 2 \times 10^{17}\ \text{cm}^{-3}$)/InGaAsP ($1.0\ \mu\text{m}$, $n = 2 \times 10^{17}\ \text{cm}^{-3}$, $\lambda = 1.3\ \mu\text{m}$)/InP ($1.0\ \mu\text{m}$, $p = 2 \times 10^{17}\ \text{cm}^{-3}$)/InGaAsP (200 nm, $p^+ = 3 \times 10^{18}\ \text{cm}^{-3}$, $\lambda = 1.2\ \mu\text{m}$). In these designs, high-speed operation was achieved by employing high-current injection [32], [33]. To achieve high-current densities, since the driver was limited to 80 mA of output current, smaller device sizes were used. E2s were $100\ \mu\text{m}$ on a side devices and E3s were $50\ \mu\text{m}$ on a side devices.

2) *Detector Design*: The optimal detector for implementation in the three-layer through-Si data link has a low capacitance per unit area, a high responsivity, and low-noise operation. A metal–semiconductor–metal (MSM) detector meets all of these requirements save the responsivity, which is poor, generally 0.2–0.4 A/W, and the dark current, which is relatively large in the InP material system [34]. An in-

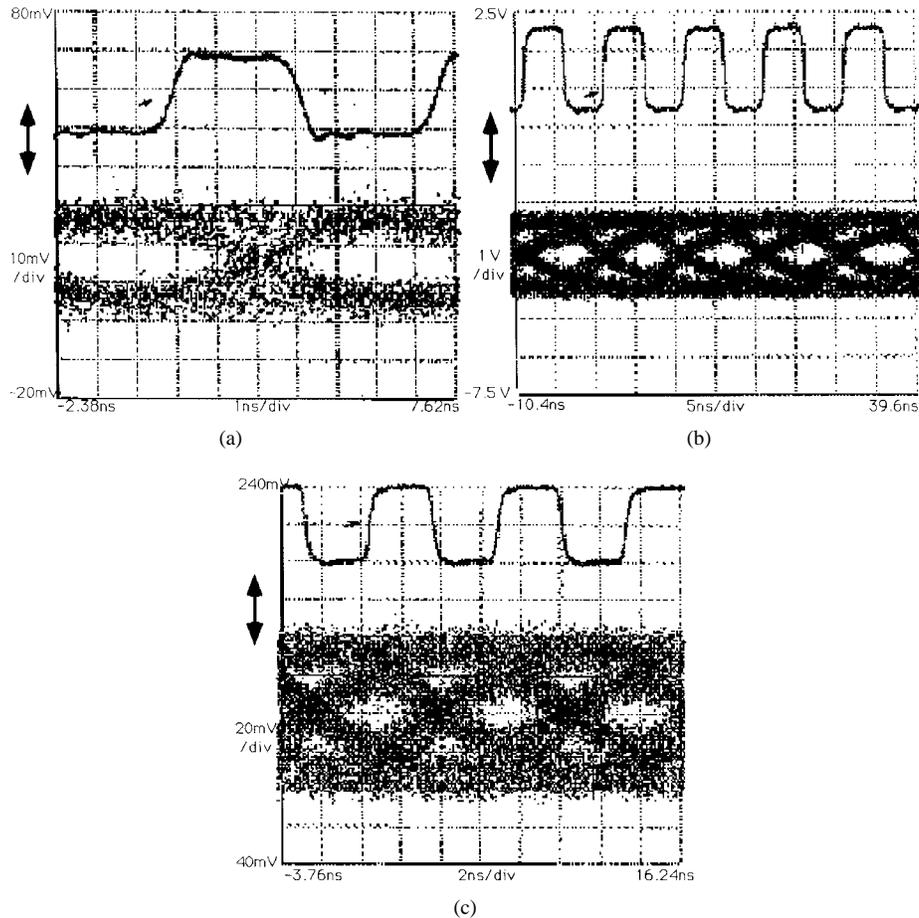


Fig. 5. Optical eye diagrams for integrated transmitters. (a) 250- μm InGaAlAs device ($E1$) at 155 Mb/s. (b) 100- μm InGaAsP device ($E2$) at 100 Mb/s. (c) 50- μm InGaAsP device ($E3$) at 155 Mb/s.

verted MSM (I-MSM) photodetector, with the electrodes on the bottom of the device and the substrate removed, can produce higher responsivity than a conventional MSM and comparable efficiency to p-i-n detectors by eliminating the shadowing effect of the electrodes [35], while preserving the desirable low capacitance, large-area characteristics of MSM's.

Two different device designs were investigated for the system under development. Since the size of the detector and the finger spacing and width affects the capacitive loading of the receiver input, detectors were designed and tested in 50- and 250- μm sizes with varying finger widths and spacings. The 50- μm active area design $D1$ utilized finger widths of 2 μm separated by 2 μm , and had an estimated capacitance of 70 fF. The 250 μm active area device $D2$ utilized finger widths of 2 μm separated by 8 μm and had an estimated capacitance of 200 fF. The MSM structure was grown lattice matched to an InP (substrate) and consisted of InGaAs (100 nm, etch layer)/InAlAs (40 nm)/InGaAs (1000 nm)/InAlAs (40 nm), with all layers nominally undoped (on the order of 10^{15} cm^{-3}). The InAlAs cladding layer minimizes the dark current [36], eliminates low frequency gain [37], and enhances the Schottky barrier height. The heterointerfaces were graded to ensure better carrier transport as well as improved dark current characteristics.

3) *Integration with CMOS Circuits:* The transmitter and receiver circuits were fabricated through the 0.8- μm MOSIS Si CMOS foundry, and were hybrid integrated by direct metal/metal bonding of the thin-film optoelectronic devices onto the Si CMOS circuitry. The optoelectronic devices were mesa etched and the growth substrate was removed from the devices using selective substrate etching. The thin-film devices were then bonded to a Mylar transfer diaphragm [38], and the devices were selectively aligned and bonded to TiAu contact pads on the transceiver circuits. Emitters bonded to transmitter circuitry required a top (AuGe) contact, which was electrically isolated from the bottom contact using DuPont polyimide 2611. The detectors used in these demonstrations had planar contacts and were directly bonded to the circuitry after the LED integration was complete. In this manner, the optoelectronic devices, the emitter and detector, were independently optimized (as was the Si CMOS circuit) and metal/metal bonded together to realize a hybrid integrated OEIC. A photomicrograph of an integrated receiver circuit and an integrated transmitter circuit are shown in Fig. 4.

III. EXPERIMENTAL RESULTS

A. Optoelectronic Integrated Transmitter

To test the speed of the integrated transmitters, the circuits were wire bonded into a high-speed quad flat pack and placed

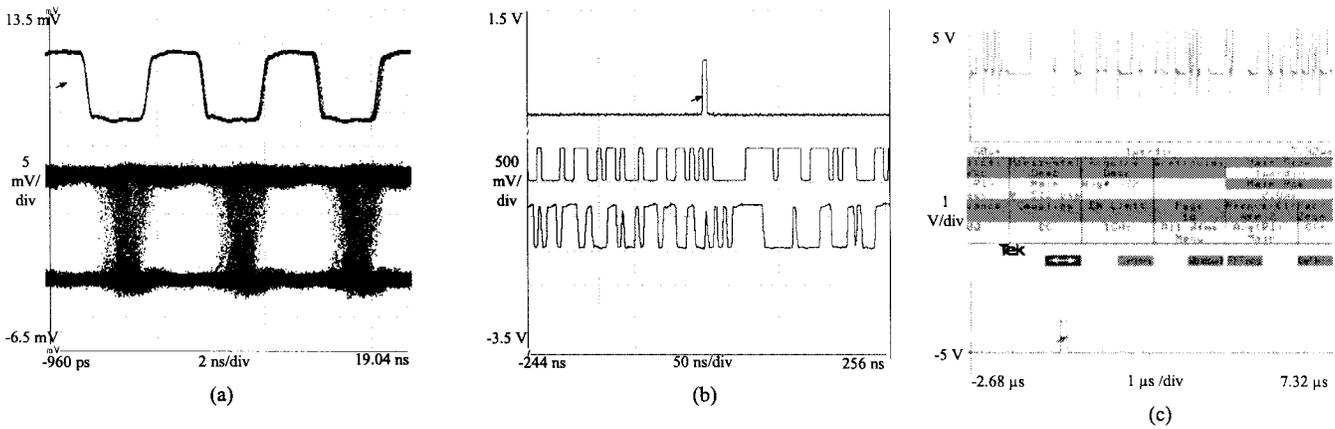


Fig. 6. Integrated receiver results. (a) Eye diagram for 50- μm MSM at 155 Mb/s. (b) Pulse diagram for 50- μm MSM at 155 Mb/s. (c) Pulse diagram for 250- μm MSM at 10 Mb/s.

into a conductive box for shielding. Prior to digital testing of the integrated transmitter, the thin-film devices were dc characterized with microprobes. Typical light output levels for the devices were: $E1$: 50 μW at 80 mA (0.128 kA/cm^2); $E2$: 500 μW at 80 mA (0.8 kA/cm^2); and $E3$: 150 μW at 80 mA (3.2 kA/cm^2). Next, a digital input to the circuit from a pattern generator was applied to the transmitter circuit. The emitted light was collected using a dual lens collimation/collection system and was detected using a high sensitivity receiver (New Focus 1811).

The three different designs were tested and the eye diagrams are shown in Fig. 5. Fig. 5(a) shows the output data for device $E1$ at 155 Mb/s ($2^{15}-1$ NRZ). Fig. 5(b) shows the output data for device $E2$ at 100 Mb/s (2^7-1 NRZ). Fig. 5(c) shows the output data for device $E3$ at 155 Mb/s (2^7-1 NRZ). Only device $E2$ had sufficient output power to conduct BER testing (BERT). The output of the signal was fed to the error detector, and the measured BER at 100 Mb/s (2^7-1 NRZ) was 10^{-13} . These results indicate that device $E2$ has sufficient output power and speed to operate in a 100-Mb/s through-Si optical data link, described in [9]. Device design $E1$ suffered from low internal quantum efficiency due to high doping in the active region and design $E3$ had low output power. High doping in the active region was used for some of the devices studied to achieve higher speeds in future link experiments (note that smaller device sized will be necessary, as well). For the most efficient interconnections, for high coupling, high efficiency, high speed, low drive current, and low-power dissipation, VCSEL's would be the devices of choice, as stated previously. As VCDEL technology in these wavelength regions progresses, the implementation of VCSEL's in these 3-D links will significantly improve the performance.

B. Optoelectronic Integrated Receiver

The integrated receivers were packaged into high speed LDCC packages, and fully tested: dc characteristics of the MSM designs $D1$ and $D2$ were measured, and digital tests were performed. The optimal dark current was achieved by annealing the MSM's and the Schottky contact metals (Ti (150

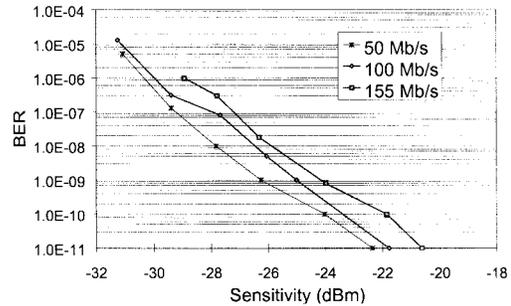


Fig. 7. BER measurements for the integrated 50- μm MSM receiver.

$\text{\AA})//\text{Pt}$ (500 $\text{\AA})//\text{Au}$ (2500 $\text{\AA})$) for one hour at 200 $^\circ\text{C}$. The dark current was less than 10 nA for device $D2$.

Digital testing was performed using a commercial laser modulated by a pseudorandom bit stream. The output of the laser was fiber coupled to the detectors. An eye diagram and output waveform for device $D1$ (50 μm) are shown in Fig. 6(a) and (b). This small device operated at a speed 155 Mb/s using 2^7-1 NRZ, due to the small capacitive loading of the receiver. This particular receiver was also tested for BER as a function of sensitivity as shown in Fig. 7. The receiver integrated with the larger device $D2$ with 25 times the area of $D1$ (capacitance of 200 fF), operated up to 10 Mb/s with a 2^7-1 pseudorandom data stream (PRBS), as shown in Fig. 6(c), and a BER of 10^{-11} for an incident optical power of 80 μW . Although the small device ($D1$) operated faster, it is not large enough to provide good alignment tolerance and collection efficiency for the LED-based through-Si optical transmitter.

C. Three-Layer 3-D Vertically Optically Interconnected Link Demonstration

The 3-D three-layer stacks of OEIC's demonstrating vertically optically interconnected through-Si CMOS systems were fabricated and tested. The Si CMOS analog interface building block circuit designs described previously herein were used in a transceiver circuit to produce three-level stacking by

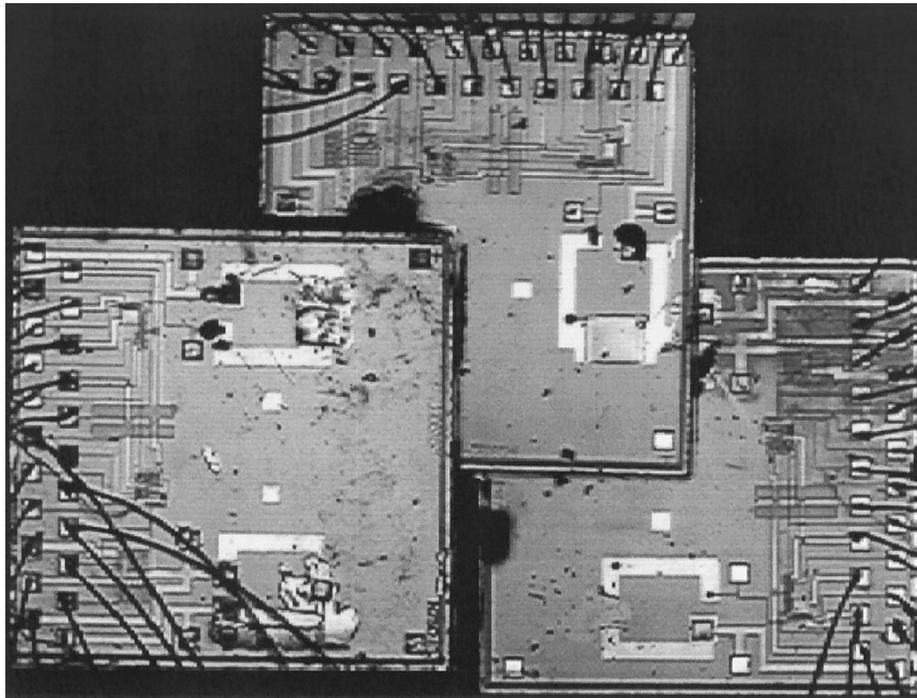


Fig. 8. Picture of tested three-layer 3-D CMOS system.

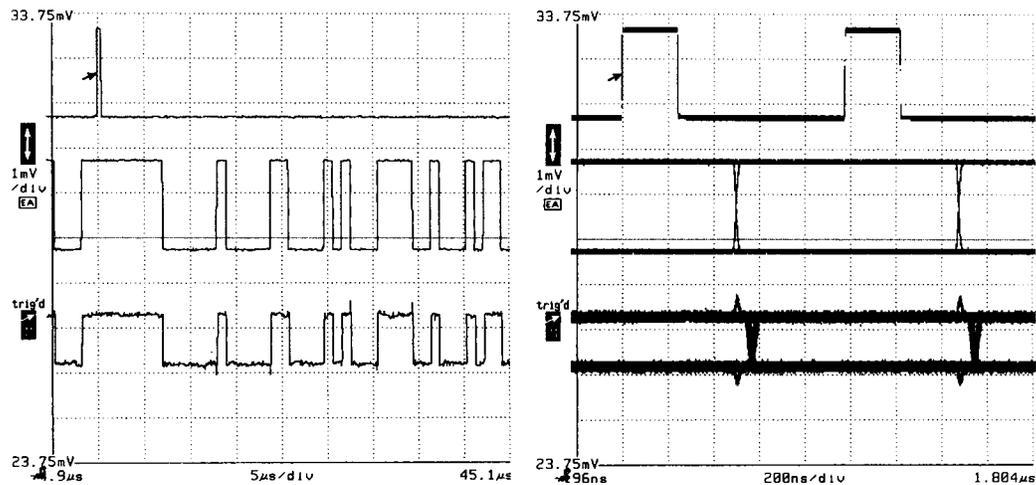


Fig. 9. Bottom through-Si CMOS optical channel RX output at 1 Mb/s.

incorporating bonding pads on only one side of the circuit and by leaving optoelectronic integration sites on the other side of the circuit free from metallization layers. The most suitable optoelectronic devices, as determined above, were integrated onto three stackable circuits. The three-layer stacked system was assembled by aligning the individual layers using an infrared backplane mask aligner and by using Si material to provide mechanical support during wire bonding of the three-dimensional system. After all three layers were assembled and attached using an ultraviolet and heat curing epoxy, the system was packaged into a 144 pin ceramic pin grid array. Fig. 8 is a photomicrograph of one of the tested packaged 3-D systems.

To demonstrate the vertical optical interconnections in the 3-D three-layer Si CMOS circuit stack, the middle integrated receiver was powered up and a digital input signal was applied to the bottom-layer transmitter. This vertical communications link operated at 1 Mb/s with a PRBS signal of length 2^7-1 . The middle layer receiver output pulse waveform and an infinite persistence eye diagram are shown in Fig. 9. The second vertical optical interconnection was operated by applying the PRBS digital signal to the middle chip transmitter and by monitoring the output waveform on the top layer integrated receiver. This vertical communications link also operated at 1 Mb/s and demonstrated open eye diagrams as shown in Fig. 10. A previous test of this system demonstrated

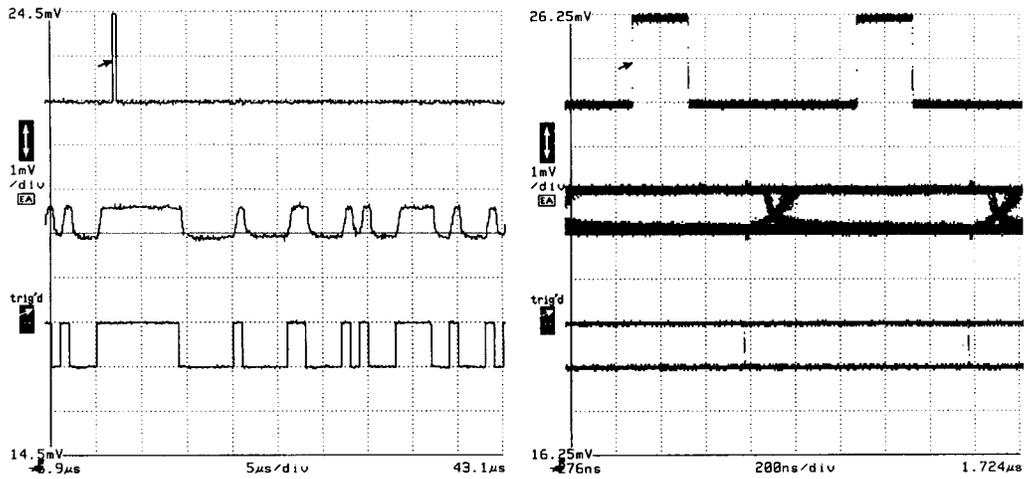


Fig. 10. Top through-Si CMOS optical channel RX output at 1 Mb/s.

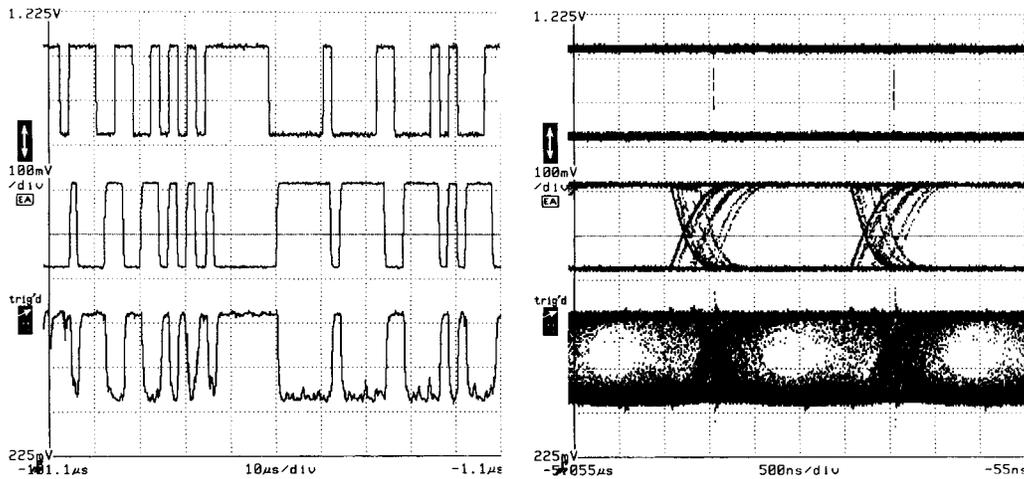


Fig. 11. Three-layer optical interconnection results at 500 kb/s (from top to bottom). Bottom layer: Transmitter input data, Middle layer: Comparator output, Top layer: RX output.

bit error rates at 1 Mb/s of 1×10^{-9} with a PRBS signal of length $2^7 - 1$; this is the first reported BER measurement for a through-Si CMOS optical interconnection.

The final demonstration that we report herein is the complete system interconnection from the bottom layer of the three-layer system to the top layer of the system, with only power supply and monitor connections to the middle layer. The PRBS digital signal was applied to the bottom-layer transmitter input that communicated optically to the middle-layer receiver circuit. The received signal on the middle layer was then sent to an on-chip clocked comparator that regenerated the receiver signal to digital levels suitable for driving the digital input of the transmitter. This signal was used as the input to the middle-layer transmitter that communicated optically to the top layer receiver. Fig. 11 shows 500-kb/s results from the through three-layer optical interconnection. The top trace is the input signal applied to the bottom transmitter, the middle trace is a monitor of the middle chip comparator, and the top signal is the output of the top circuit receiver.

Although the optical transceiver components in this system have demonstrated individual operation speeds in excess of 155 Mb/s, the multilayered system investigated in this paper was limited to 1-Mb/s operation. Signal coupling within the high-pin count CPGA packages and within the test fixture were believed to limit the speed of the layer to layer interconnections. The 3-D three-layer system, which operated at 500 kb/s, was speed limited by the noise generated within the middle layer CMOS circuit which had a clocked comparator, a single ended transmitter, and a single-ended receiver all operating simultaneously. We believe that feedback of the single-ended transmitter output signal into the sensitive single-ended receiver was the primary cause of this noise. This was confirmed by observing a decrease in the signal quality of the middle-layer receiver with an increase in the middle-layer transmitter output current. The need to run the transmitter at low power limited the speed obtainable from the top chip receiver. Higher speed demonstrations should be possible by utilizing improved decoupling networks within the test fixture, by utilizing higher speed quad-flat

packages and by utilizing differential CMOS transceiver circuits.

IV. CONCLUSION

Presented herein for the first time is a report of the development, fabrication, and test of a three-layer 3-D CMOS interconnection system with integrated long wavelength through-Si optical interconnections. We have demonstrated $\lambda = 1.3 \mu\text{m}$ InGaAlAs and InGaAsP thin-film LED's integrated directly on digital Si CMOS transmitter circuitry with digital optical operations of 100 and 155 Mb/s. We also have demonstrated a transimpedance amplifier circuit in standard digital CMOS integrated with a $\lambda = 1.3 \mu\text{m}$ thin film I-MSM demonstrating an integrated receiver with digital operation of 155 Mb/s. These system components have been combined together to demonstrate the first optically interconnected 3-D three-layer CMOS system, with operation of 1 Mb/s at a BER of 10^{-9} . This is the first report of a BER measurement on a through-Si optical interconnection. System development is continuing to resolve the signal coupling problems in the high pin count package that have limited our operation speed to 1 Mb/s with the goal of three-layer communication at 100 Mb/s.

ACKNOWLEDGMENT

The authors wish to thank the Microelectronics Research Center staff of the Georgia Institute of Technology for the assistance with microfabrication, R. P. Leavitt of the Army Research Laboratories for the growth of the InGaAlAs materials, and DuPont for the donation of PI2611 polyimide.

REFERENCES

- [1] J. D. Meindl, "Gigascale integration: Is the sky the limit?" *IEEE Circuits and Devices Mag.*, vol. 12, pp. 19–32, Nov. 1996.
- [2] [Online]. Available HTTP: <http://notes.sematech.org/97pelec.html>
- [3] S. Tang and R. Chen, "1-to27 highly parallel three-dimensional intra and inter board optical interconnects," *IEEE Photon. Technol. Lett.*, vol. 6, pp. 299–301, Feb. 1994.
- [4] J. W. Goodman and F. J. Leonberger, "Optical interconnection for VLSI systems," S.-Y. Kung and R. A. Athale, Eds., *Proc. IEEE*, vol. 72, pp. 850–866, 1984.
- [5] N. Awaya, Y. Arita, H. Inokawa, and T. Kobayashi, "Copper interconnection technology for Si large scale integrated circuits," *NTT R&D*, vol. 45, no. 4, pp. 373–378, 1996.
- [6] R. T. Chen, H. Lu, D. Robinson, Z. Sun, T. Hansson, D. V. Plant, and H. R. Fetterman, "60 GHz board-to-board optical interconnection using polymer optical buses in conjunction with microprism couplers," *Appl. Phys. Lett.*, vol. 60, pp. 536–538, 1992.
- [7] M. Koyanagi, H. Takata, H. Okano, and S. Yokoyama, "Three-dimensional memory LSI with optical interconnections," *Electron. Commun. Jpn.*, vol. 76, pt. 2, no. 2, pp. 1–13, 1993.
- [8] M. Brooke, N. M. Jokerst, S. W. Bond, and D. S. Wills, "A comparison of CMOS chip to chip interconnections: Vertical optical through-Si links versus high density electrical interconnect," presented at the Annu. Meeting Lasers and Electro-Optics Society, Dec. 1998, paper ThU3.
- [9] D. S. Wills, W. S. Lacy, C. Camperi-Ginestet, B. Buchanan, H. H. Cat, S. Wilkinson, M. Lee, N. M. Jokerst, and M. A. Brooke, "A three-dimensional high-throughput architecture using through-wafer optical interconnect," *J. Lightwave Technol.*, vol. 13, pp. 1085–1092, June 1995.
- [10] M. Campbell, M. Little, M. Yung, J. Brewer, and M. J. Yung, "Heirarchical fault tolerance for 3D microelectronics," in *Proc. Int. Conf. Wafer Scale Integration*, San Francisco, CA, 1990, pp. 174–188.
- [11] L. A. Hornak and S. K. Tewksbury, "On the feasibility of through-wafer optical interconnects for hybrid wafer-scale-integrated architectures," *IEEE Trans. Electron Devices*, vol. ED-34, pp. 1557–1563, July 1987.
- [12] A. D. Norte, A. E. Willner, W. Shieh, and A. R. Tanguay, "Multiple-layer optical interconnections using through-wafer hollow-dielectric-waveguide vias," *IEEE Photon. Technol. Lett.*, vol. 6, pp. 851–854, July 1994.
- [13] J. Yoo, J. E. Leight, G. Giarretta, W. Yuen, A. E. Willner, and C. J. Chang-Hasnain, "Experimental demonstration of a four-plane 2-D multiple-wavelength optical interconnection using integrated VCSEL arrays and MQW/DBR detectors," *IEEE Photon. Technol. Lett.*, vol. 9, pp. 1646–1648, Dec. 1996.
- [14] N. M. Jokerst, C. Camperi-Ginestet, B. Buchanan, S. Wilkinson, and M. A. Brooke, "Communication through stacked Si circuitry using integrated thin film InP-based emitters and detectors," *IEEE Photon. Technol. Lett.*, vol. 7, pp. 1028–1030, Sept. 1995.
- [15] J. Geist, A. Migdall, and H. P. Baltes, "Analytic representation of the Si absorption coefficient in the indirect transition region," *Appl. Opt.*, vol. 27, no. 18, pp. 3777–3779, 1988.
- [16] K. H. Calhoun, C. Camperi-Ginestet, and N. M. Jokerst, "Vertical optical communication through stacked silicon wafers using hybrid monolithic thin film InGaAsP emitters and detectors," *IEEE Photon. Technol. Lett.*, vol. 5, pp. 254–257, Feb. 1993.
- [17] O. Vendier, S. W. Bond, M. Lee, S. Jung, M. Brooke, N. M. Jokerst, and R. P. Leavitt, "Stacked silicon CMOS circuits with a 40 Mb/s through-silicon optical interconnect," *IEEE Photon. Technol. Lett.*, vol. 10, pp. 606–608, Apr. 1998.
- [18] M. Govindarajan, S. Siala, and R. N. Nottenburg, "Optical receiver systems for high speed parallel digital data links," *J. Lightwave Technol.*, vol. 13, pp. 1555–1565, July 1995.
- [19] T. G. Brown, P. L. Bradford, and D. G. Hall, "Optical emission from crystalline Si," *Proc. SPIE*, vol. 704, pp. 38–42, 1987.
- [20] G. W. Turner, C. K. Chen, B. Y. Tsauro, and A. M. Waxman, "Through-wafer optical communication using monolithic InGaAs-on-Si LED's and monolithic PtSi-Si Schottky-barrier detectors," *IEEE Photon. Technol. Lett.*, vol. 3, pp. 761–763, Aug. 1991.
- [21] L. A. Hornak, S. K. Tewksbury, and H. E. Nariman, "GaAs heteroepitaxy with submicron Si CMOS: An experimental compatibility study," *Proc. SPIE*, vol. 1849 pp. 38–47, 1993.
- [22] K. W. Goossen, G. D. Boyd, J. E. Cunningham, Y. Y. Jan, D. A. B. Miller, D. S. Chemla, and R. M. Lum, "GaAs/AlGaAs multiquantum well reflection modulators grown on GaAs and Si substrated," *IEEE Photon. Technol. Lett.*, vol. 1, pp. 304–306, Oct. 1989.
- [23] C. Camperi-Ginestet, M. Hargis, N. Jokerst, and M. Allen, "Alignable epitaxial lift-off of GaAs materials with selective deposition using polyimide diaphragms," *IEEE Photon. Technol. Lett.*, vol. 2, pp. 1123–1125, Dec. 1991.
- [24] D. A. B. Miller, "Dense two-dimensional integration of optoelectronics and electronics for interconnection," *Heterogeneous Integration: Systems on a Chip*, *SPIE Critical Reviews of Optical Engineering*, A. Husain and B. Fallahi, Eds., vol. CR 70, 1998, pp. 80–119.
- [25] M. Brooke, N. Jokerst, S. Bond, and D. Wills, "Comparison of CMOS chip to chip interconnections: Vertical optical through-Si links versus high density electrical interconnect," in *Proc. Conf. IEEE LEOS Annu. Meeting*, Orlando, FL, Dec. 1998, pp. 186–187.
- [26] M. Lee, O. Vendier, M. A. Brooke, and N. M. Jokerst, "Scaleable CMOS current-mode preamplifier design for an optical receiver," *Analog Integrated Circuits and Signal Processing*, vol. 12, pp. 133–144, 1997.
- [27] R. P. Jindal, "Gigahertz-band high-gain low-noise AGC amplifiers in fine-line NMOS," *IEEE J. Solid-State Circuits*, vol. SC-22, pp. 512–521, Apr. 1987.
- [28] G. M. Yin, "A high speed CMOS comparator with 8-b resolution," *IEEE J. Solid-State Circuits*, vol. 27, pp. 208–211, Feb. 1992.
- [29] T. Baba, Y. Yogo, K. Suzuki, F. Koyama, and K. Iga, "First room temperature CW operation of GaInAsP/InP surface emitting laser," *IEICE Trans. Electron.*, vol. 76-C, no. 9, pp. 1423–1424, 1993.
- [30] A. Suzuki, T. Uji, Y. Inomoto, J. Hayashi, Y. Isoda, and H. Nomura, "InGaAsP/InP 1.3 μm wavelength surface-emitting LED's for high-speed short-haul optical communication systems," *J. Lightwave Technol.*, vol. LT-3, pp. 1217–1222, June 1985.
- [31] Y. Kashima, A. Matoba, and H. Takano, "Performance and reliability of InGaAsP superluminescent diode," *J. Lightwave Technol.*, vol. 10, pp. 1644–1649, Nov. 1992.
- [32] S. Machida, H. Nagai, and T. Kimura, "Modulation characteristics of

- InGaAsP/InP LED's at 1.5- μm wavelength," *Electron. Lett.*, vol. 15, no. 6, pp. 175-177, 1979.
- [33] R. Saul, "Recent advances in the performance and reliability of InGaAsP LED's for lightwave communication systems," *IEEE Trans. Electron Devices*, vol. 30, pp. 285-295, 1983.
- [34] F. Hieronymi, E. H. Bottcher, E. Droge, D. Kuhl, and D. Bimberg "High performance large area InGaAs metal-semiconductor-metal photodetectors," *IEEE Photon. Technol. Lett.*, vol. 5, pp. 910-913, Aug. 1993.
- [35] O. Vendier, N. M. Jokerst, and R. P. Leavitt, "Thin film inverted MSM photodetectors," *IEEE Photon. Technol. Lett.*, vol. 8, pp. 266-268, Feb. 1996.
- [36] J. B. D. Soole, H. Schumacher, R. Bhat, and M. Koza, "High-speed performance of OMCVD grown InAlAs/InGaAs MSM photodetectors at 1.5 μm and 1.3 μm wavelengths," *IEEE Photon. Technol. Lett.*, vol. 1, pp. 250-252, Aug. 1989.
- [37] M. Klingenstein, J. Kuhl, J. Rosenzweig, C. Moglestue, A. Hulsman, J. Schneider, and K. Kohler, "Photocurrent gain mechanisms in metal-semiconductor-metal photodetectors," *Solid State Elect.*, vol. 37, no. 2, pp. 333-340, 1994.
- [38] C. Camperi-Ginestet, M. Hargis, N. Jokerst, and M. Allen, "Alignable epitaxial liftoff of GaAs material with selective deposition using polyimide," *IEEE Photon. Technol. Lett.*, vol. 2, pp. 1123-1126, 1991.



Steven W. Bond received the B.S. and M.S. degrees from the Georgia Institute of Technology, Atlanta both in electrical engineering, in 1991 and 1994 respectively, where he is now a Ph.D. candidate specializing in integrated optoelectronic circuits and systems.

Since beginning his Ph.D. work in 1992, he has specialized in the design and characterization of long-wavelength thin-film emitters for applications in vertical optical interconnections for standard Si CMOS circuitry. He worked at the IBM T.J. Watson

Research Center as an Engineer in 1993. He is currently employed by Lawrence Livermore National Labs in California.

Mr. Bond is a member of the IEEE Lasers and Electro-Optics Society, American Society for Engineering Education, Phi Theta Kappa National Honor Fraternity, and Tau Alpha Pi National Engineering Honor Society.

Olivier Vendier, photograph and biography not available at the time of publication.

Myunghee Lee (S'89-M'96), photograph and biography not available at the time of publication.



Sungyong Jung received the B.S. and M.S. degrees in electronic engineering from Yeungnam University, South Korea, in 1991 and 1993, respectively. He is working toward the Ph.D. degree through Georgia Institute of Technology, researching optical transmitter design and modeling for optical interconnect.



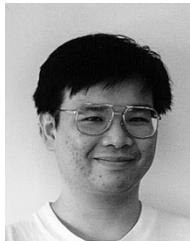
Michael Vrazel received the B.S. degree in physics from the University of Alabama, Tuscaloosa, in 1997 and is working toward the Ph.D. in electrical engineering at the Georgia Institute of Technology, Atlanta.

His area of research is in high-speed alignment tolerant optoelectronics.



Abelardo Lopez-Lagunas (S'90-M'91) received the B.S. degree in electrical engineering from the Instituto Tecnológico y de Estudios Superiores de Monterrey Campus Toluca, in 1988, the M.S. and Ph.D. degrees in electrical engineering from the Georgia Institute of Technology, Atlanta, in 1991 and 1997, respectively.

As a graduate student he formed part of the Portable Image Computation Architecture (PICA) group directed by Dr. D. Scott Wills. His doctoral research focused on hardware support for fine-grain architectures. He is an Assistant Professor in the Instituto Tecnológico y de Estudios Superiores de Monterrey Campus Toluca. In 1998, he joined the Concurrent VLSI Architecture Group, led by Dr. William J. Dally in the design of the Imagine processor at Stanford. His research interests include Parallel Architectures, VLSI design, and parallel compilers. He is a member of the IEEE Computer Society.



Sek Chai received the B.S. and M.S. degrees from the Georgia Institute of Technology, Atlanta, GA, in 1994 and 1996, respectively, both in electrical engineering in 1996. He is working toward the Ph.D. degree in the portable image computation architectures (PICA) at Georgia Tech.

His research interests include parallel architecture, VLSI, billion transistor architectures, and high performance interconnection networks. His doctoral research focuses on high throughput, efficient architectures such as systolic arrays. He is a member of

the IEEE Computer Society.

Georgiana Dagnall received the B.S.E.E. degree from Mississippi State University, Mississippi State, MS, and the M.S. degree from the Georgia Institute of Technology, Atlanta, GA. She is working toward the Ph.D. degree at the Georgia Institute of Technology researching the properties of optical devices on novel oriented substrates.

Her research interests include the design, growth, process and test of optical semiconductor devices.

Martin Brooke (S'85-M'86) received the Ph.D. degree in electrical engineering from the University of Southern California, Los Angeles, CA, in 1988. His doctoral research focused on reconfigurable analog and digital integrated circuit design.

He is an Associate Professor in the School of Electrical and Computer Engineering at the Georgia Institute of Technology, Atlanta, GA. He has three U.S. patents awarded, and he has published 32 refereed papers, and articles on his work have appeared in 15 different trade publications.

Dr. Brooke won a 1990 National Science Foundation Research Initiation Award, and the 1992 IEEE Midwest Symposium on Circuits and Systems, Myril B. Reed Best Paper Award. Dr. Brooke is a member of the INNS.

Nan Marie Jokerst (S'83-M'88-SM'98), for photograph and biography, see this issue, p. 144.



D. Scott Wills (S'80-M'83-SM'98) received the B.S. degree in physics from the Georgia Institute of Technology, Atlanta, GA, in 1983, and the S.M., E.E., and Sc.D. degrees in electrical engineering and computer science from the Massachusetts Institute of Technology, Cambridge, MA, in 1985, 1987, and 1990, respectively.

He is an Associate Professor of Electrical and Computer Engineering at Georgia Institute of Technology. His research interests include concurrent VLSI architectures, high throughput portable processing systems, and gigascale semiconductor modeling.

Dr. Wills is a member of the Computer Society.



April Brown (S'79-M'87-SM'91-F'97) is Professor in the School of Electrical and Computer Engineering and Associate Dean in the College of Engineering at the Georgia Institute of Technology, Atlanta, GA. Prior to joining Georgia Tech in 1994, she was a Senior Scientist at the Hughes Research Labs, Malibu, CA. Her research focuses on the development of materials for electronic and photonic devices. She is currently engaged in research in phosphides, nitrides, and antimonides. She is an Associate Editor of the IEEE TRANSACTIONS ON ELECTRON DEVICES. She is author or coauthor of over 120 publications and presentations.

Dr. Brown is an elected member of the Administrative Committee of the IEEE Electron Devices Society.