FULLY DIFFERENTIAL CURRENT-INPUT CMOS AMPLIFIER FRONT-END SUPPRESSING MIXED SIGNAL SUBSTRATE NOISE FOR OPTOELECTRONIC APPLICATIONS

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Abstract–**In recent optoelectronic communication systems, microprocessors tend to be imbedded on-chip with analog interface circuitry. This results in a critical substrate noise issues for mixed-signal chip designers because switching transients in digital MOS circuits can interfere with analog circuits integrated on the same die by means of coupling through the substrate. In order to optimize the dynamic range of the system and to minimize the sensitivity to substrate noise, many noise-reduction techniques, such as a P+ guard ring, a N-well guard ring, Trench oxide isolation, and MOSCAP have been developed and employed to suppress substrate noise generated by clocking of the digital circuitry in Microprocessor. In this paper, a fully differential method is described, which is used to reduce the substrate noise effect caused by microprocessor. This approach has been implemented in an communications data processing application, in which the microprocessor is located next to the analog current-input optical data receiver and quantization circuits which have a sensitivity of –28dBm and variable gain characteristic for power efficiency. Both simulated and experimental results of this design approach are presented herein.**

I. INTRODUCTION

Mixed signal IC design is critical to a number of applications, including optoelectronic (OE) systems, where mixed signal technology enables the incorporation of complex, rapidly changing transient high speed digital circuitry with highly sensitive analog OE link interface circuits. In such mixed signal IC designs, substrate noise generated by rapidly changing transients in the digital circuitry can be coupled into the sensitive analog input signal, which results in extremely poor bit error rate (BER) performance of the OE link.

A number of techniques have been explored to prevent this substrate noise coupling, such as using guard rings and MOSCAPs, but none were effective enough to satisfy mixed signal IC designers.[1] To prevent substrate noise from affecting the sensitive amplifier we must negate the effects of coupled switching signals from digital circuitry and prevent the injection of noise via the biases and the input signals of the analog interface circuitry. The switching noise is injected into the analog circuitry through both direct capacitive coupling between interconnect lines and through interaction via the substrate.

This paper focuses on reducing substrate noise and substrate coupling using a fully differential circuit topology. Described herein is a current-mode optical receiver and comparator designed to reduce the digital substrate noise injection. Both design and experimental data from a fabricated and tested circuit will be discussed.

II. CIRCUIT DESIGN

In optical communication systems, the preamplifier uses a single input/output, which makes analog interface circuitry prone to pick up noise. This pick up noise emanates from the power supply rails through the substrate from the digital circuitry when the digital circuitry coexists on a single chip with the analog circuitry. [3] From a crosstalk perspective in mixed signal chip design, a differential or balanced circuit analog interface topology is

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preferred since it delivers stabilized current for device biases. [2]

Current mode amplifiers require more power dissipation than other topologies for a certain bandwidth and sensitivity. Thus, after achieving the bandwidth requirement, the next concern is the input noise level or sensitivity of the amplifier. For amplifiers with a multi-stage configuration, the noise contribution from the later stages is negligible compared to that from the first stage. Thus, voltage mode amplifiers can be used for post amplification to minimize the power dissipation since voltage mode amplifiers have been known to consume a minimum of power.[4]

A number of researchers have investigated design techniques using current-mode approaches, Herein is described a differential current-mode amplifier which uses a current mirror as the input. Figure 1. illustrates the differential current-mode amplifier stage after using a current mirror as the input pair. To increase the bandwidth of the amplifier, it will be compensated using voltage gain differential post amplifiers, and a high-speed, diode-connected active load is employed to obtain the maximum bandwidth. The tail current, i_{bias} is supplied by another current mirror. From the analysis, a cascoded current mirror for the tail current is desirable. The transimpedance gain of the current-mode amplifier is given by

Where g_m is a transconductance of transistors, it is designed so that bias currents of both sides are the same.

By controlling the bias current ratio, the input impedance can also be adjusted. The input

$$A_R = \frac{V_{out}}{i_{in}} = (\frac{1}{g_{m1}}) \cdot (\frac{g_{m2}}{g_{m5}}) \approx \frac{1}{g_{m5}}$$

impedance's at both inputs are not symmetrical, though. Also, for the current biasing circuits, cascoded current mirrors are used since it gives not only a higher impedance, but also, it sets the bias voltage of the two input nodes at the middle of two power supply rails which are Vdd and Vss.

Figure 2. illustrates a differential voltage-mode amplifier, which is used as a post amplifier after the current-mode input stage. Since it is known that voltage-mode amplifier consumes less power for a given bandwidth, it is used for the later stages to minimize the overall power dissipation. The gain of each stage is given by

$$A_v = \frac{g_{m1}}{g_{m3}}$$

The overall amplifier schematic is shown in Figure 3. and its overall transimpedance gain is given by

$$A_{total} = A_R \cdot A_v^{\,6} \cdot A_{Last}$$

Where A_V is the transimpedance gain of preamplifier and A_{Last} is the gain of differential-input single-output stage, which is designed to have a value of twice of A_v.

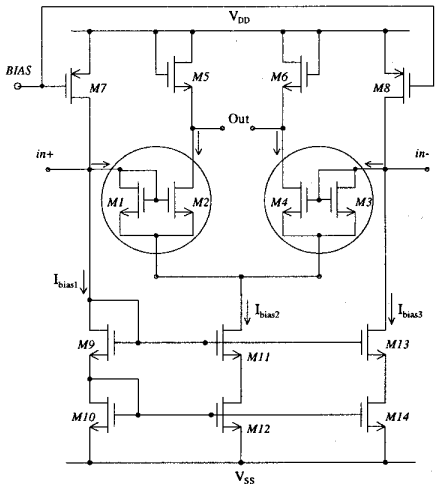

Figure 1: Differential Current-mode Amplifier Front Stage

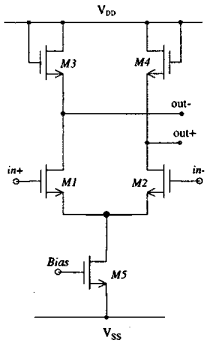

Figure 2: Differential high speed voltage amplifier stage

Figure 6. shows the Photomicrograph of the fabricated chip. In the photo the microprocessor

is located on the left side and analog interface circuitry is located on the right.[5][6][7]

III. EXPERIMENTAL RESULT

To verify the elimination of substrate noise into the analog interface circuitry, one of the fabricated chips, which contains the analog circuitry and microprocessor, was tested. Figure 4. shows the output results of analog part, when microprocessor is clocked and functioning, the data were captured from an oscilloscope. Figure 5. shows the output of the digital circuitry to verify the functioning of microprocessor. The measured bit error rate of the receiver was 10^9, with an optical input signal power of -28dBm.

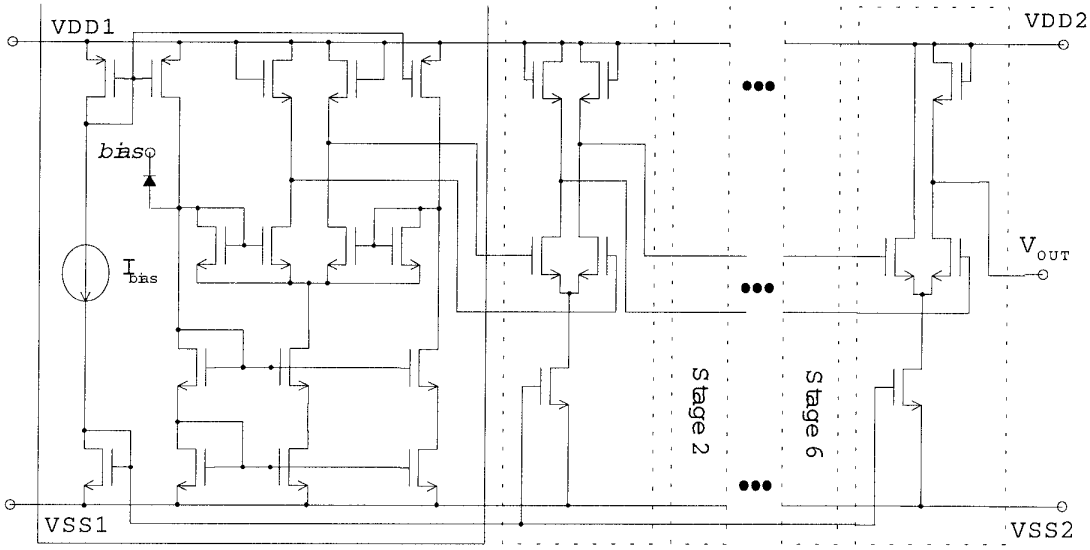

Figure 3: Whole Circuit Schematic of Current-mode Differential Amplifier

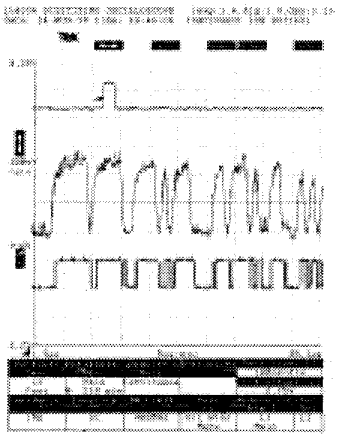

Figure 4: Output of analog circuitry (Amplifier and Comparator)

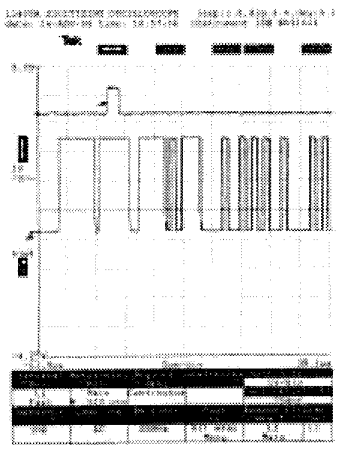

Figure 5: Output of Digital Circuitry (Microprocessor)

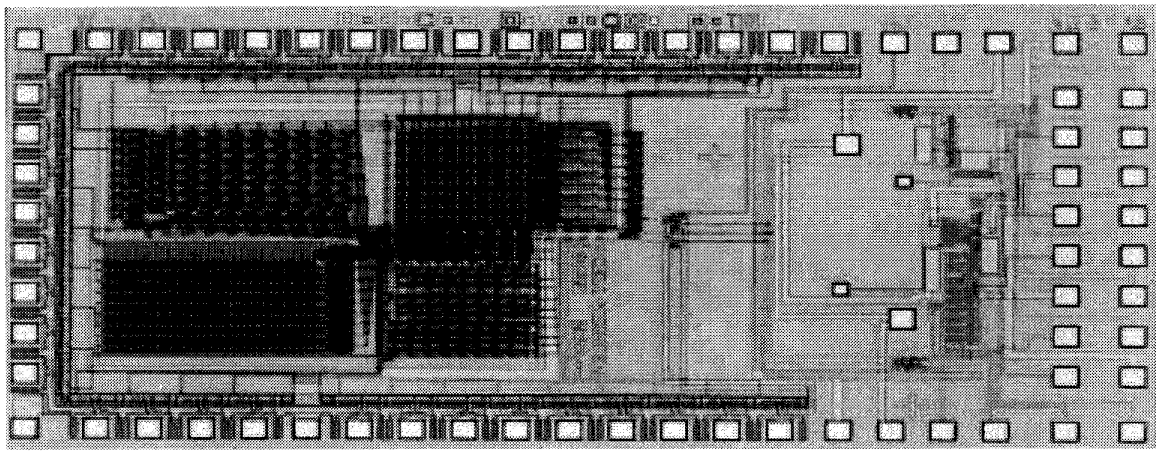

Figure 6: Photo-picture of chip (left side: Microprocessor, right side: Analog interface)

IV. CONCLUSION

A differential circuit topology with a current input front end was used to reduce mixed-signal substrate clocking noise in an optical receiver system. The differential current-mode optical receiver has been designed and fabricated in 0.8 um standard digital CMOS processor with on chip digital image processing microprocessor through the MOSIS foundry. The amplifier consists of a current mode differential preamplifier with 7 identical cascaded voltage-mode differential amplifier stages following. From the result of tests, this method was proved to be effective in reducing substrate noise.

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