ADAPTIVE DIGITAL BIAS CONTROL FOR AN OPTICAL RECEIVER AND TRANSMITTER

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Abstract-This paper presents test results for an adaptive bias control for an optical receiver and transmitter. The need for accurate adaptive bias sources has been an important issue for the design of compact, high-resolution, high-precision optoelectronic circuits. The use of an adaptive bias control is applicable to circuit designs, which require variable bias sources for low power operation or optimal performance. The use of an adaptive bias control for our optical receiver and transmitter enables substantial reductions in the pad count of circuits and are required to optimize the Bit Error Rate of the communications link the circuits operate in. The on chip adaptive bias solution may enable the circuits to be designed with reduced cost, size, and complexity, while maintaining high precision and performance.

1. INTRODUCTION

Pin count is a critical limiting aspect of mixed-signal integrated circuit (IC) design. Thus, the minimization of external connections for multiple bias sources in mixed signal designs is highly desirable. In addition, to design compact, high-resolution, high-precision CMOS mixed-signal circuits, accurate bias sources must be used. In the area of optoelectronic interface circuits, it is common to utilize circuits that process very small signals from optical detectors. Therefore, multiple variable bias sources must be used to make the entire system operate optimally. Herein is described an integrated adaptive bias solution for zero passive component count high-performance mixed-signal ICs. This paper presents experimental results of an integrated adaptive bias solution for an optical receiver and transmitter that have been applied to a low-cost bidirectional optical link.[1, 3]

In this paper, a general description for the adaptive integrated bias circuitry is presented. This biasing system (the CMOS 'Digital Bias Bus') is use to bias analog optoelectronic interface circuitry, namely, a detector amplifier and an emitter driver..

2. SYSTEM DESCRIPTION

The CMOS Bias Bus was designed to minimize pincount for an optoelectronic bi-directional link. The CMOS Bias Bus circuit was designed to be scalable, and was fabricated in a 0.8μm standard digital CMOS process through the MOSIS foundry. This chip is composed of a single-ended optical receiver, consisting of a transimpedance amplifier, a single ended optical transmitter, an array of PiN silicon detectors, a DAC, and digital interface circuitry.

The digital interface circuitry receives a digital input pattern from off-chip, and delivers a stable set of values to an on-chip DAC. In the proposed application, 35 shift register/ latch cells are required. However, the cell can be chained to any length. The desired pattern is loaded into the 35-bit shift register off-chip using a PC controlled digital I/O card. This pattern is injected to the digital circuitry through an input pad. Once the pattern is fully loaded, it is available as parallel inputs to the DACs. Seven DACs are used in this chip to produce seven bias currents. Five bias currents (RX_Isink1, RX_Isink2, RX_Isource1, RX_Isource2, RX_Ioffset) are used for the receiver and two bias currents (TX_Ibias1, TX_Ibias2) for the transmitter. Figure 1 is a schematic of the chip. Each DAC converts 5 bit digital values to analog currents to bias the receiver and the transmitter.

Although the shift register output fluctuates during pattern loading, a slave latch on the parallel output preserves stable data until the entire pattern is loaded. Loading utilizes 35 clock cycles, while the Load/Hold pad is strobed. The on-chip clock generator creates appropriate two phase non-overlapping clock signals used by the shift register. All cells are static and can hold data in the absence of clock signals.

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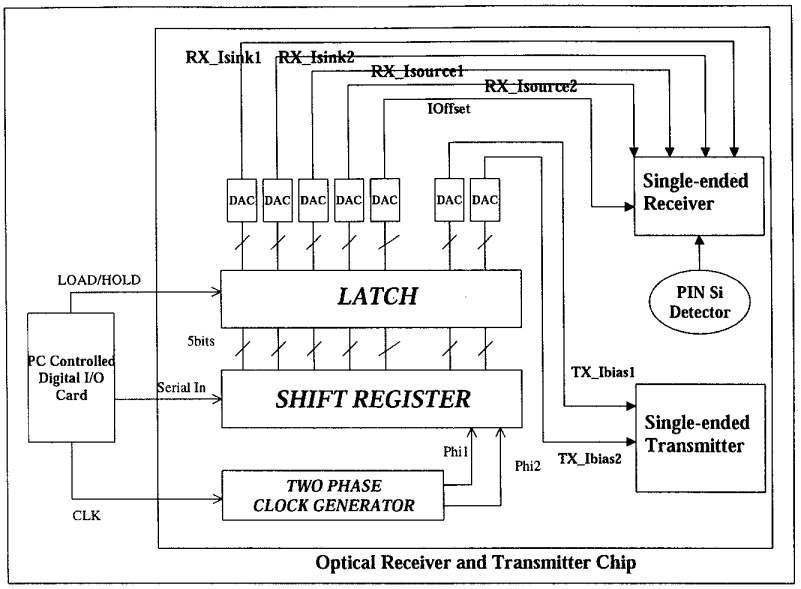

Figure 1. Schematic of chip

The layout of the IC is shown in Figure 2. An array of Si PiN detectors generates current outputs based upon optical input, and is connected to the receiver input. Due to the potentially very small magnitude of these signals, the receiver must have multiple accurate bias sources. The transmitter is designed to modulate the light emitting diode (LED) integrated onto this chip using two bias sources.

The system employs a large number of minimum-geometry DACs and digital control logic. To achieve the resolution necessary in a wide variety of applications, the system utilizes an overlapping DAC scheme. This system provides a superior solution to analog feedback in many cases where parameter adjustment must rely on signals that are not necessarily analog in nature. Additionally, an adaptive trimming algorithm has been devised to control the system in a real-time mode.[1, 3]

This basic shift register cell is a static D flip-flop. A 35-bit shift register may be constructed by cascading these cells. An incoming bit is sampled on SR In when Phi 1 is high and it is available on SR Out when Phi 2 goes high. This bit is then injected to the next shift register cell and to the transparent latch. When the Load/Hold line goes high, the shift register input value will be available on the output line. When this line goes low, the output is held independent from the shift register output.

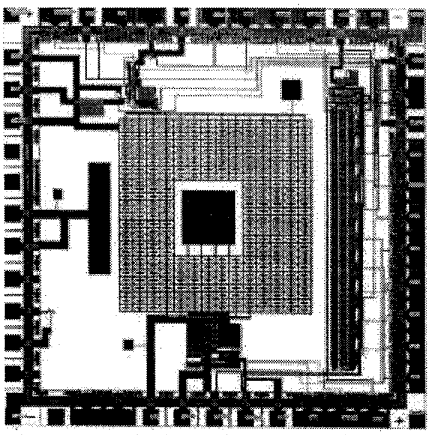

Figure 2. Optical Receiver/Transmitter Chip with Integrated Bias Solution

3. TEST RESULTS

Test results from this circuit are presented in Figures 3, 4, and 5. In important result from Figure 3 is that the output bias currents from the seven DACs are extremely linear to the five bit input digital values. The maximum current ranges from 120 μA to 130 μA, and the minimum current ranges from 15 μA to 18 μA. These currents are sufficient to bias the single-ended receiver and the single-ended transmitter on this chip. With these bias currents, the receiver works up to 5-10 MHz, as

shown in Figure 4, and transmitter also works well, as shown in Figure 5. A range of biases were generated by the CMOS Bias Bus to bias the receiver and the transmitter, which worked under all of the bias conditions shown in Figure 3. Thus, it is possible to use the CMOS Bias Bus for optical receiver and transmitter biasing instead of using noisy off-chip bias sources. These test results have demonstrated that the CMOS Bias Bus can be used to successfully bias the receiver and transmitter, thus dramatically reducing pad counts in mixed signal ICs.

	Minimum Value (00000)	(01111)	Mid-Range Value (10000)	Maximum Value (11111)
RX_Isink1	15.2uA	69.4uA	70.1uA	122.4uA
RX_Isink2	15.8uA	69.2uA	69.8uA	121.3uA
RX_Isource1	16.2uA	71.0uA	71.2uA	120.7uA
RX_Isource2	16uA	71.8uA	72.4uA	128.9uA
RX_Ioffset	18.6uA	74.4uA	75.2uA	136.8uA
TX_Ibias1	15.6uA	70.2uA	70.9uA	122.2uA
TX_Ibias2	14.2uA	69.7uA	71.7uA	119.2uA

Figure 3. Experimental results of output currents for Receiver and Transmitter with Adaptive Digital Bias Control.

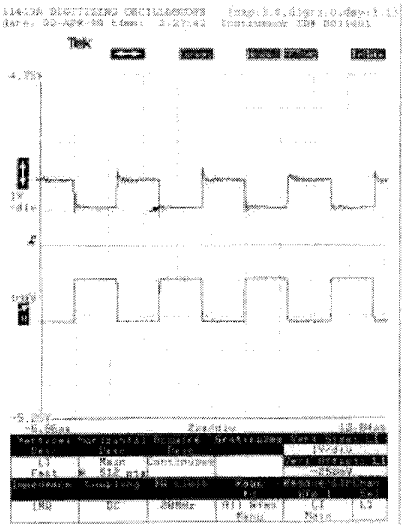

Figure 4. Output of Receiver with Digital Bias Control (Mid-range value: 10000).

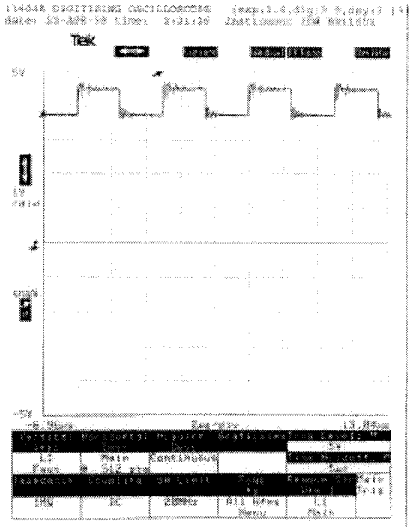

Figure 5. Output of Transmitter with Digital Bias Control (Mid-range value: 10000).

4. CONCLUSION

The results of the design and testing described in this paper demonstrate that a significant improvement in the design of compact high-resolution, high-precision mixed signal ICs such as optoelectronic interface circuits is available using an integrated on-chip adaptive bias solution in a standard digital CMOS process. It is usually undesirable to provide biasing solution to the highly sensitive optoelectronic circuits from off-chip

due to noise and limited pincount. This improvement allows substantial reductions in pad counts of chips that require many off-chip bias sources. This thus enables sensitive optoelectronic interface circuits to be designed in a mixed signal environment with reduced cost, size, and complexity, and with high precision.

5. ACKNOWLEDGMENT

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