RTD/CMOS Nanoelectronic Circuits: Thin-Film InP-Based Resonant Tunneling Diodes Integrated with CMOS Circuits

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***Abstract*— The combination of resonant tunneling diodes (RTD's) and complementary metal-oxide-semiconductor (CMOS) silicon circuitry can offer substantial improvement in speed, power dissipation, and circuit complexity over CMOS-only circuits. We demonstrate the first integrated resonant tunneling CMOS circuit, a clocked 1-bit comparator with a device count of six, compared with 21 in a comparable all-CMOS design. A hybrid integration process is developed for InP-based RTD's which are transferred and bonded to CMOS chips. The prototype comparator shows sensitivity in excess of 10^6 V/A, and achieves error-free performance in functionality testing. An optimized integration process, under development, can yield high-speed, low power circuits by lowering the high parasitic capacitance associated with the prototype circuit.**

***Index Terms*— III–V compounds, resonant tunneling diodes, thin-film integration.**

I. Introduction

THE ongoing need for improved speed and density in high-performance multifunctional electronics has motivated extensive research into the transfer and bonding of electronic and optoelectronic devices to host substrates, including silicon [1]–[5]. Hybrid thin film integration of III–V devices onto CMOS circuitry is a promising technique which has been successfully applied to optoelectronic circuits, allowing each component to be independently optimized with proven technologies at relatively low cost [6]–[8].

The resonant tunneling diode (RTD) is well known for its intrinsic bistability and high-speed switching capability due to negative differential resistance (NDR). The NDR characteristic has been exploited in novel digital integrated circuits combining RTD's and transistors, enabling greater functionality than transistor-only circuits, including digital logic [9], [10] and low-power, high-density memory cells operating at room temperature [11]. Functional density can be further improved by using vertically stacked RTD's in multistate memory and logic [12], [13]. Analog circuits are also achievable, and a prototype 4-bit, 2-Gbps flash-ADC has been implemented [14].

The inherent bistability of the RTD eliminates the need for circuit feedback in comparators, with switching time limited only by the capacitive load on the RTD. With reported switching times of 1.5 ps [15], comparators operating at 20 Gbps clock rates are possible. The high gain of the RTD NDR allows conversion from the analog input signal to the digital domain in one stage. The RTD has been used in several high-speed analog front-end circuits, including oscillators, mixers, frequency multipliers, and RF detectors [16]–[19].

We have developed a process to integrate III–V resonant tunneling devices with conventional CMOS circuitry, and have recently demonstrated the world's first resonant tunneling CMOS circuit: a clocked 1-bit comparator. The resonant tunneling devices are fabricated on an InP substrate and transferred to a CMOS die using a thin-film transfer and bonding process. These prototype circuits are being used to evaluate the advantages of tunnel devices in CMOS circuit topologies, and help in defining the roadmap for monolithic resonant tunneling CMOS IC's with the advent of an integrable silicon resonant tunneling component.

II. Fabrication and Expermental Procedure

The RTD layers were grown using molecular beam epitaxy on an InP growth substrate. A cross-sectional view of the RTD structure is shown in Fig. 1(a). The $In_{0.53}Ga_{0.47}As/InAs/In_{0.53}Ga_{0.47}As$ quantum well serves to increase the peak-to-valley ratio (PVR) by increasing the separation between quasibound resonant states due to the lower effective mass of InAs over InGaAs, and by lowering the first resonant voltage. The barriers are formed by two symmetric $In_{0.52}Al_{0.48}As/AlAs$ layers, which determine the peak current density. Although the use of InAlAs in the barrier reduces the PVR, it is employed because strain limits the thickness of the AlAs thickness to 25 Å, with peak current density reliably controlled by the thickness of the InAlAs prebarrier [11]. For the RTD's that were integrated, a 30 Å prebarrier results in a peak current density of 12 A/cm^2. The relatively low RTD peak current reflects the need to match the RTD current to the current drive capability of the CMOS circuitry.

After the RTD mesas are etched and a 500 Å Si_3N_4 passivation layer is deposited, a via is etched to the RTD mesa. A polyimide layer is spin-coated and cured. In addition to planarizing the top surface of the thin-film device for bonding, the 3-μm polyimide layer reduces the parasitic capacitance between the top contact and n-InGaAs bottom layer of the thin-film structure. A via surrounding the RTD mesa is etched

Manuscript received July 21, 1998; revised November 2, 1998.

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Publisher Item Identifier S 0741-3106(99)01779-6.

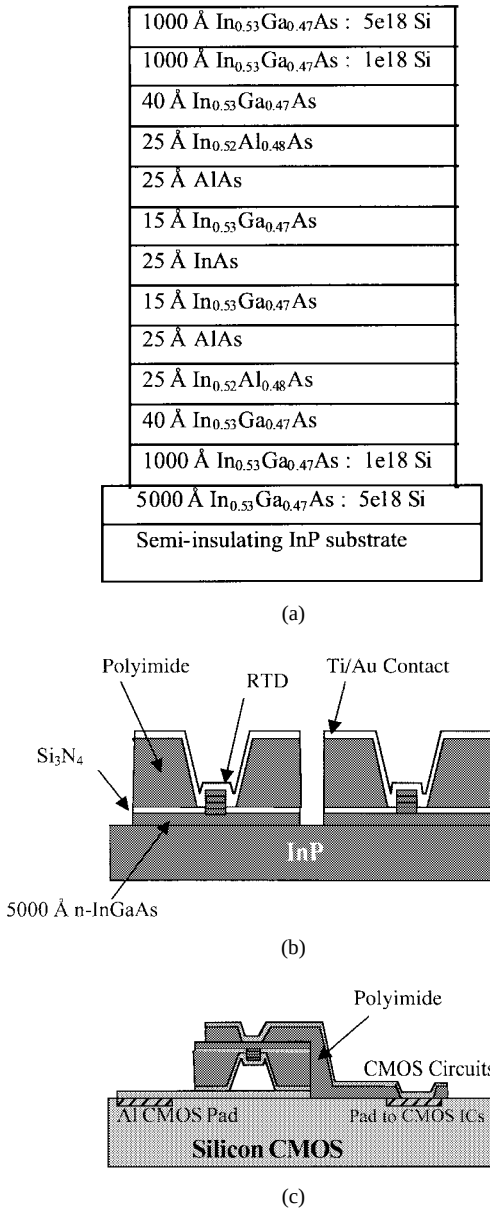
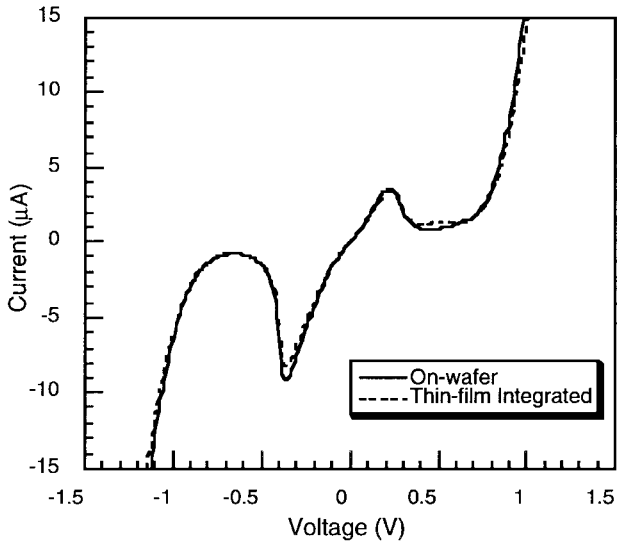
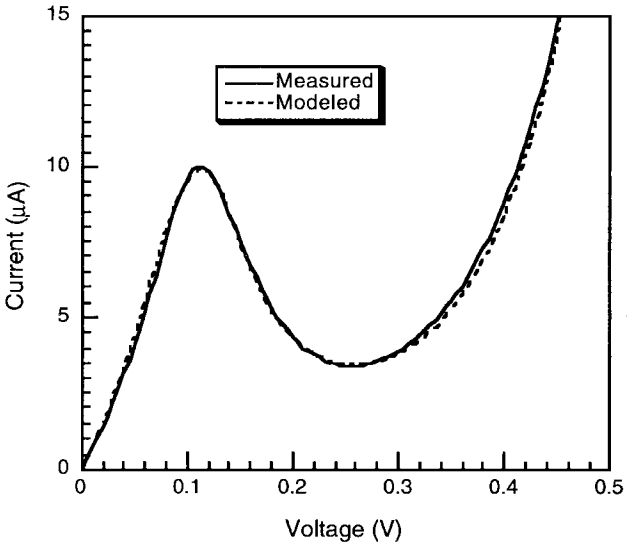


Fig. 1. Thin-film integration of RTD's to CMOS. (a) RTD layer structure as grown by molecular beam epitaxy. (b) Planarized RTD's are then individually isolated and separated from the InP substrate and aligned and bonded to (c) the CMOS chip.



(a)



(b)

Fig. 2. (a) On-wafer versus fully integrated RTD $I-V$ characteristics for a 36-μm^2 RTD, showing good agreement. (b) Measured versus SPICE modeled RTD $I-V$ characteristics.

in the polyimide by reactive ion etching (RIE), followed by contact patterning and a 200/4000 Å Ti/Au metallization. Subsequently, a self-aligned etch of the polyimide, Si_3N_4 passivation, and the 5000 Å bottom n-InGaAs layer isolates each RTD. The final on-wafer structure is shown in Fig. 1(b), with only the InP substrate linking the RTD's. The InP substrate is removed by a combination of mechanical polishing and wet chemical etching with HCl. The RTD is then metal-to-metal bonded to a standard foundry CMOS circuit using an alignable thin-film integration process as shown in Fig. 1(c) [6]. Subsequent post-processing includes the application of a polyimide layer to serve as an interlevel dielectric, and via etching to the RTD and the aluminum CMOS circuit pad. Finally, a second Ti/Au layer contacts the back of the flipped RTD die and connects the second RTD terminal to the CMOS circuitry. The thin-film RTD's show no degradation from the on-wafer characteristics, as seen in Fig. 2(a).

The combination of an accurate RTD model and an integration process that preserves the device characteristics enables design optimization. The silicon circuitry was designed for foundry CMOS fabrication and was simulated using a physics-based model for the RTD's. A comparison of the measured and modeled $I-V$ characteristics for a low current density RTD is shown in Fig. 2(b).

III. Results and Discussion

Several prototype CMOS circuits have been designed for integration with low current density RTD's. The prototypes include basic building blocks for low-power and high-speed circuit functions, including: multistate static access memory,

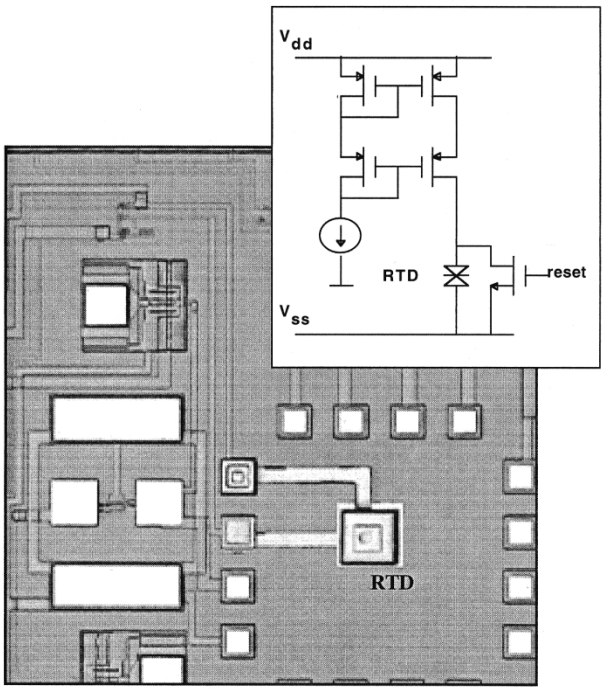


Fig. 3. An integrated RTD/CMOS comparator. The RTD die measures 95×95 μm, with a 16-μm diameter RTD. The circuit schematic is given in the inset.

tunneling binary SRAM, comparator, amplifier, and logic gates.

A prototype CMOS comparator was fabricated in an 0.8-μm foundry CMOS technology for integration with RTD's with peak currents below 200 μA. A photomicrograph of the integrated circuit is shown in Fig. 3(a), along with the circuit schematic. The comparator function is achieved by a transition between the bistable states of the biased RTD, eliminating the need for more complicated circuitry in CMOS designs to provide positive feedback and latching. We find that the device count is reduced from 21 in an all-CMOS design to six in the RTD/CMOS design. The biasing network places the RTD in its low-voltage state, near the peak current. When the injected current from the input causes the total RTD current to exceed its peak current, the circuit switches to the high-voltage state and latches. The external clock resets the comparator to the low-voltage state. The response of the circuit with a sinusoidal input is shown in Fig. 4. The response agrees well with simulation. The abrupt transition of the output is clearly shown at the threshold voltage of 1.1 V, allowing the comparator to be used as a high-sensitivity receiver. In addition to the comparator results reported, nMOS/RTD building blocks such as a Schmitt-trigger and transimpedance amplifier have been demonstrated, also showing greatly reduced component counts over comparable all-CMOS designs.

To demonstrate improved performance over all-CMOS circuits, the RTD/CMOS integration process must be improved to lower the parasitic capacitance. An optimized process currently in development is shown in Fig. 5(a). The RTD device capacitance itself is reduced by scaling the RTD area down from 16 μm^2 or more to 2 μm^2, and increasing the peak

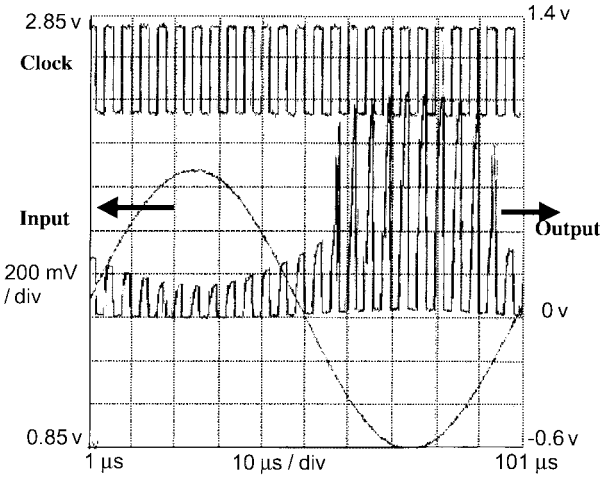
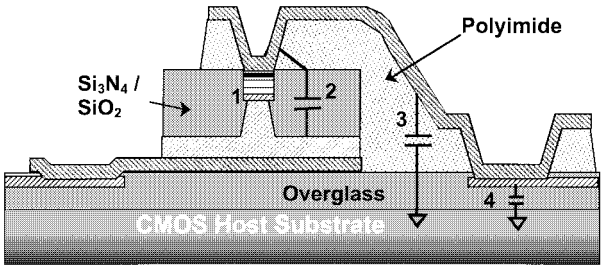
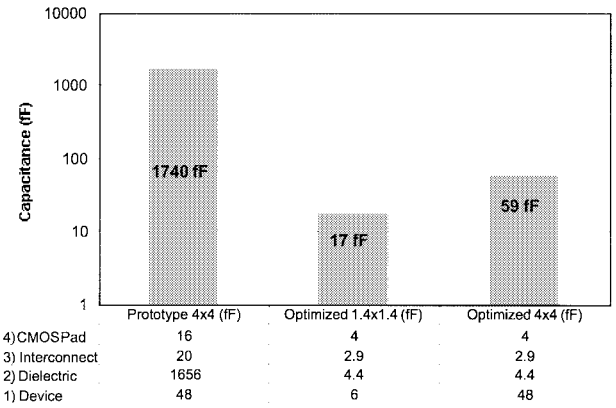


Fig. 4. Transient operation of the RTD/CMOS comparator.



(a)



(b)

Fig. 5. Distribution of the parasitic capacitance of a thin-film integrated RTD. (a) There are four sources of parasitic capacitance associated with the integrated RTD: 1) device capacitance of the RTD, 2) parallel plate capacitance through the dielectric of the transferred RTD die, 3) interconnect capacitance, and 4) pad capacitance of the aluminum pad. (b) The overall parasitics of the fabricated prototype and the optimized structure illustrated in (a). The estimated total capacitance of the optimized structure is dominated by the device capacitance for RTD's above 2×2 μm.

current density. The large capacitance through the 500 Å Si_3N_4 surrounding the RTD mesa can be eliminated by employing a thicker, planarizing Si_3N_4/SiO_2 dielectric for passivation instead of only Si_3N_4. The interconnect capacitance to the conductive silicon substrate is lowered by shortening the interconnect. Finally, the capacitance of the 40×40 μm aluminum pad to the CMOS circuit is minimized by scaling the pad to 20×20 μm. The distribution of and estimated

improvement in capacitance over the prototype process is illustrated in Fig. 5(b).

IV. Conclusion

To our knowledge, these results represent the first demonstration of integrated nanoelectronics on silicon circuitry. Prefabricated InP-based RTD's have been integrated to foundry CMOS circuits using planarization and thin-film integration processes, to realize circuits with improved function and reduced device count. Basic analog and digital building blocks have been demonstrated: comparator, Schmitt-inverter, and transimpedance amplifier. In addition, logic and static memory standard cell prototypes are in progress. Finally, a reduced parasitic integration process is under development which will provide high-performance nanoelectronic CMOS components.

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