Accurate High Speed Empirically Based Predictive Modeling of Deeply Embedded Gridded Parallel Plate Capacitors Fabricated in a Multilayer LTCC Process

Ravi Poddar, *Member, IEEE*, and Martin A. Brooke, *Member, IEEE*

***Abstract*— A novel technique is presented for the accurate, rapid, high frequency, predictive modeling of parallel plate capacitors with gridded plates manufactured in a multilayer low temperature cofired ceramic (LTCC) process. The method is empirical in nature and is based on the concept of incrementally constructing the model for a structure from well characterized individual building blocks. Building blocks are characterized by the use of test structures and measurements, and are modeled using passive lumped circuit elements. This method is applied to the predictive modeling of deeply embedded gridded parallel plate capacitor structures. The procedure has been experimentally verified, with accurate predictions of behavior obtained up to the second self resonance for large area gridded parallel plate capacitors. Since lumped element circuits are generated by this method, structure prediction speed is determined by circuit size and simulator small signal analysis time. The method is versatile and is well suited for circuit design applications.**

***Index Terms*— Capacitor, circuit models, gridded plane, low temperature cofired ceramic, LTCC, predictive modeling, S-parameters.**

I. Introduction

With advances in technology, there is a continuous thrust toward higher levels of system integration and miniaturization. New technologies have been developed which allow for the transferal of passive components away from on top of a printed circuit board to within the substrate. One technology which shows great promise for large system level area reductions is multilayer low temperature cofired ceramic (LTCC) [1], [2]. The LTCC process can support well over thirty layers of metal, each on a thin ceramic tape substrate (several mils thick), with interconnectivity between layers achieved by the use of vias. LTCC is very attractive for embedding of inductor and capacitor structures, and even resistors if a high resistivity material is used.

The LTCC passive structure system is three-dimensional (3-D) in nature, and such structures suffer from parasitic effects in all three dimensions. Due to the thinness and high dielectric constant of the ceramic tape, parasitic couplings are usually quite large. Clearly, in order to effectively design systems which utilize this technology, parasitic effects must be taken into account. Modeling of full 3-D systems has proved to be very computationally expensive in the past. In this paper, a novel modeling methodology is presented for the accurate, high speed predictive modeling of gridded parallel plate capacitor structures fabricated in a LTCC process. Experimentally verified results will be presented, showing very good agreement between results predicted using the developed method and actual measured data.

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II. LTCC Structure Modeling Background

LTCC passive systems usually consist of many levels of thin dielectric material, with conductors present on the various layers as necessary. Connections between layers are achieved by the use of vertically stacked trapezoidal vias with catch pads on each layer. To complicate matters even further, the LTCC structure causes "humps" in areas of metal coverage, and as a result, the stacked substrate has very uneven thickness after the cofiring procedure. These are just a few of the issues involved in modeling of LTCC systems, not taking into account any material related nonidealities associated with the actual manufacturing process.

Due to these concerns, previous predictive modeling efforts in this area were almost entirely limited to the use of full wave 3-D numerical tools based on techniques such as the finite element or difference methods [3]–[7]. Numerical electromagnetic methods usually are very time consuming for complex structures. In addition, structures generally need to be completely resimulated even if the input definition is modified only slightly, with little capability for the reuse of previous results. Another important issue that should be considered is that most full wave solvers generate field patterns or S-parameters which may not be easy to incorporate in a standard SPICE-like circuit simulator that would be used for circuit design applications. Wideband circuit models would be preferable for compatibility and portability reasons, but generating them from S-parameters can prove to be quite time consuming. All of these limitations contribute to making LTCC system design a difficult and time consuming task.

III. Modeling Procedure

A. General Method

A novel method of full 3-D embedded gridded parallel plate capacitor structure predictive modeling and simulation is presented in this paper, based upon the generation of circuit domain passive element models [8], [9]. This procedure involves determining a set of fundamental building blocks for the capacitors, and then designing test structures comprised of combinations of those blocks. The test structures are fabricated and measured up to a desired frequency, and the electrical contribution to the overall response by the building blocks is determined. Equivalent circuits of each of the building blocks are then extracted using a hierarchical extraction procedure. These building block equivalent circuits are then be used to construct a large area gridded plate capacitor circuit that is geometrically comprised of the blocks. Simulation of the constructed circuit in a standard SPICE compatible circuit simulator provides an accurate prediction of the behavior of the new structure in a fraction of the time and using far fewer resources than a traditional EM/RF solution methodology. The model of the new structure is verified experimentally by comparing the predicted response with that measured directly from the manufactured structure. It is important to note that the gridded parallel plate capacitor structure that is predicted in this paper is constructed entirely from the building blocks, and the electrical behavior of the structures is based only upon the behavior of the individual building blocks.

B. Choice of Structure

In LTCC processes, metal is screen printed onto the ceramic tape substrate. This procedure creates limitations with respect to metal coverage. As a result, the process which was used had a specified design rule which limited guaranteed unbroken metal coverage area to be relatively small. This directly limited the dimensions of solid parallel plates that might be used for the design of standard solid-plate parallel plate capacitors. The LTCC process is well suited for the design of large area capacitors that might be used, for example, for decoupling purposes. In order to overcome the metal area design rule, and still be able to generate large area capacitors, a design was developed which replaced the solid parallel plates of the capacitor with gridded plates (Fig. 1). It was estimated that due to the many fringing fields, the gridded plate capacitor might approximate the actual capacitance achieved by the use of solid plates. The gridded parallel plate capacitor would also be quite difficult and time consuming to model using standard numerical techniques, due to the large number of corners and edges in the structure, and would prove to be a good test for the developed modeling method.

C. Detailed Modeling Procedure

The first step involved in the modeling procedure was a determination of the various building blocks that would be required to model the gridded parallel plate capacitor devices. The structures were to be fabricated in a 12 layer LTCC process, and it was decided to design the top layer of the capacitor to be on layer 10 and the bottom layer on layer 11, with ground connections on the bottom layer; layer 12. The metal width used was 10 mils for both plates, and the grid size was also held constant, with "holes" of 30 $\times$ 30 mils. These constraints lead to the definition of only three building blocks that would be required for modeling the capacitor structures. The three building blocks were the ground-signal-ground probe pad, one uncoupled material square, and one grid square of the capacitor. The grid square actually consists of four vertically parallel line segments, with each parallel line segment corresponding to the upper and lower plate segment of the capacitor. The actual size of each block is chosen such that the physical dimension of the material being modeled is less than 1/10 the wavelength of the maximum frequency of interest. This is not a strict requirement, since the user can chose any model that they see fit (e.g., specialized hspice transmission line models or behavioral models), but for this case it simplifies the model extraction process. The building blocks are shown in Fig. 2.

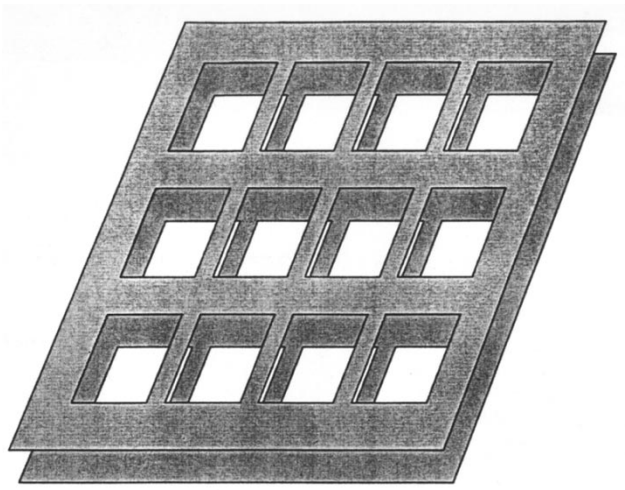


Fig. 1. Diagram of gridded parallel plate capacitor.

In order to model the building blocks, two test structures were designed and fabricated (Fig. 3). The first test structure was simply two probe pads connected by a length of line on the interconnect layer. The probe pad was designed such that the interface was on the top layer for probing, with 12 layer deep via stacks for connecting to ground probes to the ground plane, and an 11 layer deep via stack for connecting the signal probe to the interconnect layer. This test structure would aid in the characterization of the probe pad and the interconnect material. The second test structure was simply the probe pads connected to a 3 $\times$ 3 grid square parallel plate capacitor. This test structure would allow us to model one square of the gridded parallel plate capacitor (consisting of four vertical parallel line segments), taking into account fringe effects and couplings to the ground layer.

IV. Processing and Measurement

The LTCC structure was designed using integrated circuit design tools within the Cadence software environment. A tech-

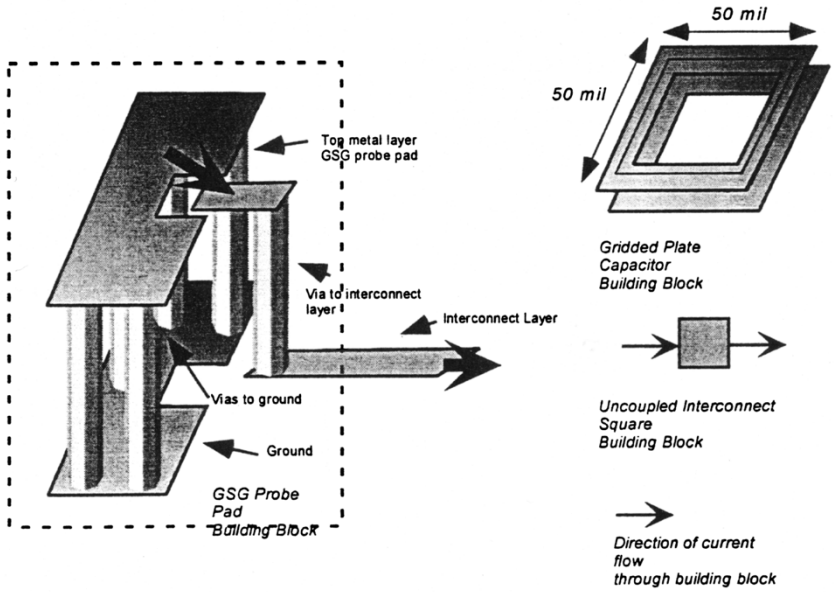


Fig. 2. Building blocks for gridded parallel plate capacitor modeling.

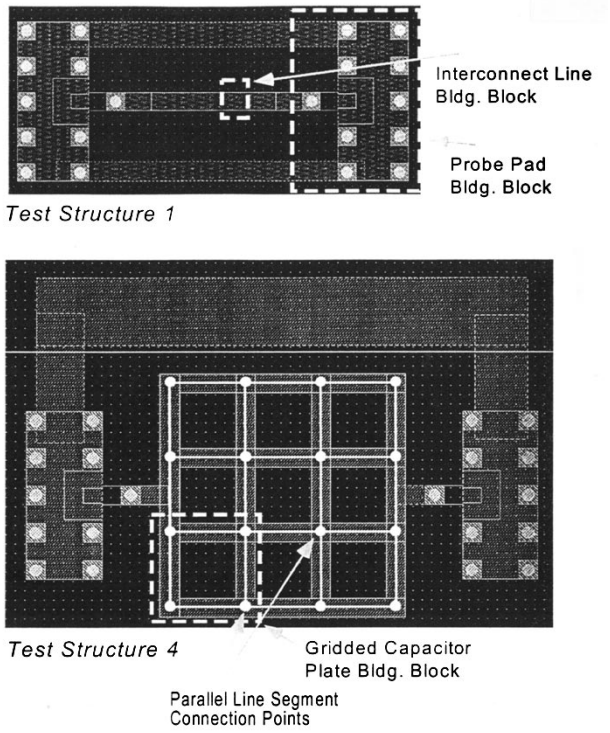


Fig. 3. Test structures for building block characterization.

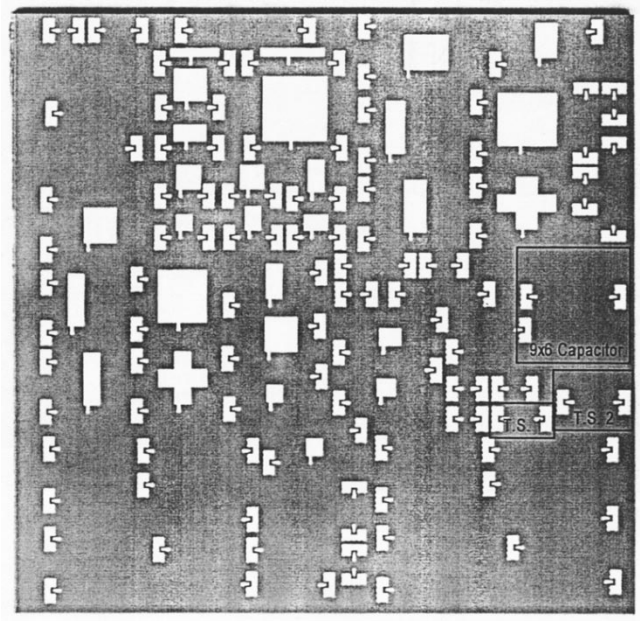


Fig. 4. Fabricated LTCC coupon with location of test structures and 9 × 6 capacitor. Only exposed top layer is visible.

nology file was developed with respect to design specifications supplied by National Semiconductor Corp., through whom the coupon was fabricated. The design utilized 12 layers of ceramic tape of dielectric constant 7.8, with each layer of tape being 3.6 mils in thickness. Interconnectivity between layers was achieved by using stacked vias. The embedded structures were interfaced to by using ground-signal-ground probe pads on the exposed top layer, with signals reaching the embedded layers through vias. The test structure coupon was designed with many different structures, and is shown in Fig. 4. First pass fabrication success was achieved.

The structures were measured using network analysis techniques. A HP 8510C network analyzer was used in conjunction with a Cascade Microtech probe station and wide pitch ground-signal-ground configuration probes. Calibration was accomplished using a supplied substrate and utilization of the line-reflect-match (LRM) calibration method. Data was gathered for each of the test structures at over 200 frequency points between 45 MHz and 5 GHz and stored with the aid of computer data acquisition software and equipment.

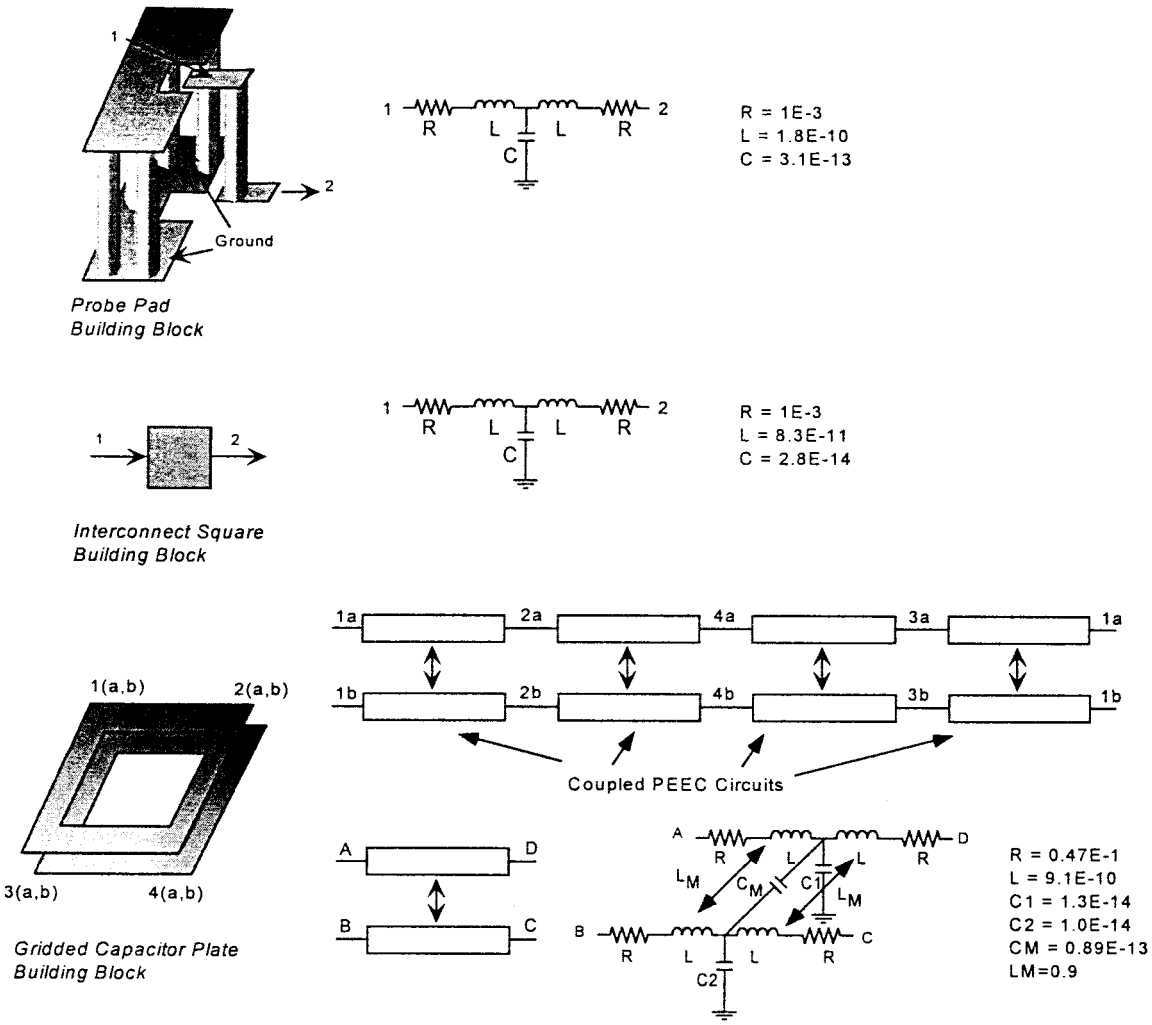


Fig. 5. Equivalent circuits and extracted circuit parameters for building blocks.

V. Modeling and Parameter Extraction

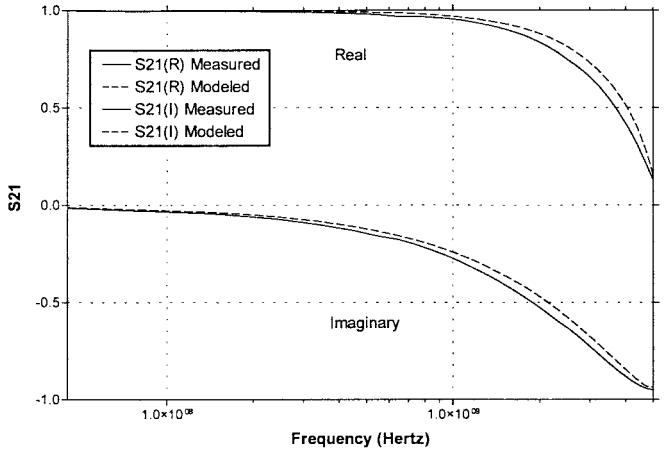
Once S-parameter measurements of the test structures were taken, circuit models were extracted for the various building blocks. The fundamental circuit used is based on the partial element equivalent circuit (PEEC) [10] which has been used extensively for interconnect analysis [11] and general 3-D high frequency structure simulation [12]. The overall building block equivalent circuits may be comprised of a combination of these with modifications to take into account building block topology and various coupling phenomena.

The extraction of the circuit model parameters was achieved in several steps. Due to the highly nonlinear nature of the generated system equations with respect to circuit parameter values, a procedure of hierarchical optimization with respect to measured S-parameter data was chosen. The optimization algorithm chosen was Leavenberg–Marquardt [13], and all optimizations and simulations were done using the Hspice circuit simulator on Sun SPARCstation 20 series workstations. The starting point or initial guesses of the circuit parameters were crucial for correct optimization results, and this was approximated directly from the measured data. In general, good results are obtained using this procedure.

Both test structures were optimized with respect to measured S-parameter data, and their individual building block equivalent circuits were extracted. The measured versus optimized results for the test structures are shown in Figs. 6 and 7. As can be seen from the plots, very good agreement has been obtained for both S_{11} and S_{21} for both test structures. The building blocks, equivalent circuits, and extracted circuit parameters are shown in Fig. 5.

VI. Results

The extracted building block models were used to predict the behavior of a large area gridded parallel plate capacitor. The large capacitor was of rectangular shape with a grid size of 9×6 (250×370 mils), having a plate area more than 50 times that of the building block (Fig. 8). An equivalent circuit of the large capacitor was constructed using the building block equivalent circuits. Specifically, probe pad, material square, and the grid square building blocks were used, with the parallel coupled PEEC circuit elements of the grid square building blocks arranged as a two-dimensional (2-D) grid, with one coupled circuit segment for each line segment of the capacitor.



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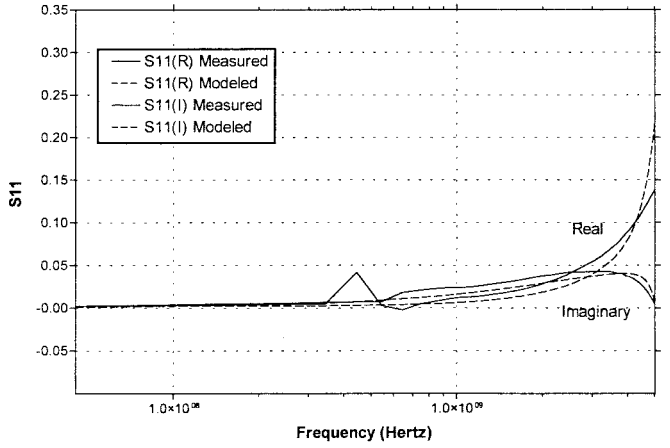
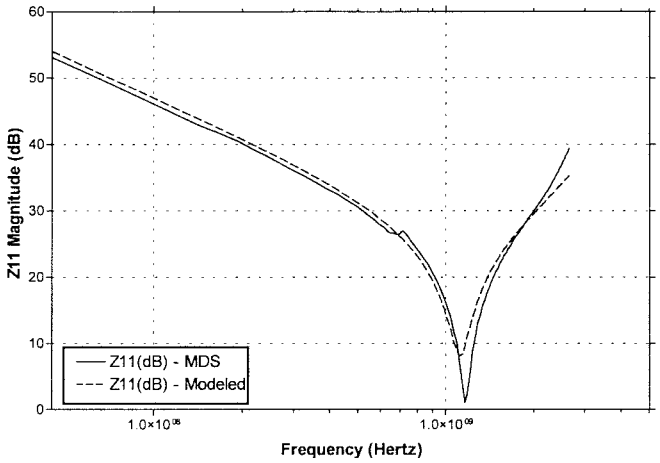
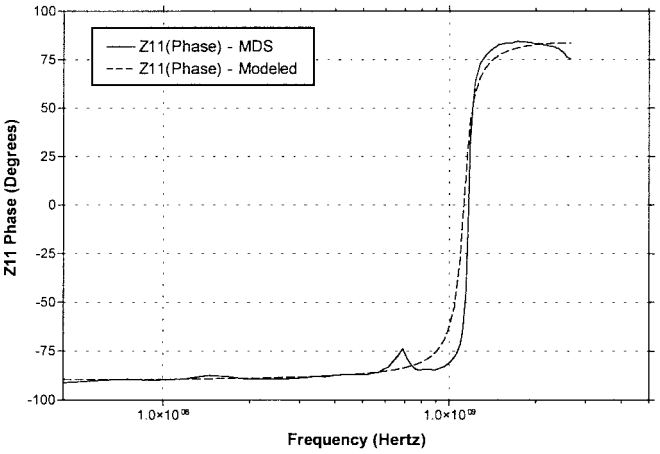


(b)

Fig. 6. Test structure 1 optimization results (a) S_{11} results and (b) S_{21} results.



(a)



(b)

Fig. 7. Test structure 2 optimization results (a) Z_{11} results and (b) Z_{21} results.

This resulted in a circuit consisting of over 500 inductors, 250 mutual inductors and 250 capacitors.

The generated circuit model for the 9 $\times$ 6 capacitor was simulated and results were compared against actual measurements. Z-parameters were considered, in particular Z11 or the input impedance was investigated by grounding the inner terminal of the structure. The results of the prediction versus actual measurements are shown in Fig. 9. As can be seen from the results, extremely good agreement is obtained in both magnitude and phase for Z_{11} up to the second self-resonance of the device at approximately 1.2 GHz. The capacitor itself is only capacitive up to $\sim$400 MHz, and beyond this it experiences a phase change to make it appear inductive before turning capacitive again. The second resonance is most probably a result of higher order parasitics which have been taken into account in the model; however, the device is no longer a capacitor beyond the first resonance, and is generally not operated in this region. It is interesting to note that the capacitance of this structure is 42 pF, while a solid parallel plate capacitor of the same dimensions would be 45 pF, indicating that the fringing fields in this case make up almost entirely for the lost plate area. Modeling errors are small, and are the result of ignoring edge effects and process variations.

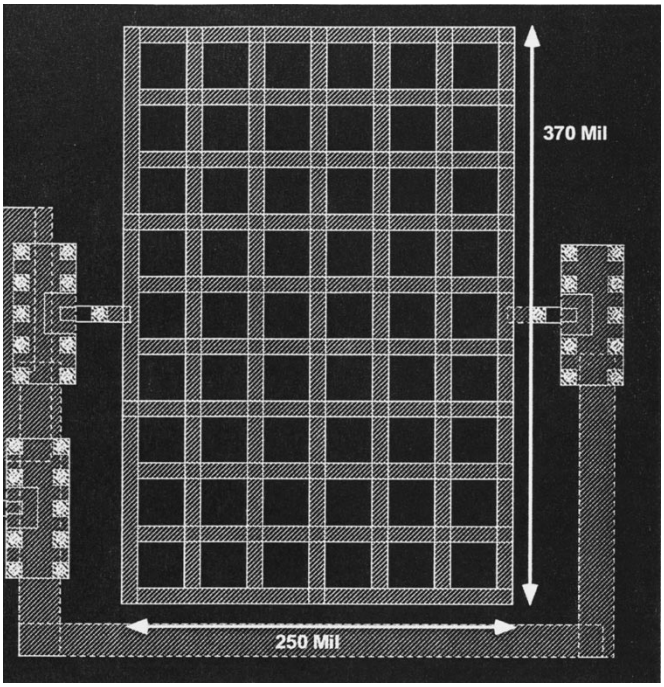
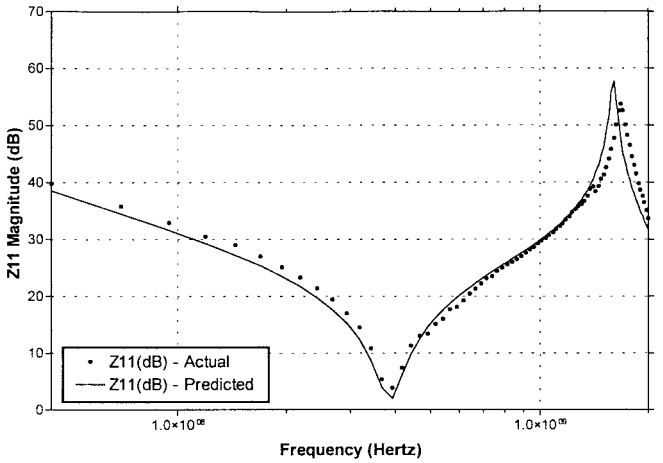
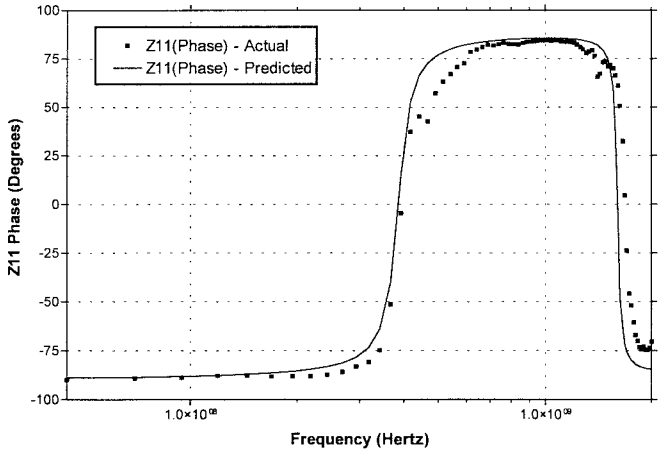


Fig. 8. Large area gridded parallel plate capacitor to be modeled.



(a)



(b)

Fig. 9. Predicted and measured results of Z_{11} for large are gridded parallel plate capacitor. (a) Magnitude. (b) Phase.

It is important to note that the behavior prediction of the large structure was obtained only from test structure measured data. The same building blocks could also be used to predict the behavior of any other structures geometrically composed of them. Since a circuit model of the structure was produced, analysis time was only dependent upon the circuit size and complexity. In this case, the large capacitor circuit required less than 30 s to simulate on a Sun SPARCstation 20 computer. This short simulation time makes it practical for a designer to modify the structure and resimulate it quickly to see results, thereby making the method very useful for design purposes.

VII. Conclusion

In this paper a novel modeling methodology has been described and experimentally demonstrated for the modeling of complex geometry full 3-D embedded gridded parallel plate capacitors fabricated in a LTCC process well beyond the first self resonance of the device. The empirical nature of the method takes into account processing and material effects and nonidealities. In addition, the method generates circuit models which simulate very quickly in a standard circuit simulator, and is considerably faster than using a numerical 3-D full wave method for similar analysis. The predictive modeling method shows great promise for the modeling of regular multilayer complex fully 3-D passive devices, and the high speed and versatility of the method also make it very well suited for circuit design applications.

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