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Three Dimensional Smart Pixel Integration of a GaAs-Based Detector Array Directly on Top of Silicon Circuits

Christophe Camperi-Ginestet, Brent Buchanan, Yiqin Wang, Nan Marie Jokerst,
Martin A. Brooke, and Mark G. Allen
Georgia Instutute of Technology
Microelectronics Research Center
Atlanta GA 30332-0269

Abstract

A smart pixel imaging array of GaAs-based thin film photodetectors has been integrated in three dimensions directly on top of silicon neuromorphic oscillator circuits. Photomicrographs of the integrated assembly and test results are presented.

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Smart pixel arrays such as focal plane image processors that incorporate both photodetectors and processing circuitry on the same substrate enable some preprocessing of input image information, but also have the disadvantage that both detection and processing devices compete for valuable silicon real estate [1, 2]. A detrimental effect of this competition is that a trade-off between the percentage of the image sampled by the photodetectors (the fill factor) and the complexity of the processing circuitry is unavoidable. Using the epitaxial liftoff to create thin film devices, we have constructed a simple focal plane processor with three dimensional electrical interconnect between the photodetector array and the processing circuitry which lies directly underneath the detectors. This enables a high fill factor for the top detector layer without influencing the area available for signal processing circuitry which lies on the second layer. In addition, since each detector is individually connected to the silicon circuitry which lies beneath it, the information in each pixel of the incident image is simultaneously processed by the circuit, thereby realizing massively parallel processing of the image information.

The fabricated three dimensional imaging array consists of a four by four array of 250 μm x 250 μm GaAs P-i-N photodetectors which was integrated directly on top of a silicon circuit that was manufactured using the MOSIS foundry standard 2 μm process. Each silicon circuit in the 4 X 4 array is a current controlled oscillator, as shown in the photomicrograph in Figure 1a. The core of the oscillator is a loop of three digital inverters, with one of the inverters current limited through current mirrors controlled by the photodetector. The photodetector current thus regulates the switching speed of this inverter stage, which in turn then regulates the frequency of the oscillator. The output of each circuit in the array is also buffered and driven off chip.

The neuromorphic circuit was planarized using spun-on layers of polyimide (Dupont 2611). After each polyimide deposition, the layer of polyimide was bake at 120 ^{o}C for 20 minutes. The total thickness of these four layers was 15 μm. After all of the layers have been spun on, the polyimide was cured at 410^{o}C for one hour. A 120 nm thick layer of Al was then deposited onto the polyimide, and, using standard photolithography, 20 μm x 20 μm vias were etched into the Al followed by a plasma etch which extended these vias into the polyimide. The plasma etch stoped when the metal pad on the silicon circuit was exposed at the bottom of the via. The Al was then removed using a wet etch, and Ti/Au was sputter deposited into the vias and on top of the polyimide, forming 250 μm x 250 μm contacts on top of the polyimide (which were each connected to the silicon circuit), as shown in the photomicrograph in Figure 1b. These are the pads onto which the detectors were then bonded.

The thin film P-i-N detectors devices were fabricated using epitaxial liftoff. The lattice-matched detector structure was: GaAs (substrate)/ AlAs (undoped, 200 nm)/ AlGaAs (n_o=2.5 10^{17} cm^{-3}, 0.5 μm thick)/ GaAs (undoped, 1.1 μm thick)/ AlGaAs (p_o= 10^{19} cm^{-3}, 0.5 μm thick). A p-type contact (AuZn/Au) was deposited onto this structure, and a four by four array of 250 μm x 250 μm mesas was defined using an etch that etched to, but not through, the AlAs sacrificial etch layer used to separated the detectors from the growth substrate. After the thin film devices were separated from the growth substrate by etching away the sacrificial AlAs layer [3], the array of devices was bonded to a transparent mylar transfer diaphragm.

The detector array (now inverted, with the p-contact facing the silicon circuit) was then aligned with the gold pads on top of the circuit and bonded to the gold-coated polyimide layer. A layer of polyimide was then spun on over the array to isolate the top and bottom of the thin film detector. Once again using an Al mask, windows were opened in the polyimide which lay on top of the devices. A common n-type contact (AuGe/Ni/Au) was then deposited and patterned into ring contacts on top of the thin film detectors. This metal contact is also connected to a common bar on the silicon circuit,

which completes the integration of the detectors to the silicon circuit, as shown in the photomicrograph in Figure 1c.

Previously, the integration of a single metal-semiconductor-metal (MSM) photodetector directly on top an amplifier circuit was reported [3]. For the integration reported herein, we have used AlGaAs/GaAs/AlGaAs P-i-N photodetectors operating at a wavelength of 850 nm. One of the advantages of the P-i-N detectors is that the contacts are located on the top and bottom of the devices, so the vias which connect each detector to the silicon circuitry below can be located beneath the detector itself, thus further increasing the fill factor. The thin film detectors used in this three dimensional integration were also separately tested, and had a dark current of 22 pA at a 0 volt bias.

The three dimensionally integrated smart pixel array was tested using a variable light source incident on the top of each detector. The output of a representative pixel in the array, namely, an integrated detector/oscillator circuit, is shown in Figure 2 for three different illumination intensities. As designed, the larger intensities produce higher frequencies of oscillation, with the circuit producing over seven decades of frequency change corresponding to increasing intensity. Each detector/oscillator circuit in the 4 X 4 array was fully functional, and exhibited a similar response for different illumination intensities.

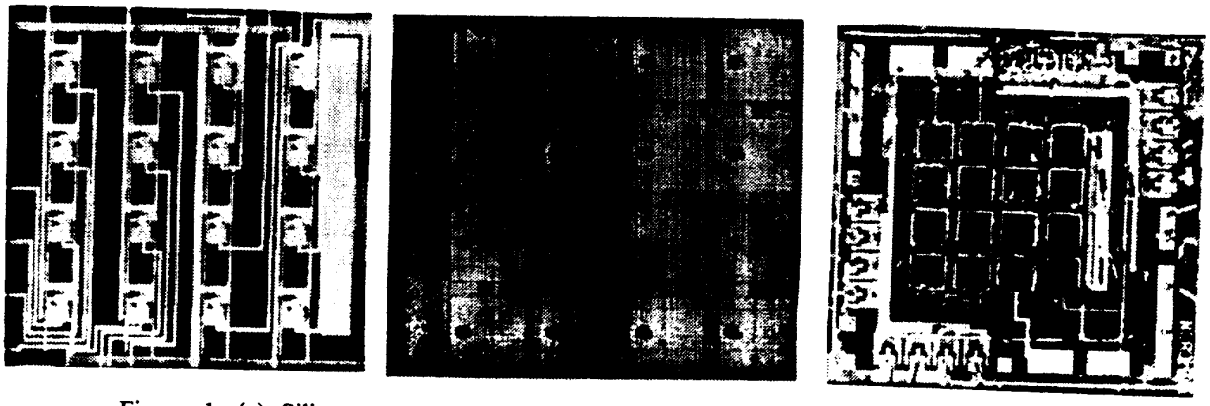

Figure 1. (a) Silicon neuromorphic osciallator circuit; (b) polyimide planarized circuit; (c) completed integration with thin film detectors on top of the planarizing polyimide.

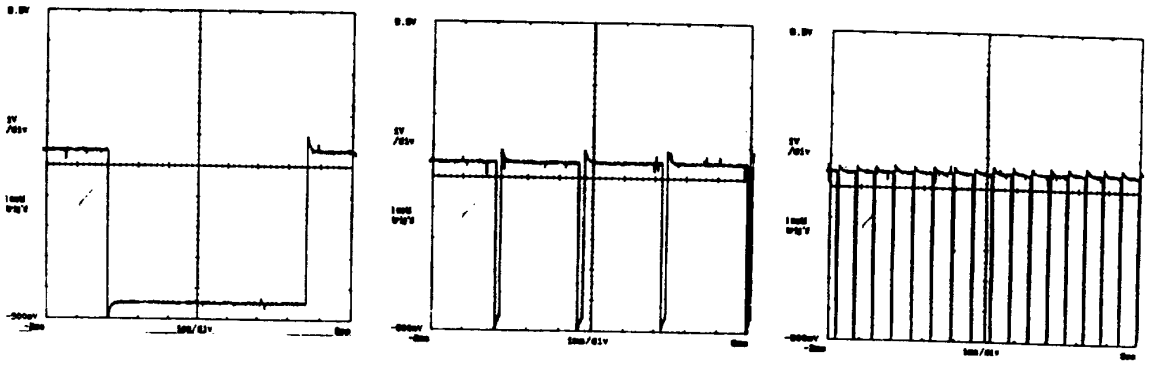

Figure 2. The response of the three dimensional integrated system: (a) low level; (b) intermediate level and (c) high level optical illumination.

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[2] E-S. Eid, E. Fossum, "Real-Time Focal Plane Array Image Processor," *Proc. SPIE-International Soc. Optical Eng.*, 1989, v 1197, p 2-12

[3] C.Camperi-Ginestet, Y.W. Kim, N.M. Jokerst, M.G. Allen, and M.A. Brooke, Phot. Tech. Lett., vol 4, pp 1003-1006, 1992