F1.4
9:40am - 10:00am

Silicon CMOS Optical Receiver Circuit with Integrated Compound Semiconductor Thin-Film P-i-N detector

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Low cost, high complexity silicon CMOS circuitry is a prime candidate for low cost, high performance integrated optoelectronics. For many applications, however, silicon detectors do not operate at the wavelength of interest. Thus the integration of compound semiconductor detectors with silicon circuitry, forming a mixed material integrated system, is an attractive prospect. In this paper we report the integration of GaAs and InP-based thin film P-i-N detectors with a five stage silicon CMOS transimpedance amplifier. This integrated system utilizes low cost foundry silicon CMOS circuitry coupled with thin film devices which are bonded to this circuit in post-processing steps which utilize only standard microelectronics materials and processes to produce a low cost hybrid integrated circuit.

Thin film double heterostructure AlGaAs/GaAs/AlGaAs and InP/InGaAsP/InP photodetectors were separated from the lattice matched growth substrate using selective etching (epitaxial liftoff), and were then each bonded to a host silicon CMOS circuit. To begin this process, an ohmic contact was deposited onto the structure, and the structures were subsequently mesa etched to define 250 μm X 250 μm squares. These devices were then separated from the growth substrate using selective etches [1, 2], and were then contact bonded to a transparent Mylar transfer diaphragm [3].

The five stage silicon transimpedance amplifier circuit was designed at Georgia Tech and fabricated using the MOSIS foundry 1.2 μm digital CMOS process. The optimized CMOS transimpedance amplifier circuit consists of five identical stages with each stage having a current gain of 3. A schematic of the single stage amplifier is shown in Figure 1. Since the amplifier operates in the current-mode, the current signal from the P-i-N detector is fed directly into the input of the amplifier, minimizing the effects of parasitics. The total transimpedance gain is 12,000 ohms when a 50 ohm load resistor is used. The minimum detectable input signal is 150 nA.

To integrate the thin film detector onto the silicon amplifier, a Ti/Au pad is patterned and deposited onto the CMOS transimpedance amplifier pads onto which the detector will be integrated. The detector on the mylar transfer diaphragm, which has been inverted from the as-grown condition, is then aligned and bonded to the Ti/Au pad. A rapid thermal anneal of the integrated circuit causes a strong mechanical bond to be formed between the ohmic contact on the thin film device and the Ti/Au pad on the circuit. The circuit is then spin coated with 4 μm of polyimide (DuPont 2611), hard baked at 120 C for 15 minutes, and cured at 350 C for 1 hour. The polyimide planarizes and isolates the two sides of the detector. An Al mask (120 nm) is deposited onto the polyimide and windows are opened over the circuit pads and the top of the detector. A plasma etch is used to open vias in the polyimide. The top contact for the device is then defined by a lift off process, and a AuGe/Ni/Au contact is evaporated onto the detector, connecting it to the other circuit pad. Figure 2 is a microphotograph of the hybrid integrated circuit.

To test the hybrid integrated device, a commercial 1W pigtailed laser diode was modulated by a current source and pseudorandom signal generator fed through a bias tee. We found that the receiver integrated with the GaAs-based detector operates at speeds up to 80 Mb/s in a non-return-to-zero (NRZ) data format. Fig. 3 shows the output signal (bottom trace) when NRZ pseudorandom data at 80 Mb/s, shown in the top trace, is incident on the detector in the hybrid integrated receiver. A single 5 V power supply was used and the power dissipation of the integrated receiver is approximately 70 mW. The InP-based integrated receiver has been fabricated and is currently under test.

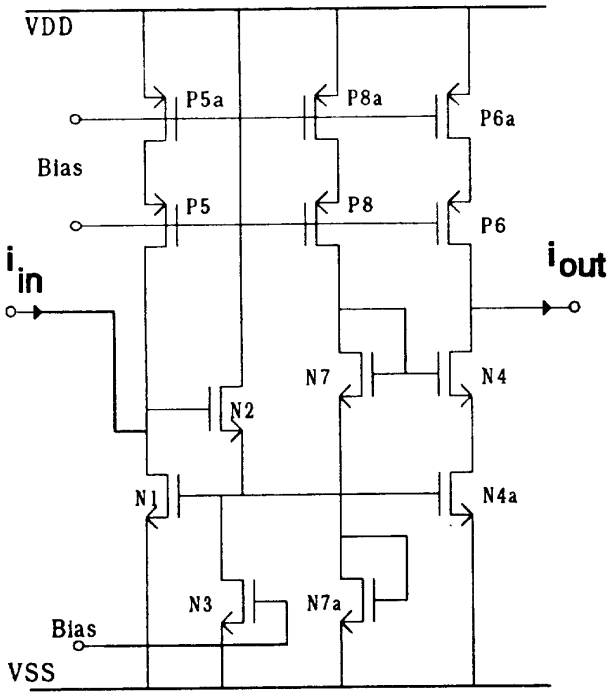

Figure 1. Schematic of a single stage of the transimpedance amplifier.

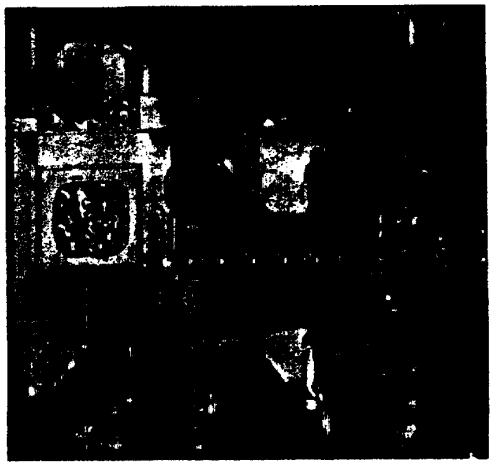

Figure 2. Photomicrograph of the hybrid integrated receiver.

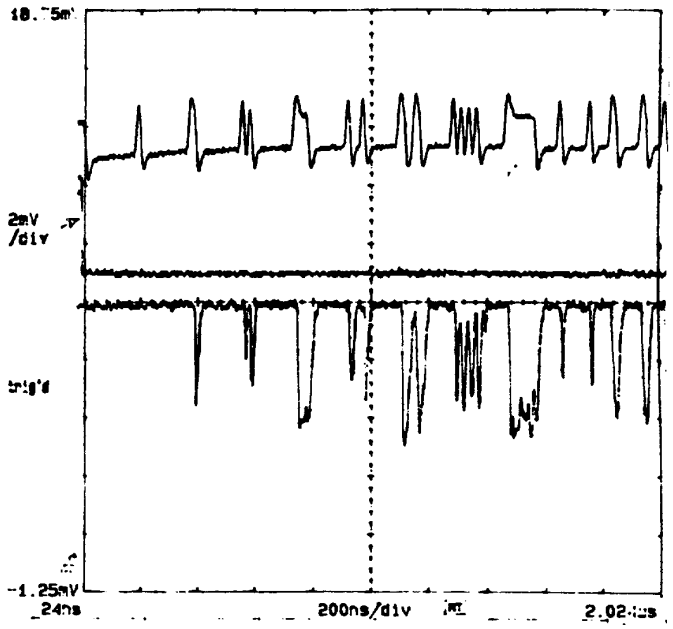

Figure 3. Response (bottom trace) of the hybrid integrated receiver to pseudorandom data (top trace).

[1] E. Yablonovitch, T. Gmitter, J.P. Harbison, and R. Bhat, Appl. Phys. Lett., vol 51, pp2222-2224, 1987

[2] G. Augustine, N. M. Jokerst, and A. Rohatgi, Appl.Phys. Lett., vol 61, pp1429-1431, 1992

[3] C. Camperi-Ginestet, M. Hargis, N.M. Jokerst, and M. Allen, Phot. Tech. Lett., vol 3, pp1123-1126, 1991