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High Speed, Smart Focal Plane Processing Using Integrated Photodetectors and Si CMOS VLSI Sigma Delta Analog to Digital Converters

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High speed imaging applications such as combustion, transMach fluid flow, and aerooptic sensing require a high frame rate image acquisition system with frame rates in excess of 100 kfps (frames per second). Currently, imaging systems implemented using charge-coupled device (CCD) technology with off-chip analog to digital data converters are limited to continuous frame rates of approximately 1 kfps [1]. Analog data transfer bottlenecks, which are limited by signal to noise ratios and the requirement for fast ADCs, are the cause of this low frame rate limitation and the lack of scalability of these imaging systems. Smart pixel imaging systems which implement low speed direct digital ADC at the pixel level translate this data transfer problem to that of parallel digital links, which can be realized with through-Si vertical optical data links [2], which can be used to realize fully scalable smart pixel imaging systems.

This paper reports the first demonstration of a high frame rate smart pixel imaging system which uses an ADC per pixel in an 8x8 integrated detector array. The smart pixel architecture of this system enables frame rates up to 100 kfps operating in continuous imaging mode. This integrated imaging system has been implemented in digital Si CMOS VLSI, and, to realize scalability, has been integrated with an emitter driver circuit for through-Si vertical optical communication down to a second layer of dedicated Si image processing circuitry [3][4].

There are three main building blocks used to realize this smart pixel image acquisition system. The first building block is the integrated photodetector array. Two implementations have been demonstrated herein: Si CMOS and thin film hybrid integrated GaAs-based PiN detector arrays. Figure 1 is a schematic illustration of the smart pixel imaging system, and Figure 2 is a photomicrograph of the integrated GaAs-based 8x8 photodetector array directly on top of the ADC array. This implementation realizes higher fill factor than the monomaterial Si detector array. The second smart pixel system building block is the ADC. Due to the small Si area available underneath each pixel, a compact ADC with high speed and large dynamic range is necessary. A current input sigma delta ADC has been used in the demonstrated system. A sigma-delta ADC is a good candidate for this imaging application because it is immune to component mismatch, and through subsequent digital filtering of the ADC output signals, a tradeoff between dynamic range and frame rate can be achieved. In addition, the digital filtering can remove high frequency noise from the image data, which is impossible with CCD imagers operating at the same frame rate, resulting in an improved signal to noise ratio for the ADC-based system. The final system building block is the ADC readout system. By locating an ADC at each pixel, the readout noise associated with the analog transfer of charge in CCD arrays has been eliminated. The integration of an emitter driver enables a fully parallel, scalable transfer of data down through the Si circuit using a vertical optical link to a second layer of digital processing hardware. Maintaining this fully parallel data link enables the scalable realization of 100 kfps smart pixel imaging systems since each 8x8 array in a larger, tiled system can be associated with a vertical readout link.

The Si and GaAs-based imaging array smart pixel circuits have been fabricated and successfully tested, and the Si imaging array has been extensively tested. Each of the sigma delta ADCs is clocked at 15.6kHz, resulting in a frame rate of 976 fps. The output data is captured using a digital acquisition card in a Pentium-class computer. This test configuration, shown in Figure 3a, is the primary limitation of the measured frame rate. Figure 3b shows the image data displayed on a video screen, which cannot display the measured frame rate. Simulated results indicate a frame rate capability in excess of 100 kfps. To measure this performance, a faster test facility is necessary.

In conclusion, this paper reports the first demonstration of a high frame rate smart pixel imaging system using an ADC per pixel in an 8x8 integrated detector array. This integrated imaging system has been implemented in digital Si CMOS VLSI, and has measured operation of 976 fps, with a projected frame rate of 100 kfps.

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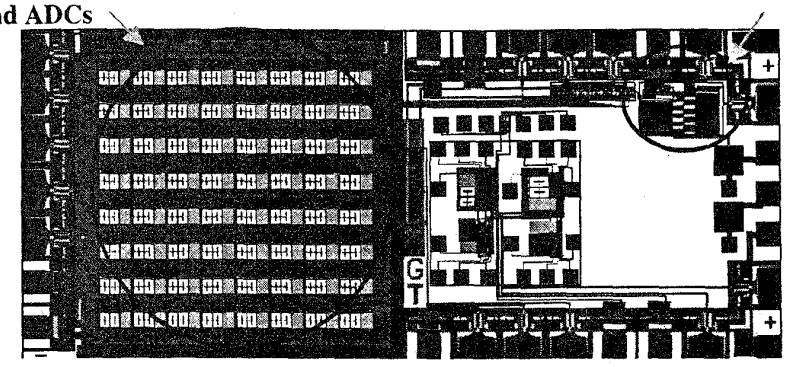


Figure 1. Si CMOS VLSI smart pixel imaging array.

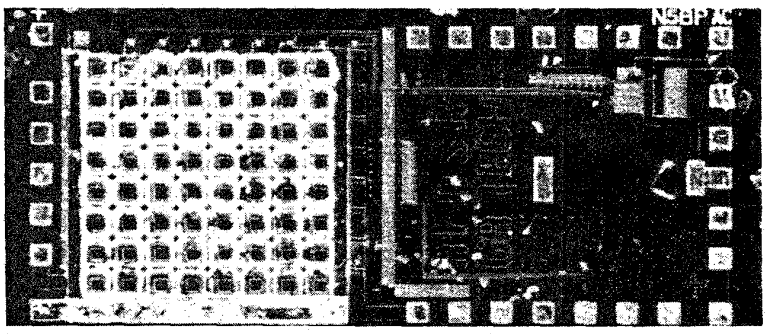
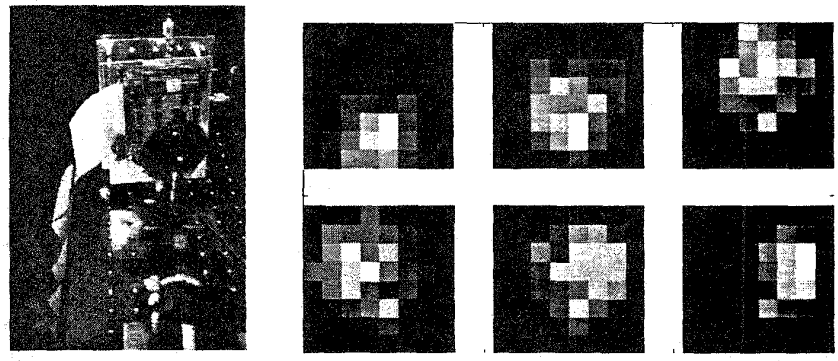


Figure 2. Photomicrograph of hybrid integrated GaAs-based detectors directly on top of sigma delta ADCs to form integrated smart pixel imaging array.



(a) (b)

Figure 3. Test setup with low speed test results

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