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3D Stacked Si CMOS VLSI Smart Pixels Using Through-Si Optoelectronic Interconnections

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A fundamental limitation of smart pixel systems is the interconnection of the pixels to a high level of Si signal processing circuitry. Often, the limited Si area under or surrounding each pixel is insufficient for a high level of Si CMOS VLSI signal processing. Interconnection to more Si circuitry could enable a higher level of signal processing associated with each pixel. However, interconnection of more than two vertically stacked layers of functional Si CMOS signal processing circuitry with vertical optical interconnections has never before been demonstrated. This is essentially an interconnection problem, which is a limitation that also plagues electronic systems [1]. Three dimensionally interconnected systems with vertical optical interconnections can offer solutions to these fundamental electrical interconnection limitations. For example, one such limitation, latency, plagues even highly advanced electrical interconnection technologies such as MCM and HDI interconnection substrates [2]. Architectures in which a critical data path can be routed in three dimensions (to circuit layers above or below) can minimize the path length, and, since the signal is transmitted near the speed of light, the delay usually associated with long electrical interconnections can be reduced. Further, although MCMs enable a high level of electrical interconnection, they are not scalable with increasing interconnection densities and system size [3]. Thus, enabling 3D smart systems using vertical optical interconnections can have profound effects upon electronic and smart pixel signal processing systems. One example of a smart pixel system that utilizes a 3D through-Si vertical optical interconnection for processing of image data from a focal plane array is shown in Figure 1 [4,5].

This paper reports the first demonstration of a three layer, 3D vertically optically interconnected Si smart pixel system. Three layers of standard foundry Si CMOS VLSI circuits, each integrated with long wavelength thin film emitters and detectors (to which the Si is transparent), have been stacked to realize a three dimensional system with optical interconnections between the layers. Each circuit operates both electrically and optically, and optical communication between the three layers has been demonstrated up to speeds of 1 Mbps.

Each hybrid smart pixel Si CMOS VLSI integrated circuit contains analog components designed for implementation in any digital Si CMOS process. Each circuit contains a transmitter capable of DC and AC modulation currents up to 120 mA, a receiver operating in an open loop mode with current gain of 243, and a clocked comparator for data regeneration to digital levels. Hybrid integration of thin film InP/InGaAsP/InP LEDs (λ=1.3μm) and InAlAs/InGaAs/InAlAs MSM photodetectors was used to create the smart pixel integrated optoelectronic circuit (OEIC) [6,7]. Each of the three OEICs in the stacked system was assembled with silicon support pieces to provide mechanical support during wire bonding of the 3D system. The individual layers were aligned using an IR backplane alignment feature of a Karl Suss mask aligner. After all three layers were assembled and attached using an UV and heat curing epoxy, the system was packaged into a 144 pin ceramic pin grid array. Figure 2 shows a photomicrograph of the packaged system.

To demonstrate the vertical optical interconnections in the 3D smart pixel three layer Si CMOS circuit stack, the integrated transmitter and receiver circuits were tested. The vertical communications link between the middle and top layer operated at 1 Mbps with bit error rates of $1x10^{-9}$ with a PRBS of 2^7-1. An infinite persistence receiver eye diagram at 1 Mbps for this channel is shown in Figure 3. The bottom to middle chip channel suffered from decoupling problems in the test network, and functioned at speeds up to 100 kHz. Although the bottom optical communication channel did not operate with low noise, the clean operation of the top channel indicates that, with adequate off-chip decoupling in the bottom channel, that the system will produce high quality operation in both of the vertical optical communication channels.

We have presented the first demonstration of an optically interconnected three dimensional smart pixel system connecting three stacked layers of Si CMOS VLSI circuitry. We have demonstrated vertical optical communication between three CMOS circuit layers with operation speeds up to 1 Mbps. This system demonstrates the viability of implementing optical interconnections for scalable 3D interconnection systems for ultra-smart pixel applications.

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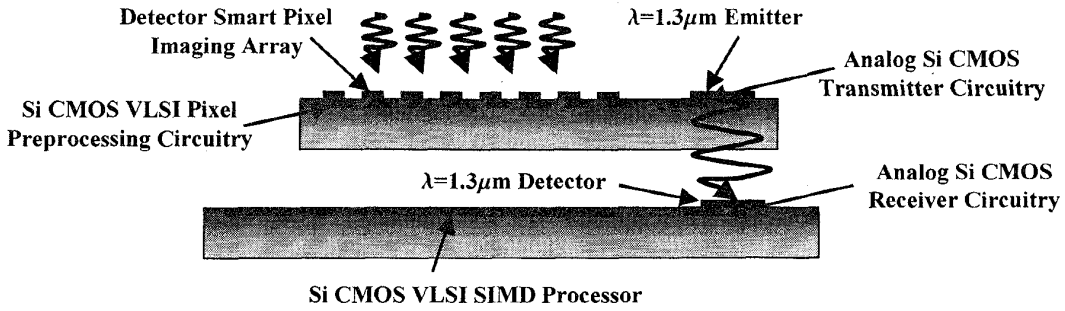

Figure 1: Smart Pixel Focal Plane array with VLSI Processing and Through-Si Interconnection

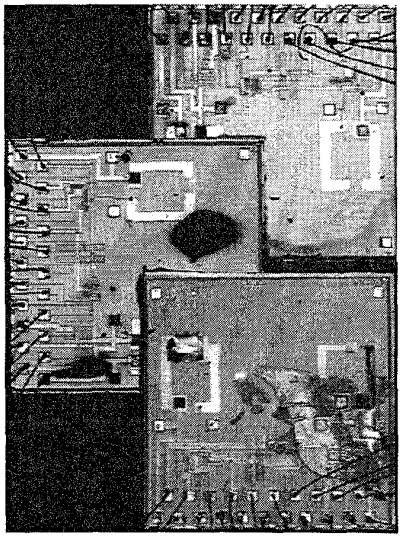

Figure 2: Photograph of the tested three-layer stack with layers focused individually.

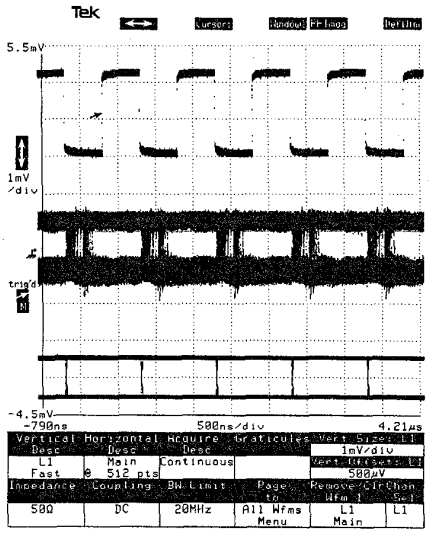

Figure 3: 1Mbps Infinite persistence eye diagram from the output of the top-chip receiver.

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