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INTEGRATED 1.55 µm RECEIVERS USING GaAs MMICS AND THIN FILM InP DETECTORS

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Abstract

A GaAs-based amplifier has been designed with a large area, high and integrated efficiency, thin film InP-based metalsemiconductor-metal photodetector. Thin film integration is a hybrid integration scheme that minimizes the parasitics between the InP detector and the GaAs circuit to the order of integrated circuits.. The GaAs integrated circuits are fabricated using a commercial TriQuint Semiconductor foundry process, demonstrating the use of standard GaAsbased foundry circuits for long wavelength, highly integrated, high speed, low cost photoreceivers. Utilizing thin film integration to minimize interconnect parasitics, a 1.55 μm wavelength receiver has been demonstrated at 1 GB/s, and initial results for a 10 GB/s receiver under fabrication are presented.

Introduction

component in optical key any communication system is the front end Future fiber-optic based photoreceiver. communication systems and distribution networks expecting to take advantage of 1.3 μm and 1.55 μm wavelengths for low dispersion fiber communication require the of InP-based materials photodetector. Monolithic OEIC receivers in InP-based materials have been reported [1,2]. However, the lack of a commercially available foundry process for InP-based circuits indicate cost and access limitations for the widespread utilization of this technology.

For high speed optical transmission systems in the tens of GB/s, very broad bandwidth amplifiers are required. To achieve these wide bandwidths, traveling wave amplifiers, TWAs, based upon the theory of artificial transmission lines have been demonstrated as a suitable topology [3-4]. Because the design of the amplifier is sensitive to the parasitic inductance and capacitances of the circuit, added parasitics and variations in interconnects between the circuit and detector can be detrimental to performance.

Flip chip bonding is one hybrid technology that has been used for OEIC applications [5-6]. Another process is thin film device bonding where only the epilayers of the bonded device are used and the bonding metallization is on the order of the contact thickness, rather than the thicker solder bumps. The thin film process enables the ability to utilize novel structures to improve overall circuit performance, such as in this case, removal of the InP substrate for higher responsivity detectors. An inverted MSM structure (I-MSM) has shown to provide alignment tolerance for detector to fiber connections relaxing the stringency on the packaging requirements.

MMIC Amplifier Design and Integration

The MMIC was fabricated in TriQuint's HA2 process. This process is a GaAs **MESFET** process utilizing implanted depletion mode MESFETs with cutoff frequencies of approximately 20 GHz. The amplifier has been used distributed successfully for MMIC broad bandwidth amplifiers, but one of the limitations to the bandwidth is due to the losses of the gate and drain lines. Cascoding a pair of transistors provides loss compensation to achieve wider bandwidths [4]. In this investigation, the TWA incorporates a cascode pair to extend the bandwidth to the limit imposed by the device's cutoff frequency.

One approach to reduce this cost of the receiver is to design alignment tolerant optoelectronic systems. The I-MSM, with the electrodes on the bottom of the device, overcomes this responsivity disadvantage by eliminating the shadowing effect of the electrodes [7] thus yielding high responsivity, high speed, large area detectors for high data rate, alignment tolerant OEICs. Metal strips (Ti/Au) are deposited on the circuit, the substrate is removed from the epilayer of interest, and the thin film I-MSMs are aligned and bonded to these strips using a transfer diaphragm [5]. The process is diagrammed in Figure 1 and the resulting OEIC is shown in Figure 2(a).

Results

The optical to electrical transfer curve is determined with a HP8703A lightwave network analyzer of an integrated detector and amplifier is shown in Fig 3(a). The optical signal is fed by a single mode fiber to the detector and on-wafer coplanar waveguide (CPW) probes are used to extract the electrical signal. Generation of an eye

diagram demonstrates its suitability for digital operation. A 1.55 μm single mode laser source directly modulated with a pattern generator sends an optical pseudorandom data stream (up to 2^{31-1}) to the receiver which produces the 1 GB/s eye diagram shown in Fig 3(b).

Work is underway to produce a 10 GB/s receiver using a TWA to achieve the wide bandwidths necessary for the high data rate. As shown by Figure 4(a), the TWA has a measured bandwidth of 18 GHz and approximately 7 dB of gain with an HP8510C network analyzer and CPW probes. The return loss up to 18 GHz is below 10 dB at the input and output. The amplifier is driven by a single 3 V power supply and the power consumption of the amplifier is 45 mW. A 10 GB/s electrical eye diagram of the TWA is shown in Figure 4(b).

Conclusion

In this paper, we demonstrate, for the first time, the operation of an hybrid integrated OEIC receiver using a standard GaAs MMIC foundry circuit and a 50 µm diameter thin film InGaAs photodetector. The OEIC operates at 1 GB/s, matching the SONET OC-48 speed specification. A wide bandwidth amplifier for 10 GB/s operation demonstrates a measured RF bandwidth of 18 GHz and an open electrical eye diagram. These results demonstrate the feasibility of the thin film hybrid integration of standard, GaAs-based MMIC circuits with high quality thin film detectors for low cost, alignment tolerant, high speed, long wavelength OEICs.

Acknowledgments

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References

- [1] L. M. Lunardi, S. Chandrasekhar, A. H. Gnauck, C. A. Burrus and R. A. Hamm, "20 Gb/s monolithic pin/HBT photoreceiver module for 1.55 µm applications," IEEE Photon. Technol. Lett., vol. 7, no. 10, pp. 1201-3, 1995.
- P. Fay, W. Wohlmuth, C. Caneau, I. Adesida, "15 GHz monolithic MODFET-MSM integrated photoreceiver operating at 1.55 μm wavelength", *Electron. Lett.*, vol. 31, no. 9 pp. 755-6, 1995.
- [3] S. van Waasen, et. al., "27-GHz Bandwidth High-Speed Monolithic Integrated Optoelectronic Photoreceiver Consisting of a Waveguide Fed Photodiode and an InAlAs/InGaAs-HFET Traveling Wave Amplifier," IEEE Journal of Solid-State Circuits, vol. 32, no. 9, pp. 1394-1401, 1997.
- [4] S. Kimura, Y. Imai, "0-40 GHz GaAs MESFET Distributed Baseband Amplifier IC's for High-Speed Optical Transmission," *IEEE Trans. Microwave Theory Tech.*, vol. 44, no. 11, pp. 1688-1693, 1996.
- [5] M. Makiuchi, H.. Hamaguchi, T.. Kumai, O. Oikawa, O. Wada, "GaInAs pin photodiode/GaAs preamplifier photoreceiver for gigabit-rate communications systems using flip-chip bonding techniques," Electron. Lett., vol. 24, no. 16, pp. 995-6 1988.
- [6] S. Yamaguchi, Y. Imai, S. Kimura, H. Tsunetsugu, "New Module Structure Using Flip-Chip Technology for High-Speed Optical Communication ICs," IEEE MTT-S Digest, vol. 1, pp. 243-246, San Francisco, CA, 1996.
- [7] O. Vendier, N. M. Jokerst and R. P. Leavitt, "Thin film inverted MSM photodetectors" *IEEE Phot. Tech. Lett.*, vol. 8, no. 2, pp. 266-8, 1996.

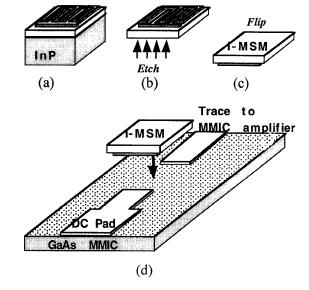
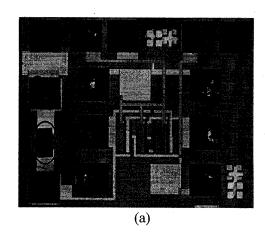


Figure 1: Diagram of thin film integration technique: (a) Fabricate devices (b) Etch away substrate of detector, leaving only the active layers (c) Flip the MSM so that contacts are on the bottom (d) Place onto GaAs MMIC so that pads on I-MSM and MMIC align, anneal to secure metal to metal bond



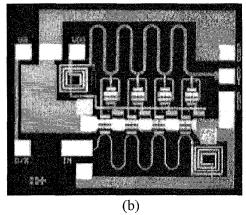
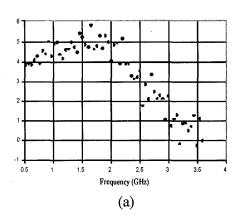


Figure 2: (a) Integrated photoreceiver (b) TWA amplifier



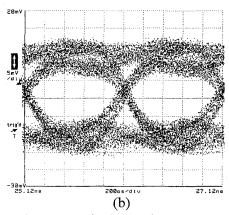
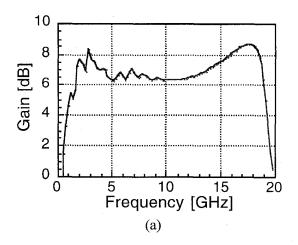


Figure 3: (a) Optical to electrical gain of receiver in dB (b) Eye diagram of the OEIC at 1 GB/s



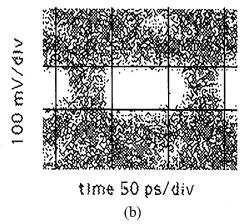


Figure 4: (a) S-parameter response (b) electrical eye diagram of the TWA