Review of RF Packaging Research at Georgia Tech's PRC

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INTRODUCTION

The emergence of wireless applications as perhaps the most financially significant market in recent years , wireless technology has become a global core competency. The demand for increasingly higher rates of data transmission, from voice to video and data, will drive technology to exploiting higher frequencies, where bandwidth for channel capacity is easier to find. The emerging applications of personal communication networks, wireless local area networks, satellite communications and automotive electronics provide the impetus for the wireless electronics thrust.

Consistent with the Packaging Research Center's vision of low cost single level integrated modules (SLIM), the Wireless Thrust is focused on developing integrated solutions for wireless interfaces. The improvements in wireless components come in a few categories: those of the evolutionary type, where gradual improvements will happen as a result of engineering, those of the revolutionary type, where paradigm shifts in approaching the problem are necessary to solve the problem, and regulatory type, where the rules must be changed to allow an alternative approach to the problem. In collaboration with PRC researchers, industrial partners and university partners we are focused upon both revolutionary and evolutionary improvements for emerging wireless applications using the SLIM prototype concept. The PRC is well positioned to impact microwave wireless applications in the 1 to 100 GHz range and to partner with leading industry in several core research areas. The goal is to merge low cost packaging and interconnection approaches with the SLIM concept as applied to the emerging wireless revolution.

In the past 18 months the Wireless Thrust within the PRC has identified core research projects which are critical for the development of the SLIM wireless concepts. In addition, we have established one of the most comprehensive microwave/millimeter wave design and characterization facilities for wireless packaging research in a US university including: four HP 8510 network analyzers (with coverage to 110 GHz), five on-wafer probing systems, on-wafer cryogenic characterization (10K to 300K), on-wafer 2-26.5 GHz noise characterization facilities, and on-wafer load-pull from 8-18 GHz. The focus of the core research projects are the development of the material and structural properties for high frequency applications of SLIM.

The core focus is to develop: (1) Development and analysis of multi-layer microwave assemblies. The goal is to assess the critical technology break points required for SLIM and requirements for SLIM to progress to higher frequencies of operation. This project includes development of SLIM based high frequency test structures for evaluation and study. (2) Development of RF microwave packaging and interconnects for microwave multi-chip assemblies. This project focuses on developing the necessary structural properties for SLIM to operate at mmW frequencies with particular emphasis upon developing vertical interconnects. (3) Development of next generation wireless integration approaches. This project focuses upon applying thin-film integration to develop three dimensional wireless ICs for direct integration with SLIM. A detailed data base development is proposed, based upon PRC SLIM prototypes, to establish measurement based methodology to accurately model entire high density interconnect systems at microwave frequencies. Several industry are currently participating in various capacity with the wireless thrust area including: Cascade Microtech, General Electric, Hewlett-Packard, Hughes, Lucent Technologies, National Semiconductor, Northrop-Grumman, Rockwell, Texas Instruments and Triquint Semiconductor.

MULTI-LAYER MICROWAVE ASSEMBLIES

We have designed various microstrip transmission lines on three-layers of Kapton E® with adhesives as shown in Figure 1. The dielectric data of the polymer and adhesive is found in [1]. The total dielectric thickness including Kapton E® and adhesives is 102 μm. The microstrip transmission lines have coplanar waveguide (CPW) launches. These launches are connected to ground using vertical stacked vias. These stacked vias represent the vertical interconnects to an IC in a cavity.

We use an HP85109C network analyzer (ANA), coplanar waveguide microprobes and a Cascade Microtech probe station to obtain S-parameters. We perform an on-wafer Thru-Reflect-Match calibration prior to measurements on an Impedance Standard Substrate (ISS). We then measure various microstrip transmission lines (Figure 2) which include vertical stacked vias for the ground pads of the coplanar launches. In Figure 3, we show the insertion loss of 50-Ω microstrip transmission lines on polymers and alumina dielectric substrate. The loss performance of the 50-Ω microstrip transmission line on Kapton and BCB is comparable to that of the microstrip transmission line on a 5-mil thick alumina substrate at W-band (75GHz-110GHz). We develop an equivalent circuit model for the vertical interconnect as shown in Figure 4. The L_g, C_1 and C_2 represent the inductance and fringing capacitance of the vertical stacked via. We use the Hewlett-Packard's Microwave Design System to optimize this circuit until the measured and modeled results are well correlated as shown in Figure 5.

We compare the return loss of our interconnect to that of bond wires. The data for the bond wires is reported in [2]. In Table 1, we show that the vertical stacked via interconnect has ultra low parasitics and provides an excellent match. To evaluate its performance, we design a test structure connecting a 50-Ω microstrip line to a 50-Ω stripline using the vertical stacked via as shown in Figure 6. In Figure 7, we achieve the measured return loss of less than 20dB for this structure to 50GHz. We compare the return loss of our structure with one using flip-chip [3]. For the flip-chip case, the two 50-Ω transmission lines are connected using bumps. In Table 2, we show the performance of the vertical stacked via interconnect and bumped flip-chip.

Table 1. Comparison of the return loss of the vertical stacked via and wirebond

Frequency (GHz)	Return loss (dB) of Vertical Stacked Via	Return loss (dB) of Wirebond [2]
10	-38	-12
30	-34	-9
50	-19	-6

Table 2. Comparison of the return loss of two 50-Ω transmission lines connected using the
vertical stacked via and flip-chip

Frequency (GHz)	Return loss (dB) using Vertical Stacked Via	Return loss (dB) using Flip-chip [3]
10	-24	-21
30	-22	-17
50	-20	-15

RF/MICROWAVE PACKAGING INTERCONNECTS

Ball Grid Arrays (BGA) have received great attention as a low-cost, high density microwave integrated system interconnection solution [4]. The BGA multilayer structures have the advantages of reduced size and weight, possibility of mounting cheap ceramic substrates on PCB, compatibility with automatic manufacturing and minimized electrical path to the mother-board. Therefore, the modeling and characterization of BGA packages to microwave frequencies is of great practical interest. This paper presents the first comprehensive approach for characterization of microwave BGA's. A scaleable lumped-element circuit model up to 12 GHz and extendible to higher frequency is presented. The demonstration of the equivalent circuit shows the variation of the lumped element values with the horizontal diameter of the bump.

A schematic of the test structure is shown in Figure 8. The printed circuit board (PCB) consists of two 50 ohm coplanar waveguides (CPW) (A_1 and A_2) on a low-cost Duroid multilayer substrate. A 50 ohm CPW transmission line (B) on Low Temperature Cofired Ceramic (LTCC) multilayer substrate is soldered to the PCB using two balls. The study of the loss and reflection due to the ball interconnect is done using the equivalent circuit model in Figure 9, which is similar to the configuration for a flip-chip transition [5]. C_1 denotes the discontinuity capacitance at the chip, C_2 the discontinuity capacitance at the mother-board, L_1 the inductance of the bump, and R_1, R_2, R_3 model the loss in the interconnection. The approach for deembeding the effect of the interconnection is presented in Figure 10. The values of the lumped elements are obtained by matching the measured S-parameters of the overall attached structure to the cascaded CPW transmission lines, LTCC vias and bump model, as presented in the block diagram in Figure 11. The LTCC grounded CPW and the two LTCC vias have been simulated using SONNET EM simulator. The on-wafer measurements have been taken with an HP85109C network analyzer. The on-wafer line-reflect-match (LRM) calibration has been performed on a Cascade Microtech impedance standard substrate.

The lumped elements values obtained as the result of the deembeding technique are presented in Figure 9. The comparison of the measured and simulated S-parameters of the overall attached structure is presented in Figure 12. Application of this method is demonstrated by analyzing the effect of the via horizontal diameter on the elements of equivalent circuit model. Figure 13 shows the S-parameters of the equivalent circuit compared to a simple via simulation. For several diameters of the bumps, the variation of the reactive elements in the model is presented in Figure 14.

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[2] T. Krems et al, "Millimeter-Wave Performance of Chip Interconnections Using Wire Bonding and Flip Chip," *IEEE MTT-S Digest,* Vol 1., pp 247-250, June 1996.

[3] T. Krems et al, "Advantages of Flip Chip Technology in Millimeter-Wave Packaging," *IEEE MTT-S Digest,* Vol. 1, pp 987-99-, June 1997.

[4] M.S. Cole, T. Caulfield, "A Review of Available Ball Grid Array (BGA) Packages", *Proceedings of Surface Mount International Conference,* pp. 207-213, Aug. 1995.

[5] Hussein H.M. Ghouz and EL-Badawy EL-Sharawy, "An Accurate Equivalent Circuit Model of Flip Chip and Via Interconnects", *IEEE Transactions on Microwave Theory and Techniques,* vol. 44, no. 12, pp. 2543-2554, Dec. 1996.

FIGURES

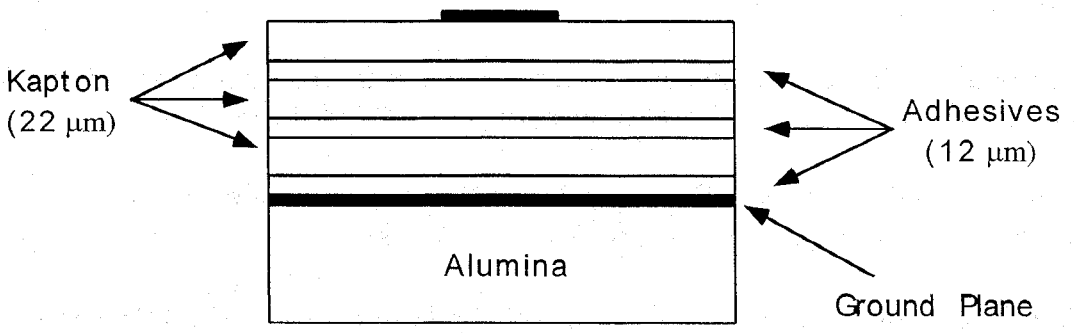


Figure 1. A cross-section of a microstrip line on multi-layer structure

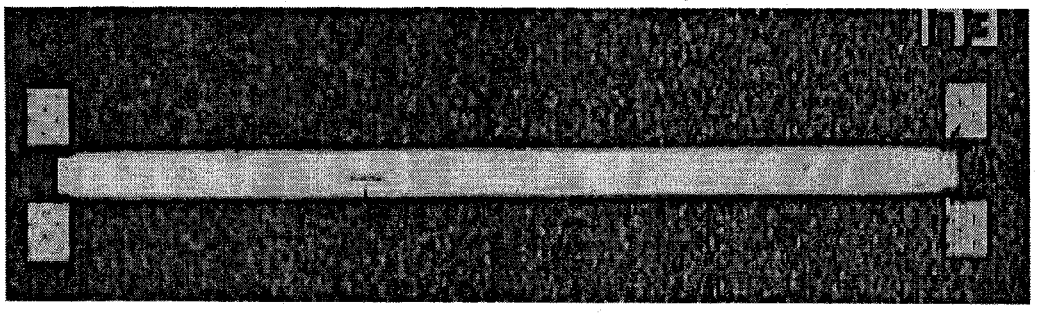


Figure 2. A microstrip transmission line with vertical interconnects at both ends

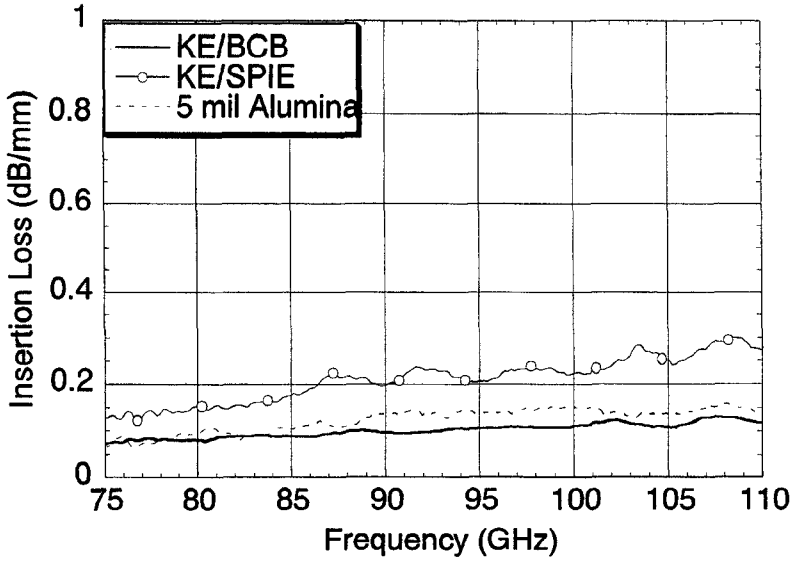
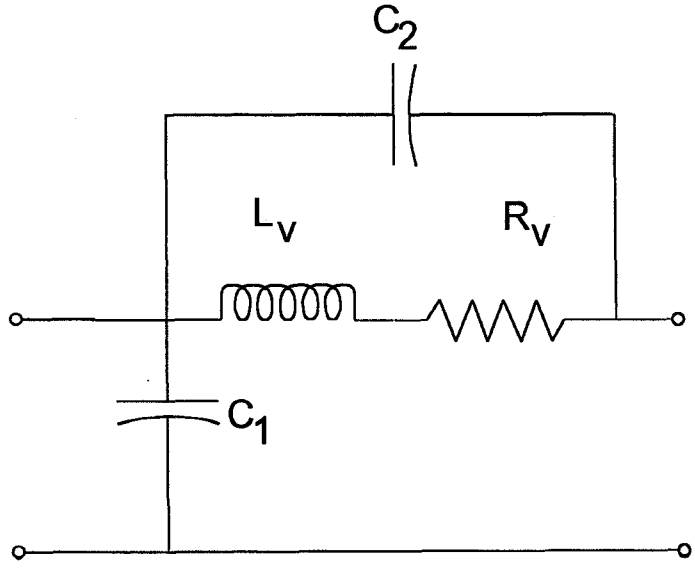


Figure 3. Insertion loss versus frequency data for the following three types of microstrip lines: (1) multi-layer 50-Ω microstrip with Kapton E dielectric and BCB adhesive (KE/BCB), (2) multi-layer
50-Ω microstrip with Kapton E dielectric and SPIE (KE/SPIE), and (3) 50-Ω microstrip on 5 mil thick alumina



L_v = 55 fH, C_1 = 10 fF, C_2 = 9.3 fF, R_v = 0.1 Ω

Figure 4. The equivalent circuit model of the vertical interconnect

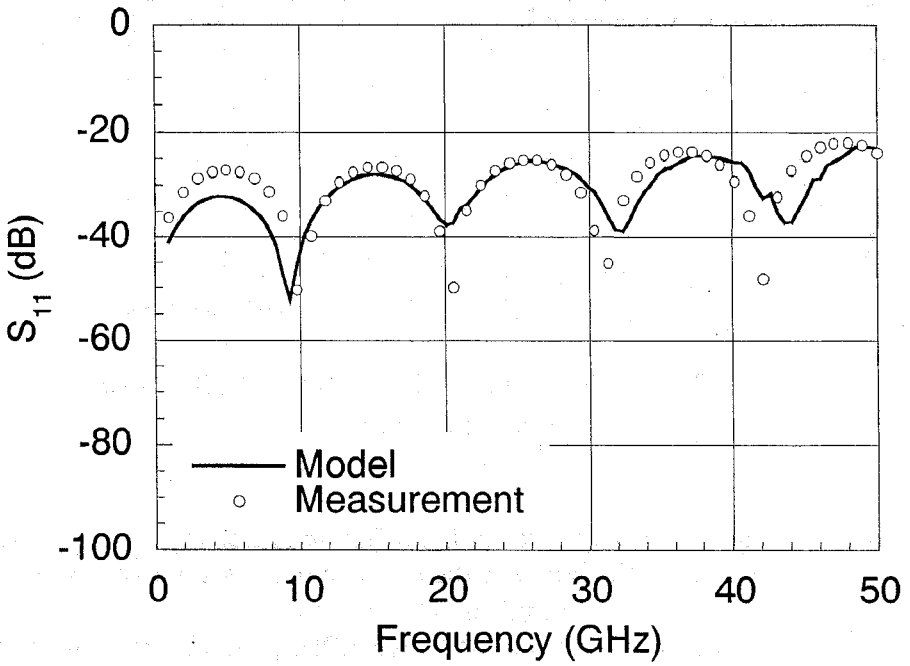


Figure 5. Measured and modeled S_{11} of the 50-Ω microstrip line with the vertical stacked via interconnect

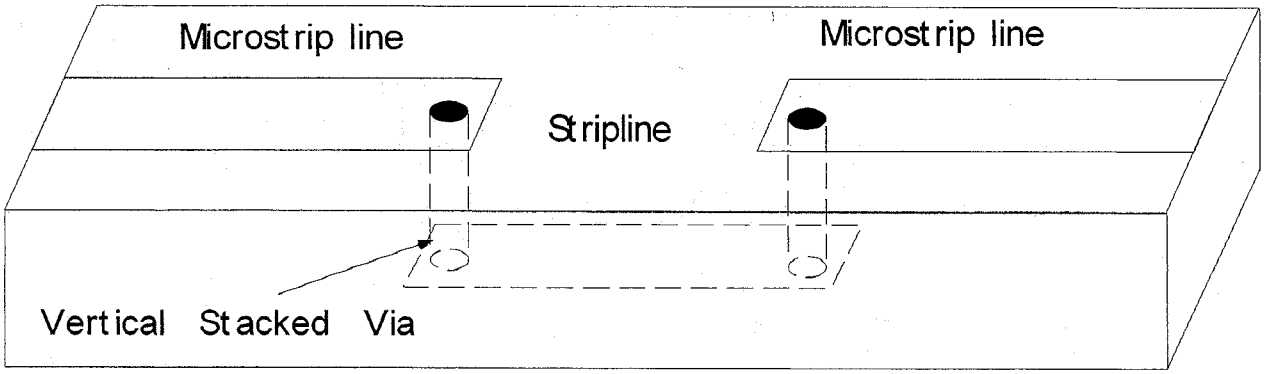


Figure 6. Schematic representation of a microstrip to stripline transition using vertical stacked via

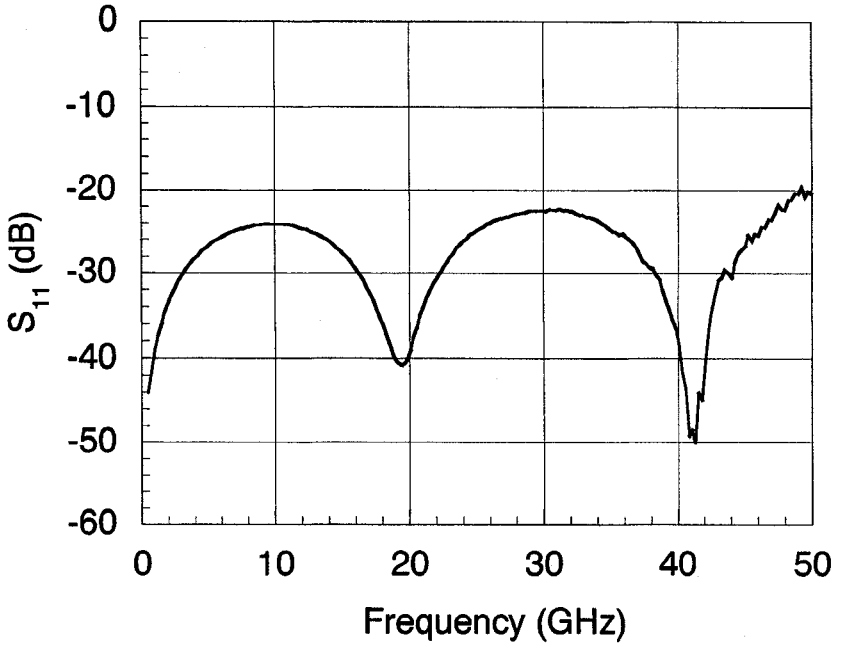
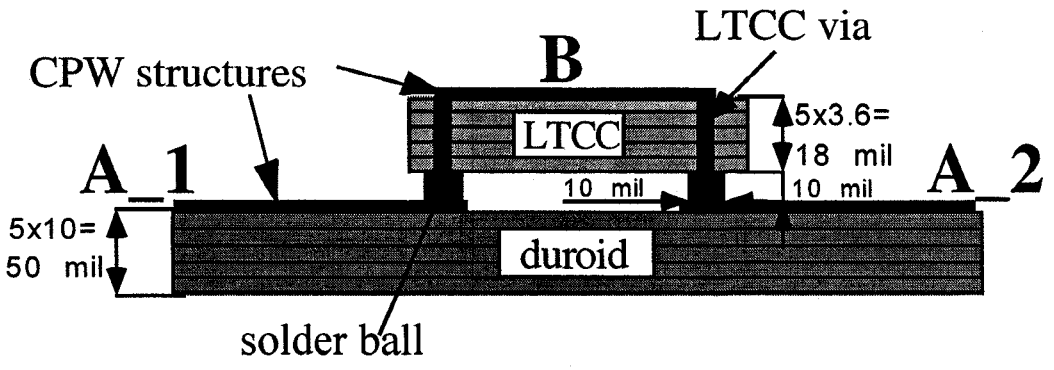
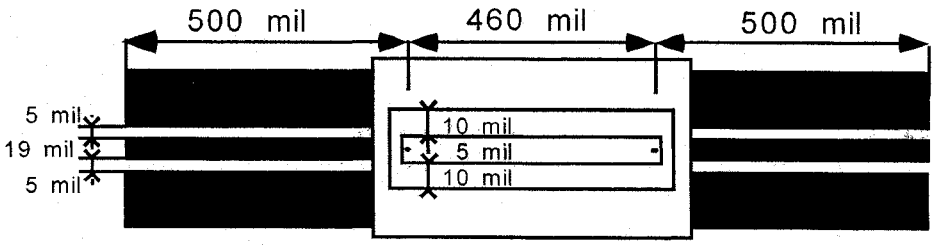


Figure 7. Measured return loss of the 50-Ω microstrip connected a 50-Ω stripline using the vertical stacked via interconnect



a) Side view



b) Top view

Fig. 8. Schematic of the interconnection structure

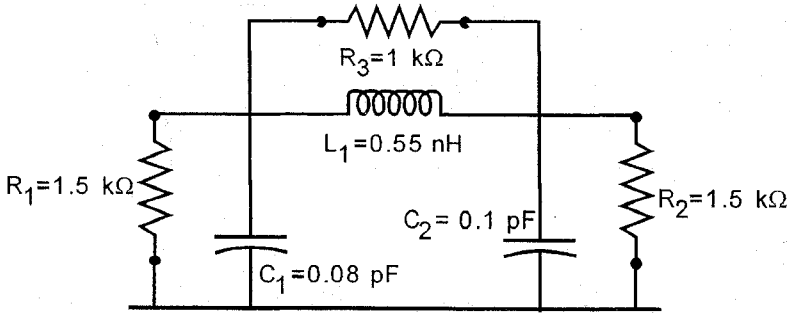


Fig. 9. Lumped element circuit model

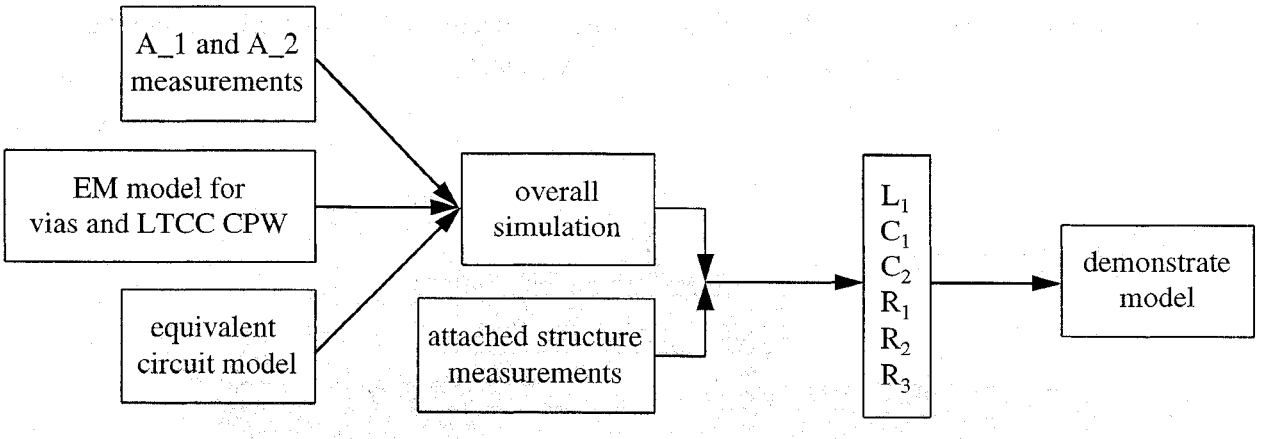


Fig. 10 Deembeding technique

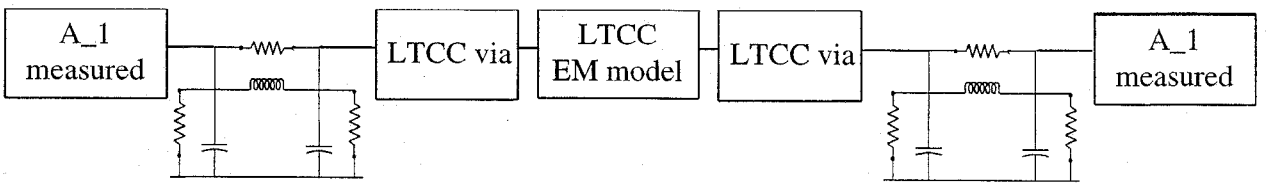


Fig. 11 Block diagram

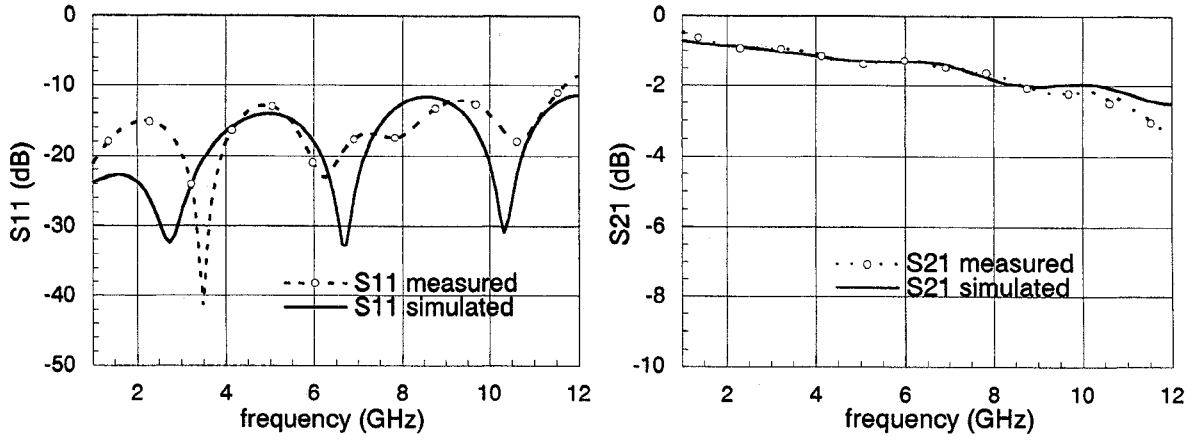


Fig.12. Optimization result

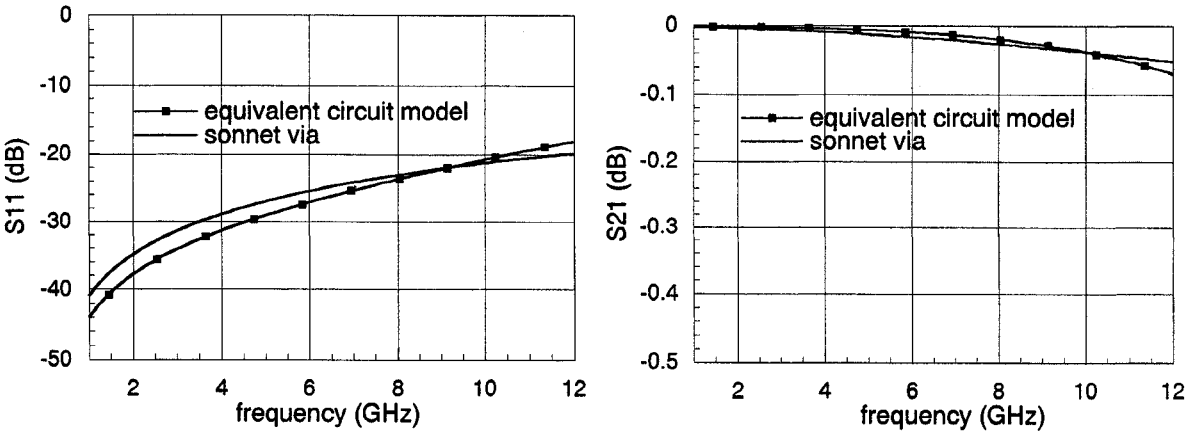


Fig. 13. Demonstration of the equivalent circuit

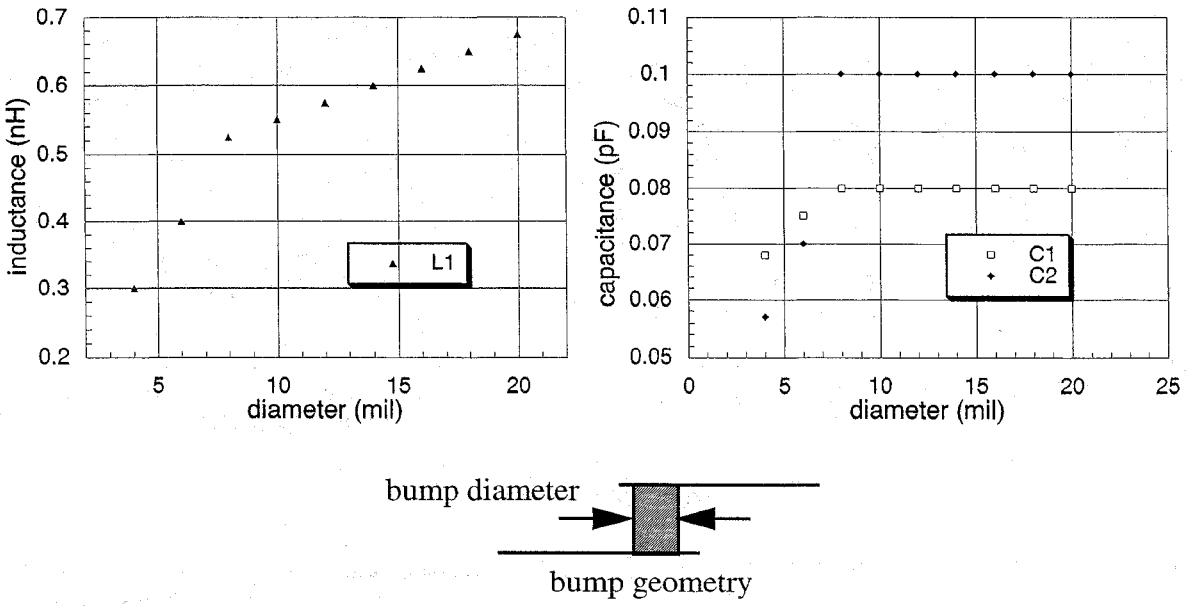


Fig. 14. Variation of lumped elements with the horizontal diameter of the bump