Accurate, High Speed Modeling of Integrated Passive Devices in Multichip Modules

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Abstract

A new method for the predictive modeling of passive devices with interactions based upon measurement and primitive cell charactereization is presented. Building block RLC equivalents can be utilized for arbitrary geometry device modeling in high speed circuit simulators.

Introduction

Accurate, high speed predictive modeling of integrated passive devices with their associated parasitics are essential towards achieving the goal of module characterization [1]. Test structures of various geometry passive devices are designed and fabricated on various substrates such as silicon, FR4, teflon and alumina-like materials, and their resistance, inductance and capacitance measured using high speed measurement techniques up to a desired frequency and correlated to produce appropriate passives models. Models are extracted for all fundamental geometrical building blocks of Manhattan geometry based components. There are a total of five fundamental geometrical shapes, but of varying dimensions, for which models must be derived. This process can be repeated for different types of materials and geometries, thus enabling us to completely characterize the canonical forms for a variety of materials. Over time, a large amount of measurement data will be compiled, and a database of responses for different geometry primitive forms as a function of frequency will be built up. The data will also include statistical variation data due to different measurement results made from similar devices fabricated on different process runs. This data will then be utilized in constructing a model for any arbitrary geometry structure by substituting the correct responses for the corresponding primitives that form that structure.

Test Structures

Test structures of various geometries are designed for the different types of passive device that are desired to be built. The objective behind designing and fabricating test structures is to be able to characterize the equivalent circuit RLC model of each of the fundamental building blocks of the drawing scheme used in designing those structures. For a drawing scheme in which only straight lines and right angled bends are allowed (Manhattan geometry), the fundamental building blocks reduce down to 5 basic shapes of varying width and length. These building blocks are determined with respect to their surrounding material and have been outlined in Figure 1. The primitives shown are of the first order; higher order primitives can be obtained by expanding the number of squares of surrounding material, thereby including coupling effects. It is important to note that a square can represent empty space, or an entirely different material, thereby allowing the modeling scheme to take into account coupling between dielectric layers in a multi-layer structure, or compute interactions between entirely different structures fabricated on the same layer. This is becoming an increasingly difficult and important issue faced by engineers today, brought on by the push to higher levels of integration in substrates and multichip modules.

The test structure sets are designed in a manner such that the contribution of each of the fundamental building blocks used to build those structures can be deembedded. The number of different shaped structures that are required is determined by the level of accuracy and the amount of flexibility that is to be allowed in designing the passive structures. For instance, in

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resistor designs, it is not uncommon to force the width of a resistor to be one of a few set values, and then vary the lengths in order to achieve different resistances. In this case, far fewer test structures would have to be fabricated than if arbitrary widths were allowed. In addition to designing a deterministic test structure set, a few additional ones are drawn to test the validity of the extracted models.

Measurements on the test structures are performed using a network analyzer, for frequencies up to 10Ghz. The reason for the 10Ghz limit is that the quasi-TEM assumption that is made for microstrip lines does not hold above far above this frequency [2]. RLC model extractions are performed using standard formulas [3] followed by an optimization technique such as steepest descent. The computational expense of optimization at this stage is acceptable since it only has to be done once in order to extract accurate models of the fundamental building blocks. The models are then stored in a database, and can be used by designers by simple table look-up techniques. An advantage of the measurement based method is that the test structures can be fabricated on different runs of the same process, and the extraction process repeated. The variations in the extracted models are stored, and ultimately a statistical database of the RLC parameters is created, thereby allowing yield analysis of the structures being designed.

Circuit Construction

Once the model database has been built up, equivalent circuits of arbitrary geometry structures can be constructed. Depending on required accuracy, high order coupling effects can be taken into account, yielding highly interconnected complex circuits. Assuming models are extracted on a per square basis, with each square being approximately 1/10th the wavelength of the highest frequency of interest or smaller, very large networks can result for even moderately large structures [4]. Small signal analysis of these systems can proceed very quickly in a SPICE compatible simulator; several orders of magnitude faster than an equivalent simulation performed in a full wave solver.

In time domain simulations, the large numbers of poles which result from complex RLC networks can cause extremely slow time stepping in a transient solver in a SPICE compatible simulator, and result in long simulation times. In order to make time domain simulations practical, the circuits must be simplified in some way. In order to reduce the complexity of the network, a circuit compression algorithm is used.

The compression procedure that is used is based upon the familiar star-mesh node elimination algorithm. The method is exact for a specified frequency. In the case of simplification of a RLC network, the L and C elements introduce frequency dependent errors, with the errors increasing with the number of compression steps. However, these errors are usually at a very high frequency, far above the maximum frequency of interest. This fact allows us to compress the circuit in a supervisory manner, based upon user specified tolerances at some maximum frequency. With each compression step, 50% of the nodes in the circuit are eliminated, thus yielding much simpler circuits and shorter simulation times.

Example Resistor Modeling

An example of modeling a resistor structure is shown. The structure being modeled is a 4 segment winding resistor. In this particular example, models for two primitive forms were computed; a corner and a coupling model for material with connectivity on two sides. The S parameter data sets for various test structures were computed in a full wave solver. Models were optimally extracted, and an equivalent circuit representing the resistor was constructed. The S parameter responses between the constructed circuit and the resistor simulated in the full wave solver were compared, with very good agreement. The time savings of the circuit method over the full wave method is about a factor of 30.

Conclusions

A high speed, accurate modeling procedure for interconnect and integrated passives has been presented. The method is based upon test structures and measurements which yield the added advantages of modeling process fluctuations and imperfections, as well as obtaining statistical models. Modeling of primitives allows the user to perform predictive modeling of arbitrary geometry devices in a multi layer, multi structure environment. The algorithm

has been shown to perform well, and at a far greater speed than full wave solvers that have been traditionally used for this application.

References

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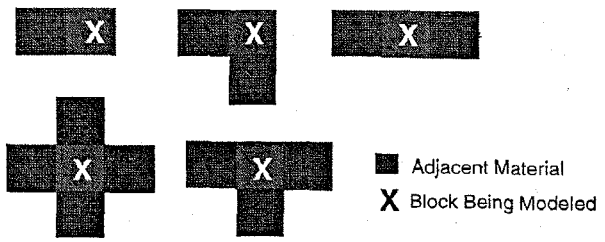

Figure 1 Fundamental primitives for Manhattan drawing scheme

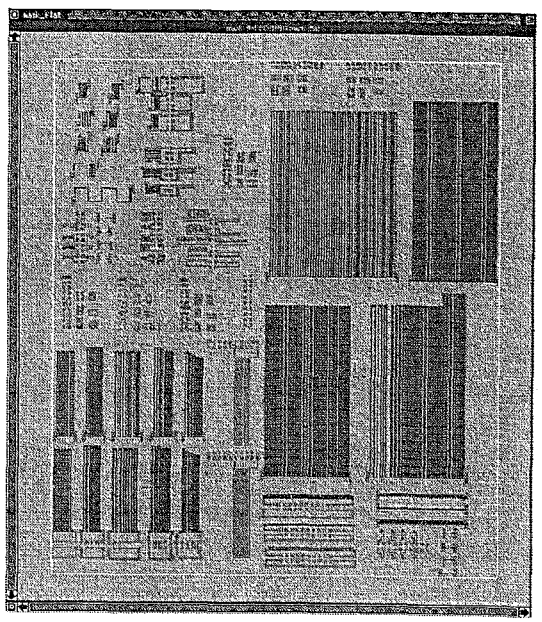

Figure 2 Resistor test structure mask set currently in fabrication at Boeing

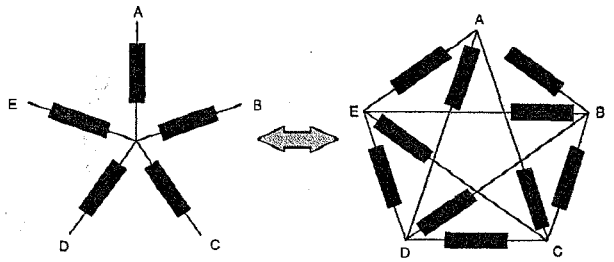

Figure 3 Simplified representation of node elimination network compression algorithm

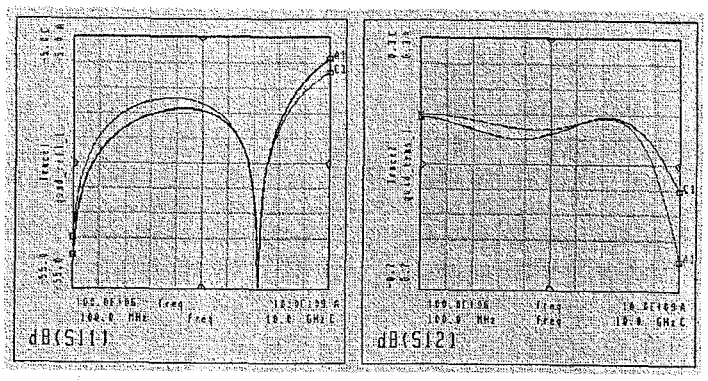

Figure 4 Modeled vs. actual results for 'snaky' resistor structure

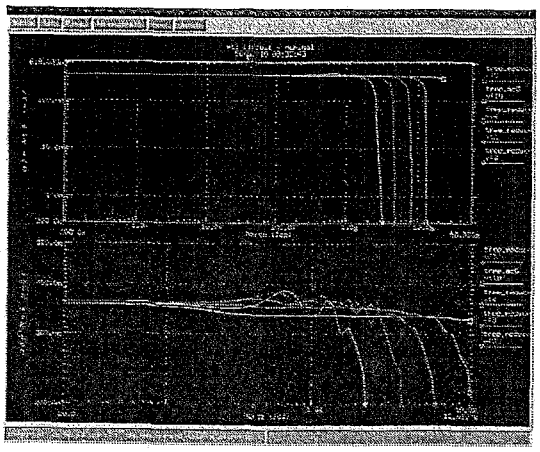

Figure 5 Circuit bandwidth as function of compression step for 400 segment RLC linezzz