## 11:30am - 11:45am WA8

## CMOS Optical Receiver with Integrated InGaAs Thin-Film Inverted MSM Detector Operating up to 250 Mbps

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Standard digital CMOS receivers are desirable for their low-cost and low-power dissipation. In addition, tele-communication applications require long-wavelength (1.3  $\mu$ m /1.55  $\mu$ m) optoelectronic devices, which is possible only with compound materials. Because of material mismatch, implementing a monolithic optical receiver requires exotic process technologies [1] or hybrid integration. Digital CMOS amplifiers with external photodetectors have been reported [2,3]. We have previously demonstrated an optical receiver in which GaAs photodetectors are integrated onto standard digital CMOS amplifiers [4-7] by using a thin-film epilayer device separation and bonding technology [6]. We now report that an amplifier has been fabricated in a 0.6  $\mu$ m digital CMOS foundry, and integrated with an InGaAs inverted Metal-Semiconductor-Metal (I-MSM) photodetector sensitive to 1.3  $\mu$ m/1.5  $\mu$ m light, and characterized up to 250 Mbps.

Fig. 1 shows a single-stage amplifier circuit. The overall amplifier consists of 5 identical stages and is fabricated through a 0.6  $\mu$ m standard digital CMOS process through MOSIS foundry. Each stage has a current gain of 3. The total transimpedance gain is about 12 K $\Omega$  with a 50  $\Omega$  load. To get a wide bandwidth, a multi-stage, low-gain-per-stage configuration is employed. Detailed operation of circuit in Fig. 1 has been reported [5,6]. To achieve stability, an open-loop approach over feedback-type is selected since an open-loop usually provides stability. Another important feature is the current-mode design. It gives wide-bandwidth capability due to low impedance nodes on the signal path. In addition, a diode-connected transistor at the front of an optical receiver replaces a bias resistor and minimizes parasitics.

A metal-semiconductor-metal (MSM) photodetector was selected since low capacitance per unit area is of vital importance in the design of high speed, low power and alignment tolerant optical receivers. The I-MSM detector, with the electrodes defined on the bottom of the device, overcomes the low responsivity problem of conventional MSM detectors with fingers on the top by eliminating the shadowing effect of the electrodes. The I-MSMs demonstrated up to 0.7 A/W responsivity and the leakage current is less than 10 nA at 10 V bias [7]. The bandwidth is up to 6 GHz. Because the I-MSM photodetector is fabricated separately, it is not compromized by CMOS process constraints. The detector structure has 3  $\mu$ m metal finger width with 3  $\mu$ m spacing between fingers. The detector size is 50  $\mu$ m x 50  $\mu$ m, resulting in 70 fF of capacitance. The detector is integrated onto the CMOS amplifier by using a thin-film epilayer device separation and bonding technology [6].

Fig. 2 shows a microphotograph of the completed receiver front-end after integration of the I-MSM photodetector. Two small pads at left side of the figure have overglass cuts for integration of the thin film detector in post processing.

The eye diagrams and pulse waveform at 250 Mbps has been measured for  $2^7$  -1 NRZ pseudorandom bit stream (PRBS) and are shown in Fig. 3. +/- 2.5 V power supplies are used for the amplifier. Total power dissipation is less than 20 mW. However, more than half of the power consumption is used for the offset control. Therefore, the 5-stage amplifier itself dissipates less than 10 mW and its size is about 150  $\mu$ m x 50  $\mu$ m. 50  $\Omega$  output impedance is used to measure the data in Fig. 3.

In conclusion, a quasi-monolithic digital CMOS amplifier integrated with 1.3  $\mu m$  wavelength, InGaAs I-MSM is reported. The power dissipation is less than 20 mW. The sensitivity for  $10^{-10}$  BER measured at  $2^{7}$ -1, 155 Mbps PRBS is about 8  $\mu A$ . To our knowledge, we have demonstrated a quasi-monolithic digital CMOS amplifier with 1.3  $\mu m$  photodetector for the first time. This integration shows the possibility to make low-cost, low-power, and small-size digital CMOS amplifiers for tele-communication applications such as SONET and FDDI.

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## <u>References</u>

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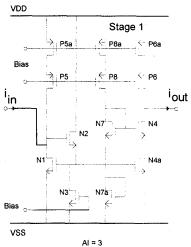


Figure 1. A single-stage circuit diagram of the standard digital CMOS amplifier.

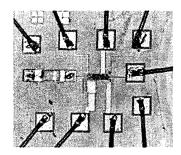


Figure 2. The microphotograph of the integrated amplifier.

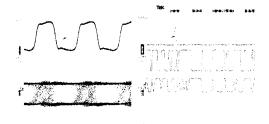


Figure 3. The eye diagram and pulse waveform of the integrated optical receiver at 250 Mbps.