# DESIGN OF HIGH-ORDER SINGLE-BIT SIGMA-DELTA MODULATORS

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## ABSTRACT

This paper describes a design procedure for high-order (e.g. $2 \geq n \leq 10$) single-bit sigma-delta modulators. A crucial design tool for these high-order loops is a numerical simulator which enables optimum scaling, stability testing under various operating conditions, determination of the maximum applicable input swing and the computation of the dynamic range and the signal-to-noise ratio. Numerical examples for various loop orders are given and silicon prototype circuits are presented.

## 1. INTRODUCTION

In order to increase the resolution and/or reduce the oversampling rate of (low-order) sigma-delta converters, there exist three basic approaches. In the first case, the simple single-bit quantizer at the loop output is replaced by a multi-bit quantizer [1]. This not only reduces the quantization noise and thus increases the dynamic range but also decorrelates the quantization noise spectrum from the input signal. Consequently, the system is less likely to fall into a cyclic behavior which can give rise to spurious tones in the passband of the converter. The major drawback of this solution is the extremely high linearity requirement for the digital-to-analog converter in the feedback path of the modulator, rendering a monolithic implementation very difficult. In the second approach, the single modulator loop is replaced by a multi-loop configuration whereby the additional loop(s) create an estimate of the quantization noise of the previous loop(s). This noise estimate is subsequently subtracted from the previous loop output(s) [2]. Consequently, the output of a multi-loop system is a multi-bit stream. Analogous to the first approach, the multi-loop solution whitens the quantization noise and thus prevents the occurrence of spurious tones. However, the reduction of the quantization noise by signal subtraction requires well matched capacitor ratios in the analog modulator loops and a good control over the op-amp gains. In the third approach, finally, the order of the loop filter is increased such that the inherent discrimination between signal and quantization noise is significantly enhanced. Similar to the previous two approaches, increasing the loop order tends to decorrelate the quantization noise from the input signal. In contrast to the multi-bit solution, the single-bit high-order approach preserves the original insensitivity of the modulator with regard to minor variations of its constituent analog components. The major obstacle in this case is the difficulty of designing these high-order loops such that stability can be guaranteed under the various operating conditions.

## 2. HIGH-ORDER SINGLE-BIT LOOPS

By replacing the nonlinear quantizer of a single-bit sigma-delta modulator by an additive white noise source of variance $\sigma_q$ and assuming a loop filter with ideal noise shaping characteristics, the rms in-band noise $\sigma_o$ at the output of such an $n^{th}$ order system can be written as

$$\sigma_o = \sigma_q \frac{\pi^n}{\sqrt{2n+1}} OSR^{-(n+\frac{1}{2})} \tag{1}$$

The variable OSR denotes the oversampling rate $\frac{f_s}{2B}$, where $f_s$ and B represent the modulator sampling frequency and the system bandwidth, respectively. If we denote the voltage step of the single-bit quantizer by $V_{ref}$, the variance of the quantization noise can be expressed as

$$\sigma_q = \frac{1}{\sqrt{12}} V_{ref} \tag{2}$$

According to equation (1), increasing the loop order from n to n+1 reduces the output quantization noise by a factor

$$G_{n,n+1} = \sqrt{\frac{2n+3}{2n+1}} \frac{OSR}{\pi} \tag{3}$$

The dynamic range inprovement, as predicted by the above equation, is very optimistic and increasingly overstates the noise reduction factor as n increases. The two major reasons for the inapplicability of the above equation to higher-order loops are the assumed idealized loop filter characteristics and the oversimplified model for the nonlinear quantizer at the modulator output. It is obvious that the filter poles will affect the modulator performance, yet their influence is not reflected in equation (3). A less intuitive fact is the correlation between quantization noise and applied input signal. This correlation is most pronounced for large input signals and thus cannot be ignored in an accurate analysis of the loop behavior.

Since there exists no exact mathematical treatment for high-order single-bit sigma-delta modulators, we have referred to a very pragmatic solution by having written a simulator (DelSi) which accurately mimics the modulator in the (discrete) time domain. In this way, one can readily incorporate the nonlinear quantizer at the loop output or any signal saturation effect encountered in the amplifiers of the loop filter. Furthermore, after the system poles have been placed, dynamic range optimization and stability testing can be performed under realistic conditions. For example, the scaling factors for the loop filter are not computed by completely ignoring the

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quantizer but rather are deduced via statistical means by observing the actual voltage excursions at the output of each amplifier for a variety of different operating conditions (i.e. the frequency and the amplitude of the input signal are varied such that the entire range of interest is covered). Finally, the modulator output spectrum is computed by applying an FFT to the single-bit output stream. To minimize windowing effects, a large number of output samples is computed. We typically use $2^{15} = 32,768$ points which are subsequently shaped by a Hanning window.

The design procedure begins with the selection of an appropriate loop filter topology. The DelSi program presumes an inverse follow the leader feedback (IFLF) topology. Even though this structure is not considered a minimum sensitivity topology such as a ladder configuration, its many feedbacks, all originating from the comparator output, tend to randomize the quantization noise. The resulting whitening of the noise spectrum helps to prevent spurious harmonics in the passband of the converter.

Figure 1 shows an example of a $3^{rd}$ order modulator with an IFLF loop filter topology.

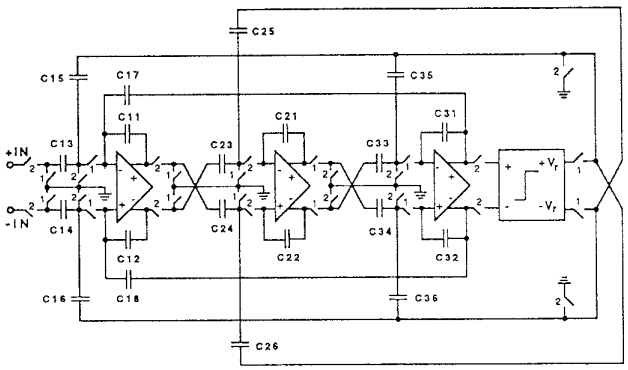


Figure 1: Schematic of $3^{rd}$ order sigma-delta modulator loop

Note that the switching scheme of this fully-differential switched-capacitor network has been arranged such that each op-amp possesses an equal settling time of half a clock period. Consequently, no direct signal feed-throughs do occur. This significantly relaxes the conditions for the amplifier settling behavior. Furthermore, the depicted circuit has been supplemented by an additional feedback path realized by $C_{17}$ (or $C_{18}$ for its symmetrical counterpart) to enable the implementation of a finite stopband zero in the noise transfer function. This zero serves to further suppress the in-band quantization noise. Higher order loops can utilize multiple zeros in the noise transfer function and thus can yield even better noise shaping characteristics. The major drawback in conjunction with these additional zeros is the inherently high coefficient spread since these singularities are located in the vicinity of the origin and consequently the ratio of zero frequency to sampling rate becomes extremely small.

The next decision, the determination of the loop order, largely depends on the chosen oversampling rate OSR and the system resolution or dynamic range (DR). An initial estimation of the required modulator loop filter order can be derived from equation (1).

The actual placing of the filter poles is an iterative process. This procedure is initiated with an approximate stable solution which is successively improved upon by maximizing the corresponding signal-to-noise ratio (SNR) by means of multiple DelSi runs. Some useful guidlines as to how the initial stability can be estimated can be found in [3]. Note that an unstable solution is readily detected by the simulator since it causes the amplifiers of the loop filter to saturate at a user specified level. This in turn leads to a collapse of the SNR. Apart from finding an optimum pole (and zero) placing, this recursive optimization procedure also reveals the maximum amplitude of the input signal under which stable operation can be guaranteed.

Having experimented with various loop filter pole configurations, we found that the polynomial type, i.e. Butterworth, Chebyshev, etc. is a far less crucial factor as far as quantization noise suppression is concerned than the ratio of loop filter cutoff frequency to sampling rate. To maximize the passband noise suppression, one would like to keep this ratio as large as possible, on the other hand, too high a filter cutoff frequency increases the high frequency gain in the noise transfer function which in turn enhances the quantization noise and can even render the system unstable. With the help of a numerical simulator, a designer can readily find an acceptable compromize between these contradictory objectives.

## 3. DESIGN EXAMPLES

To demonstrate the advantage of utilizing high-order modulator loops, we will consider four design examples involving four circuits of progressively higher order. The first two examples are a $2^{nd}$ and $3^{rd}$ order system, both of which are to be optimized for an OSR of 64. The other two examples deal with a $5^{th}$ and $7^{th}$ order loop, respectively. These higher order circuits are aimed at an OSR of 32.

We have selected Butterworth poles for all loop filters and, apart from the $2^{nd}$ order example, added finite zeros in the noise transfer function to further suppress the in-band quantization noise. The four output spectra, derived from optimized modulator loops, are displayed in figure 2. Note that all spectra have been simulated for the case of a single sinusoidal input signal at 20kHz ($2^{nd}$ and $3^{rd}$ order) or 40kHz ($5^{th}$ and ($7^{th}$ order), respectively, while the sampling rate has been maintained at 10.24MHz. The first two examples thus exhibit a system bandwidth of 80kHz while the two highest order modulators pass frequencies up to 160kHz.

For both OSR values, the presented plots clearly demonstrate the superiority of the higher order loops.

Figure 3 shows the SNR of each modulator as a function of the input signal power. Note that the input signal swing has been normalized to the reference voltage $V_{ref}$. Consequently, an sinusoidal input with a swing equal to $V_{ref}$ possesses a relative power of -3dB. The four plots reveal a minor shift of the SNR peak towards smaller input signal amplitudes as the order of the loop filter is increased. If the input amplitude exceeds its optimum value $V_{in_{opt}}$, the quantization noise rapidly increases and eventually all but the $2^{nd}$ order system become unstable. The final instability is reflected in the displayed plots by the abrupt collapse of the SNR at the right end of the horizontal scale.

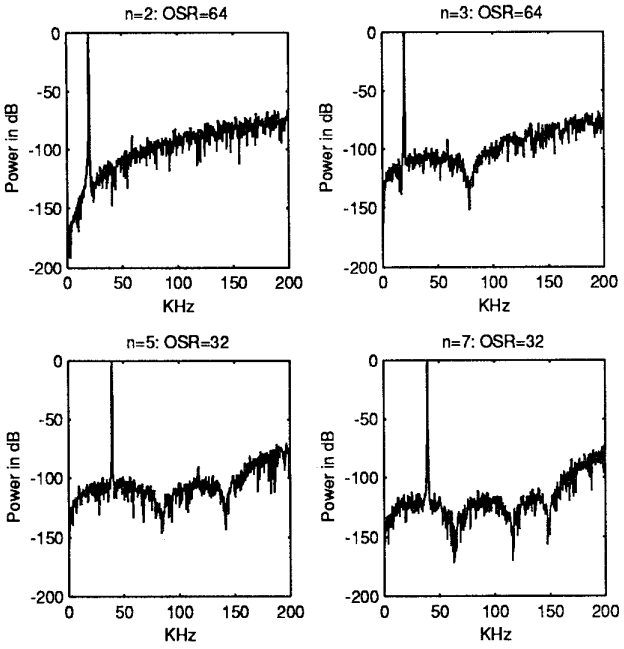


Figure 2: Output power spectra of the four optimized modulator loops

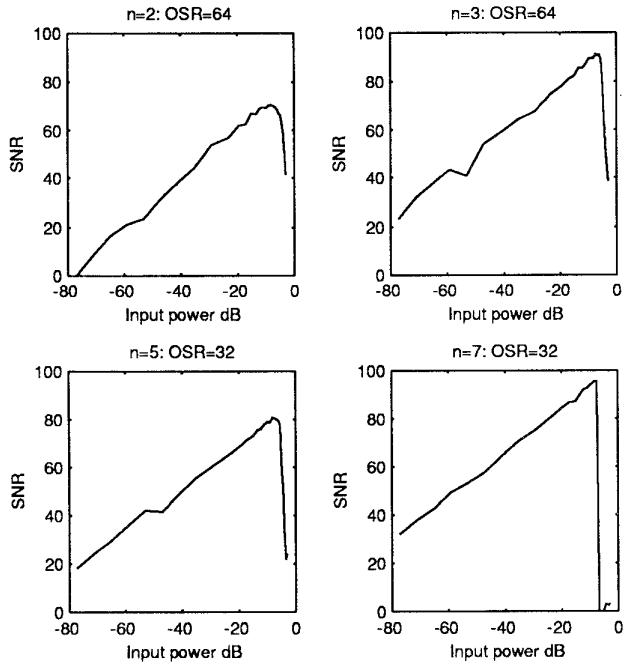


Figure 3: SNR versus input amplitude (DelSi simulation)

The most important performance parameters of the four simulated modulator loops are summarized in table 1.

Note that the DR parameter listed in table 1 has been defined as the difference between the input power yielding the maximum SNR and the minimum signal power detectable in the presence of the quantization noise. Since a large input swing enhances the quantization noise by a noticeable margin, the DR value exceeds the peak of the SNR. Therefore, the noise suppression of the $7^{th}$ order modulator is sufficient to realize a converter with a digitally equivalent resolution of 16-bit.

| Feature | $2^{nd}$ order | $3^{rd}$ order | $5^{th}$ order | $7^{th}$ order |
|---|---|---|---|---|
| OSR | 64 | 64 | 32 | 32 |
| $SNR_{max}$ | 70.6dB | 90.1dB | 84.3dB | 95.6dB |
| DR | 72.5dB | 95.5dB | 88.1dB | 101.0dB |
| $\hat{V}_{in_{opt}}$ | $.70V_{ref}$ | $.60V_{ref}$ | $.60V_{ref}$ | $.55V_{ref}$ |

Table 1: Performance of the four sigma-delta modulator loops

## 4. LAYOUT CONSIDERATIONS

In order to verify the validity of the presented DelSi simulations, we have implemented the three highest order examples by a $2\mu m$ double-poly CMOS process. The circuits have been aimed at a nominal power supply of $V_{DD} = -V_{SS} = 2.5V$. The three modulators have been layed out on a single chip in form of fully-differential circuits.

As a representative example, figure 4 depicts the complete layout of the fully-differential $3^{rd}$ order modulator.

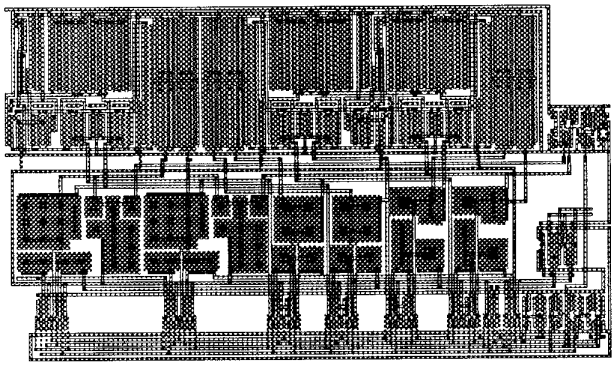

Figure 4: Layout of $3^{rd}$ order modulator loop (size: $512\mu m \; x \; 900\mu m$)

The floor plan of this circuit has been arranged such that analog and digital circuit sections are separated by a maximum physical distance, i.e. the amplifiers and the single comparator are placed on top followed by the filter capacitors while switches, clock generator and clock bus are located at the very bottom. Furthermore, the capacitors are shielded from the n-type substrate by an additional grounded p-well.

The fully-differential op-amps are based on a folded cascode topology complemented by a resistive continuous-time feedback network. These transconductace amplifiers have been designed to drive a nominal capacitive load of 3pF. According to a CAzM[1] simulation carried out with level 2 MOSFET models, they yield a unity-gain frequency of 40MHz and a slew

[1] CAzM: A Circuit Analyzer with Macromodeling, Microelectronics Center of North Carolina, 1989

rate of approximately $40V/\mu s$. It is thus feasible to sample the modulator circuits by a clock rate as high as 10MHz.

The single quantizer has been implemented by a comparator consisting of a (low-gain) differential input stage followed by a resettable CMOS latch.

By utilizing T-sections to reduce the high capacitor spread characteristic for the realization of the additional feedback loops emulating the finite stopband zeros of the noise transfer function, the maximum C-spread in all three loop filters could be limited to a value of approximately 10. In order to balance the amplifier loads, the integrating capacitors in all three modulators have been adjusted such that the effective load capacitance of each stage have summed up to a value in between 2.5pF and 3.5pF.

At the time of the writing of this paper, the prototype chip is still in fabrication so that no measurements can be reported. However, each circuit layout has been verified by having extracted a netlist from the actual mask geometry. Subsequently, the resulting circuit descriptions have been analyzed by CAzM. An example of such a transistor level simulation is shown in figure 5. The plot shows the response of the $3^{rd}$ order modulator due to a single sinusoidal input at 50KHz with an amplitude of 1V. The quantizer step size $V_{ref}$ has been set to 1.5V

The three traces depicting the intermediate amplifier output signals, i.e. V(Out1), V(Out2) and V(Out3), reveal an increase of the quantization noise as we proceed from the filter input to the output. This behavior is expected since each subsequent stage in the IFLF topology has accumulated one additional signal feedback originating from the quantizer output. Furthermore, the well balanced amplifier output swings underline that the applied scaling procedure has been appropriate.

Last but not least, the CAzM simulation does provide a verification of the system stability under the given operating conditions.

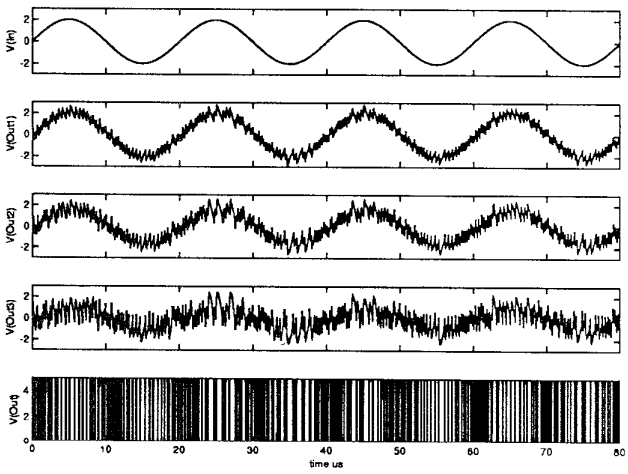


Figure 5: CAzM simulation of $3^{rd}$ order sigma-delta modulator loop

If the transient output response of the modulator, as obtained via a CAzM simulation, is computed over a sufficiently long time interval (e.g. 3.2ms yield 32,768 time samples obtained by a 10.24MHz clock rate), the digital output signal (cf. bottom trace in figure 5) can be subjected to an FFT to extract its frequency content. Unfortunately, such a procedure is not only very computationally intensive, but ultimately it is also limited by the numerical accuracy of the analog simulator and the agreement between the physical process parameters and the applied MOSFET models. In trying to do the above, we have encountered a dynamic range limitation of approximately 100dB in the resulting output spectrum. Consequently, we have not been able to verify the exact passband noise behavior as displayed in figure 2 by means of a DelSi simulation. As a matter of fact, this situation is not too different from a physical performance verification. Apart from the quantization noise, a real circuit comprises a variety of other noise sources such as capacitor switching noise, amplifier thermal and 1/f noise etc. that will obscure the output spectrum.

## 5. CONCLUSIONS

By employing numerical simulation methods, it is possible to predict the behavior of high-order sigma-delta modulators in such a way that operating conditions can be defined which avoid the potential instability. In addition, such a simulator is an indispensable tool for optimizing the pole and zero locations of the modulator noise transfer function and finding the appropriate scaling coefficients under realistic conditions. Finally, it is only via simulation that one can deduce the expected performance of such a complex high-order nonlinear system since the simplified models applied for $1^{st}$ and $2^{nd}$ order systems (cf. equation(1)) prove inappropriate.

## 6. REFERENCES


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