Thin-Film Multimaterial Optoelectronic Integrated Circuits

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***Abstract*—The multimaterial integration of thin-film optoelectronic devices with host substrates ranging from silicon circuits to glass waveguides to polymer micromachines offers to the system designer the freedom to choose the optimal materials for each component to achieve performance and cost objectives. Thin-film compound semiconductor optoelectronic devices are comparable to, and, in some cases, better than, their on-wafer counterparts. Thin-film detectors have been integrated with receiver circuits and movable micromachines, thin-film emitters with drive circuitry, and both have been used to demonstrate three-dimensionally interconnected systems. Vertical electrical integration of detector arrays on top of circuits is examined for massively parallel processing of images. Vertical optical interconnections of stacked silicon circuits (which are transparent to the wavelength of light used) are explored, and are used to develop a massively parallel processing architecture based upon low memory, high throughput, and high input/output.**

***Index Terms*—optoelectronics, interconnect network, thin film devices, epitaxial liftoff**

I. Introduction

ONE ROAD toward a future where the boundary between a system and its package is less distinct is that of multimaterial integration, which strives to introduce greater functionality directly onto a single substrate. For example, the preferred materials for individual components of integrated optoelectronics systems often include silicon for VLSI circuitry and displays, GaAs and InP-based materials for photonic and high-speed electronic devices, and polymers and glass for optical waveguides and gratings. Often, using the optimal material for a particular application can reduce the system cost and/or increase system performance. The fabrication challenge in integrated optoelectronics is to take advantage of the cost and performance advantages of each of these materials in a manufacturable manner. One promising method for integrating semiconductor devices, both electronic and optoelectronic, with arbitrary host substrates is thin-film device integration. Single crystal, thin-film semiconductor devices can be separated from the growth substrate and bonded to host substrates using standard microelectronic processes, a particularly attractive option for multimaterial integrated optoelectronics. The separation of Si, GaAs, and InP-based thin-film epitaxial devices from the growth substrate, called epitaxial lift off (ELO), and the subsequent transfer and bonding of these thin-film devices to relatively smooth host substrates, such as silicon circuits, waveguides, and polymers, has been demonstrated by a number of groups.

Multimaterial integrated systems, both electronic and optoelectronic, enable the system designer to explore issues such as power, speed, interconnect, and heat dissipation from a new perspective. With packaging issues such as interconnectivity and heat dissipation currently limiting electronic processing density and speed, the prospect of optoelectronics serving a useful role in heretofore electronic systems is on the horizon. Optoelectronics has an opportunity not to compete with silicon, but to complement and augment the capabilities of silicon electronics. For example, using post processing to integrate compound semiconductor devices onto a silicon circuit, highly complex electronic functions can be realized in conjunction with optoelectronic functions. Thus, tremendously "smart" integrated optoelectronic devices and arrays can be realized with low cost CMOS circuitry, such as that from the MOSIS foundry. This multimaterial integration not only enables smart OEIC's, it also opens the door to optoelectronics to increase the functionality of silicon circuitry.

The use of thin-film optoelectronic devices can extend the interconnection of silicon circuits into the third dimension through the vertical interconnection of layers of processing. Herein two such three-dimensionally interconnected systems using thin-film devices will be explored. The first, an imaging system, integrates thin-film devices directly on top of planarized silicon neural circuitry to form an imaging array. This massively parallel, three-dimensionally interconnected imager operates in a manner based loosely upon a retina. Microphotographs and test results of this imager will be presented.

The second three-dimensional system stacks standard two-dimensional silicon circuits and provides vertical interconnect between the stacked chips using through-silicon wafer optical signals operating at a wavelength of 1.3 μm (to which silicon is transparent). This type of interconnection also enables efficient heat dissipation (using an optically transparent gaseous or liquid coolant) in that the optical signals are not degraded by the flow, nor do they impede the flow. This heat dissipation advantage for optical interconnect is significant in that heat is a

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key issue for two-dimensional systems, and is the limitation to operation for some three-dimensional schemes. To demonstrate this three-dimensional optical interconnect, InGaAsP-based emitters and detectors operating at a wavelength of 1.3 μm were integrated onto silicon which was subsequently stacked, and through-wafer communication was achieved. These emitters and detectors have now been integrated onto silicon circuits which contain routing and processing circuitry. This type of three-dimensional interconnectivity enables the design of high efficiency, massively parallel systems. Two of the first levels of an optically interconnected image processing system have been fabricated, and will be discussed. A three-dimensional architecture for a system design for a massively parallel, optoelectronically interconnected image processor will also be examined.

II. Thin-Film Device Fabrication and Integration Techniques

Highest quality, defect-free optoelectronic materials are grown lattice matched (or near lattice matched) to growth substrates. These substrates, however, seldom contribute to the function of the epitaxial device, and may be removed without detriment (and sometimes with advantage) to the thin-film epitaxial device. Thin-film material can be separated from a growth substrate using selective or stop etch layers which lie between the growth substrate and the device layers of interest. These thin films, usually on the order of microns thick, can then be bonded to host substrates of arbitrary composition to create multimaterial optoelectronic integrated circuits (OEIC's).

To separate thin-film epitaxial material from the growth substrate, either selective etching of a sacrificial etch layer (epitaxial lift off) or substrate removal with stop etch layers can be used. In 1987, Yablonovitch reported a process for the separation of epitaxial $Al_xGa_{1-x}As$ $(x < 0.4)$ from the lattice matched GaAs substrates upon which they were grown [1]. This ELO uses a sacrificial layer of AlAs between the epilayers of interest and the GaAs growth substrate, as illustrated in Fig. 1(a). For this lateral sacrificial etch process in the GaAs material system, a sacrificial etch layer of $Al_xGa_{1-x}As$ $(x > 0.6)$ must be grown between the thin-film device and the growth substrate. Sacrificial etch layers ranging in thickness from 20 Å [1] to 0.5 μm [2] have been reported. Prior to epitaxial layer separation, the sample surface can be metallized (for electrical contact, and to aid in bonding), optically coated, photolithographically patterned and mesa etched, or processed in whatever manner is appropriate for the final device and integrated system. The first step in the lateral etch ELO process is to apply an Apiezon W handling layer to the epitaxial sample, easily accomplished by melting the wax directly onto the sample, and cleaning the edges so that they are exposed to the etch solution. When the GaAs-based sample is immersed in a 10% HF etch, the sacrificial $Al_xGa_{1-x}As$ $(x > 0.6)$ epilayer is selectively laterally etched, thereby separating the epilayers of interest from the GaAs growth substrate. High quality ELO thin films as large as 2 cm × 4 cm [3] and as thin as 200 Å [3] to as thick as 5.0 μm [4] have been reported. This ELO process

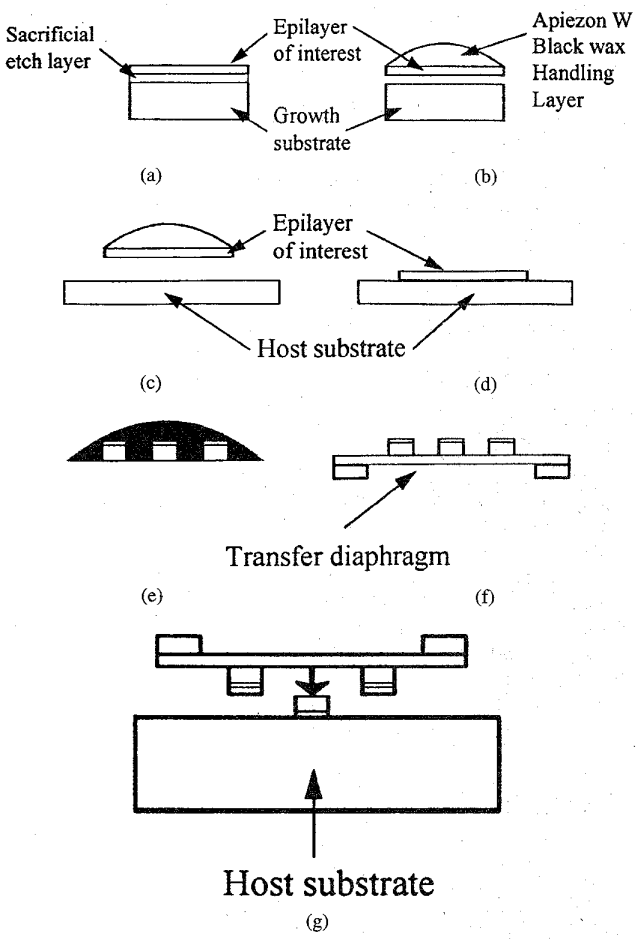


Fig. 1. Diagram of the ELO process. (a) As-grown sample. (b) After application of Apiezon W handling layer and sacrificial etch. (c) Bonding to host substrate. (d) Thin film bonded to host substrate. (e) Mesa-etched thin-film material embedded in Apiezon W handling layer after ELO. (f) Thin-film devices bonded to transparent transfer diaphragm. (g) Bonding from transfer diaphragm to host substrate.

is limited to the separation of $Al_xGa_{1-x}As$ $(x < 0.4)$ epilayers from the substrate since all layers with $x > 0.6$ are etched by the HF solution. One solution to this problem is to mesa etch the outer edges of the epitaxial layers down to, but not through, the AlAs sacrificial etch layer, as illustrated in Fig. 1(e), where the thin-film devices are separated from the host substrate, embedded in the Apiezon W. The Apiezon W then protects these high Al composition layers from the HF etch while still enabling the separation of the epilayers from the growth substrate. In GaAs, the mesa etch $H_2SO_4 : H_2O_2 : H_2O$ $(1:8:160)$ is used as a fast etch to quickly remove the material between the devices followed by a $NH_4OH : H_2O_2$ $(1:100)$ selective etch which stops at the AlAs epilayer.

An alternative to ELO is total substrate removal: the substrate can be removed from the thin-film devices with selective etches and stop etch layers. This process can use Apiezon W to protect the devices, or the devices can be bonded to an intermediate or final host substrate with subsequent substrate removal. Goossen bonded modulators to a metallized host silicon circuit, and removed the GaAs substrate with NH_4OH :

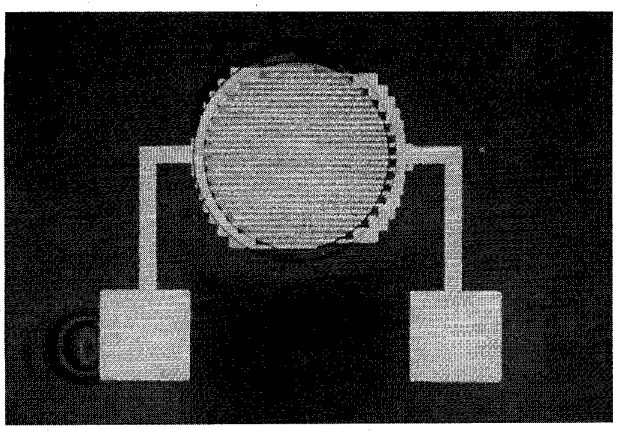


Fig. 2. Photomicrograph of GaAs MSM thin-film photodetector bonded to a Si_3N_4-coated silicon substrate.

H_2O_2 (1 : 100) [5], which selectively etches the GaAs, but etches the AlGaAs stop etch layer minimally. Worchesky [6] bonded an array of GaAs-based modulators to a silicon circuit and subsequently removed the substrate. Fathollahnefad [7] bonded vertical cavity surface emitting lasers (VCSEL's) to a glass slide using Apeizon W, thinned the substrate to 100-μm thick using mechanical thinning, and then used NH_4OH : H_2O_2 with a pH of 8.5 to stop at an AlAs stop etch layer. To maintain a high quality semiconductor Bragg mirror, a succession of selective etches (HF and NH_4OH : H_2O_2) coupled with AlGaAs/GaAs alternating stop etch layers can be used, to thin and smooth the sample [7].

After the epitaxial thin film has been separated from the growth substrate, it can be bonded onto a smooth host substrate, as illustrated in Fig. 1(d), and the Apiezon W handling layer removed using trichloroethane. The bonding to the host substrate occurs through contact (van der Waals) bonding. Figure 2 is a photomicrograph of a GaAs metal–semiconductor–metal (MSM) thin-film photodetector which has been separated from the growth substrate using epitaxial lift off, and then Van Der Waals bonded to a host silicon nitride-coated silicon substrate [8]. This photodetector bonded to silicon operates at frequencies up to 1 GHz. Alternatively, the thin films can be affixed to the host substrate using adhesives such as cement, or bonded using an interface metal such as palladium.

A number of modifications to this basic process have been developed. These include a transfer diaphragm process, which uses a transparent Mylar diaphragm as an intermediate transfer medium, as shown in Fig. 1(f) and (g) [9]. After bonding the devices to the transfer diaphragm and the Apiezon W is removed, the diaphragm (and devices) are inverted and the array of devices can be aligned and selectively bonded to the host substrate individually or as an array of devices. This transfer diaphragm technique utilizes the thin-film material in a cost effective manner since many host substrates can be serviced with one thin-film array of devices, and, since the devices are inverted, both sides of the thin-film devices can be processed while under substrate (either growth or host) support. This is particularly useful for bonding, since the side of the device that was processed (e.g., metallized) before separation is now bonded to the host substrate. Thus, the metal contact on the thin-film device and a metallized host substrate will form a stable electrical and mechanical bond when the metal/metal contact is rapid thermal annealed after contact bonding.

Total substrate removal is the primary separation process used for InP-based thin-film device formation. A stop etch layer is grown between the epilayers of interest and the InP substrate, the devices are defined through mesa etching, an Apiezon handling layer is applied to the epilayers, and the substrate is selectively etched away to the stop etch layer. Either InGaAs [10] or InGaAsP [11] can be used as stop etch layers for InP substrate removal. Substrate removal is accomplished using HCl or a HCl : H_3PO_4 (3 : 1) solution. After substrate removal, the stop etch layer can also be removed using a second selective etch. For example, to fabricate an InP thin film, an InP (substrate)/InGaAsP (stop etch layer)/InP sample was used. After mesa etching to the InGaAsP layer, the sample was immersed in HCl : H_3PO_4 (3 : 1) to remove the InP substrate. The sample was then immersed in HF : H_2O_2 : H_2O (1 : 1 : 10) to selectively remove the InGaAsP layer from the InP epilayer, leaving the InP thin film attached to the Apiezon W.

III. Performance of Thin-Film Devices

Numerous materials and device characterizations have been completed to establish that thin-film devices perform comparably or, in some cases, better than their on-wafer counterparts. Standard materials characterization techniques, including photoluminescence, Hall measurements, and minority carrier lifetime have been applied to epitaxial lift off thin-film materials. Photoluminescence and Hall measurements have been performed on AlGaAs/InGaAs single strained quantum well ELO thin-film structures on glass [12], photoluminescence measurements on InP thin films on glass [11], and minority carrier lifetime measurements on AlGaAs/GaAs/AlGaAs double heterostructure thin films on glass [3]. All of these experiments indicated that the quality of the thin-film material is not degraded by the process used to separate the epitaxial layers from the host substrate.

The formation of high quality single crystal thin semiconductor films using ELO has enabled some optical material characterization which had been hampered by the growth substrate. Photoabsorption measurements of InP at high photon energies necessitate the use of thin films without the InP substrate since the absorption coefficients of the InP at these wavelengths are high. To measure the high energy absorption coefficients in InP, thin-film InP samples were fabricated and transmission measurements were performed [11]. These measurements indicated that the InP absorption coefficients and bandtails vary with doping in the same manner as GaAs. Substrate removal has also aided some nonlinear optical measurements. Nonlinear refraction measurements close to the band-edge, with high absorption coefficients, and with large electric field applied, can be measured using sufficiently thin samples. Changes in index of refraction and

absorption coefficient as a function of electric field near the semiconductor bandedge (the Franz–Keldysh effect, or electroabsorption and electrorefraction) are difficult to measure due to absorbing substrates in the GaAs materials system (limiting modulators to reflective, rather than transmissive operation), high absorption coefficients near the band-edge of semiconductors, and the difficulty in applying high voltages to thick devices limit measurements of and the utility of these effects. Thin-film structures have been used to characterize electrorefraction in bulk GaAs. These thin films naturally form a Fabry–Perot resonant structure that can be enhanced with deposited mirrors. In fact, these thin-film Fabry–Perot resonant structures are so thin that the coherence length of light from a monochromator is sufficient to probe the resonances of these thin films. Thin-film ELO Fabry–Perot measurements were first performed on GaAs based ELO multiple quantum well modulators bonded to glass [13]. The transmission measurements on these devices show a shift in the exciton peak toward longer wavelengths with increasing electric fields, which is consistent with measurements performed on MQW's on bulk substrates (in reflection mode) to characterize the quantum confined Stark effect. The resonant peaks of the transmission characteristic of these thin-film Fabry–Perot structures shift as a function of change in index of refraction in the sample and can be used to quantitatively measure electrorefraction. To measure electrorefraction near the bandedge in GaAs, a thin-film double heterostructure AlGaAs/GaAs/AlGaAs p-i-n epitaxial structure was bonded to glass. Using a monochromator and a pulsed (to minimize heating) voltage source to apply the electric field, resonance shifts as a function of applied voltage were measured, resulting in the closest to the bandgap and highest electric field measurements of Franz–Keldysh electrorefraction in GaAs to date [14].

In addition to material studies, device experiments have been used to test the quality of thin-film devices. The first report of GaAs light emitting diodes bonded to silicon exhibited output powers as a function of input currents which were slightly larger than that of on-wafer devices [15]. Likewise, double heterostructure laser light output–current (L–I) characteristics for ELO and on-wafer lasers have been compared, with no measurable change in either the L–I curve or in the laser threshold current (about 1000 A/cm^2) after ELO processing [16]. These performance characteristics were substantially better than GaAs-based light emitting diodes which were grown directly onto silicon substrates, indicating that the material quality of the ELO thin-film devices deposited onto silicon is better than that of the GaAs material grown directly onto silicon. Passivated metal–semiconductor–metal (MSM) detectors have demonstrated comparable dark currents and bandwidths to on-wafer MSM detectors [17].

Access to the back surface of an epitaxial device removes some of the limitations imposed on device designers by the presence of the substrate, and can result in low cost, higher performance devices than on-wafer devices. Resonant cavity devices, including resonant cavity enhanced detectors and emitters, vertical cavity surface emitting lasers with dielectric mirrors, and MSM photodetectors with interdigitated finger contacts on the bottom to eliminate finger shadowing, are examples of thin-film devices that can exhibit enhanced performance because the substrate has been removed. In addition, resonant cavity devices can be fabricated in a more manufacturing tolerant manner using vacuum deposited multilayer dielectric and/or metallic mirrors, which have a large high reflectivity bandwidth and are less costly to fabricate than semiconductor Bragg reflectors.

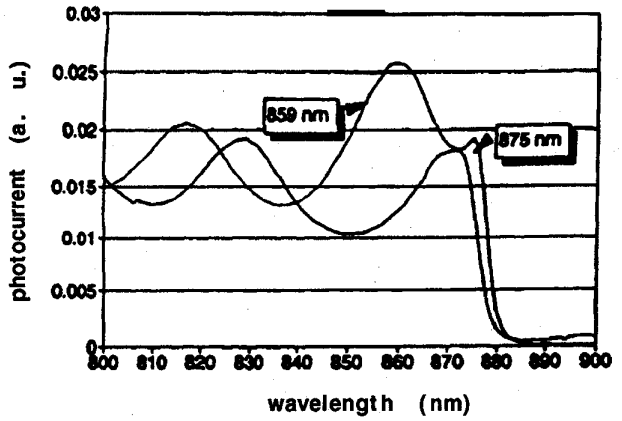
Resonant cavity enhanced detectors have been fabricated using double heterostructure p-i-n detector structures, high reflectivity coatings, and cavity etching to tune the Fabry–Perot cavity resonance [18]–[20]. The thin-film detector had metallic mirrors vacuum deposited onto the backside of the thin film using the transfer diaphragm ELO process. The bottom contact/mirror was broad area and the top contact had a window defined in the metal. Conventional detectors of with a 1.1 μm absorbing region, which have not been optimized for resonance, have a maximum theoretical quantum efficiency of 51%. These resonant cavity detectors had a theoretical maximum quantum efficiency of 78% and a measured quantum efficiency within 1.5% of the theoretical maximum. In addition, the cavity resonance could be tuned by wet etching the thickness of the AlGaAs layer exposed through the top contact window. The optimal depth of the controlled wet etch was monitored through the peak resonant photocurrent from the cavity, as illustrated in Fig. 3 [21].

An alternative to direct deposition of a high reflectivity layer onto a thin-film device is to use a high reflectivity host substrate to reduce reflection losses. Double heterostructure thin-film diodes bonded to high reflectivity substrates have exhibited internal quantum efficiencies of 99.7% and external quantum efficiencies of 72% under optical pumping [22]. Further improvements in light emitting diode efficiency have been demonstrated by adding a textured front surface to increase the escape cone of the light. External efficiencies as high as 30% have been demonstrated in such textured light emitting diodes [23].

Performance enhancements due to substrate removal can also be realized in MSM detectors by placing the metallized fingers on the bottom of the device, as illustrated in Fig. 4. This eliminates the primary drawback to MSM photodetectors: low efficiency due to finger reflection. MSM's are particularly attractive for integration with silicon circuits for low-cost OEIC's since, in comparison to p-i-n's, they have a larger surface area for the same capacitance. This larger surface area facilitates alignment tolerant packaging while maintaining the low capacitance necessary for high speed receiver OEIC operation. Current GaAs-based anti-reflection coated inverted MSM (I-MSM) exhibit a full width half maximum pulse response of 52 ps and a record external quantum efficiency of 95% (for MSM's under normal incidence at this speed) [24].

IV. Thin-Film Optoelectronic Integrated Circuits and Three-Dimensional OEIC's

The integration of thin-film devices with silicon integrated circuits opens OEIC's to the endless signal processing capabilities, inevitable improvements, and cost advantages of



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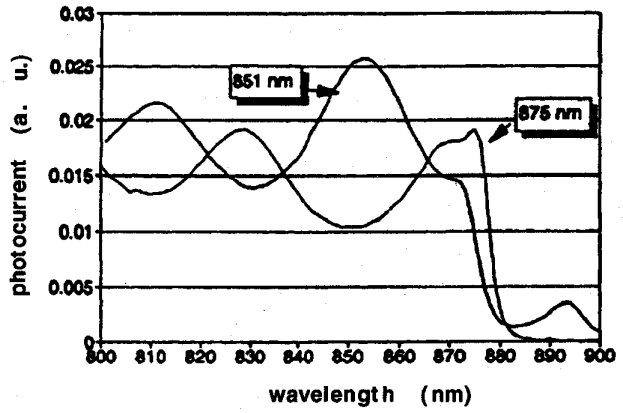
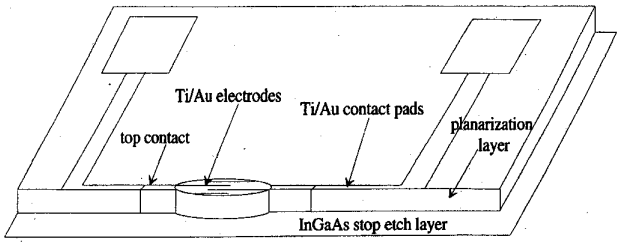


(b)

Fig. 3. Tuning of peak resonance of p-i-n photodetectors using a cavity wet etch method. Peak resonance shifted from 875 nm to 859 nm in the first etch step (top graph), and shifted to 851 nm with further etch tuning (lower graph).



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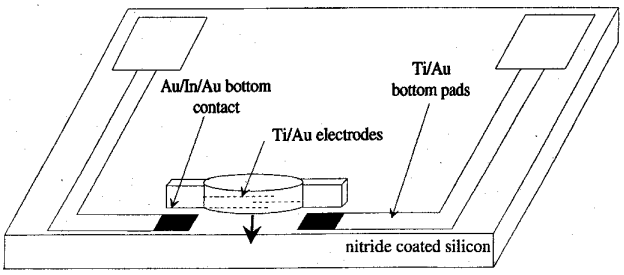


(b)

Fig. 4. (a) On-wafer MSM. (b) Inverted MSM integrated onto host substrate.

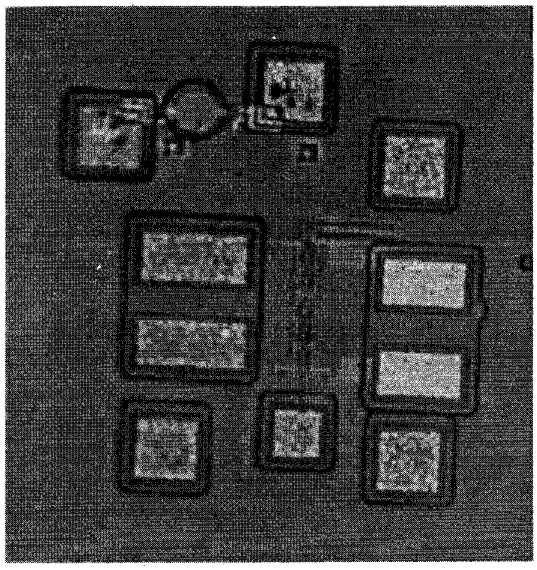


Fig. 5. Photomicrograph of a thin-film GaAs photodetector integrated onto a front-end transimpedance amplifier in 0.8 μm CMOS.

silicon circuitry. In particular, silicon CMOS is attractive for access to highly complex signal processing at a very low cost. Thin-film optoelectronics bonded to silicon circuits in post processing steps can offer enormous added value to silicon circuitry without decreasing silicon circuit foundry yields.

The integration of thin-film GaAs and InP-based thin-film detectors with silicon receiver circuits are excellent examples of this type of integration. GaAs-based P-i-N photodetectors have been bonded to a silicon front-end transimpedance amplifier fabricated through the MOSIS 1.2 μm digital CMOS process, and open eye diagrams have been demonstrated for 100 Mb/s NRZI pseudorandom data [25]. Figure 5 is a photomicrograph of the thin-film photodetector bonded to the CMOS receiver circuitry. In a second demonstration, a silicon front-end transimpedance amplifier was designed and fabricated through the MOSIS 0.8 μm standard digital CMOS process, and integrated with an inverted GaAs-based MSM, which demonstrated 155 Mb/s operation [26]. Thin-film emitters have also been bonded to silicon CMOS driver circuits, as shown in the photomicrograph in Fig. 6. The integrated devices emitted as LED's, and were controlled by the silicon circuitry.

Another interesting area of integration is that of thin-film devices with micromachines for sensor and alignment applications. Figure 7 shows a photomicrograph of a thin-film detector bonded to a polymer/metal micromechanical platform [27]. Note that a device with the substrate attached would be too massive for the platform, pinning it to the surface of the silicon. The light weight of the thin-film device did not impede the motion of the platform.

One of the most interesting integration techniques for thin-film devices is three-dimensional integration. The current two-dimensional nature of interconnect on circuitry (even

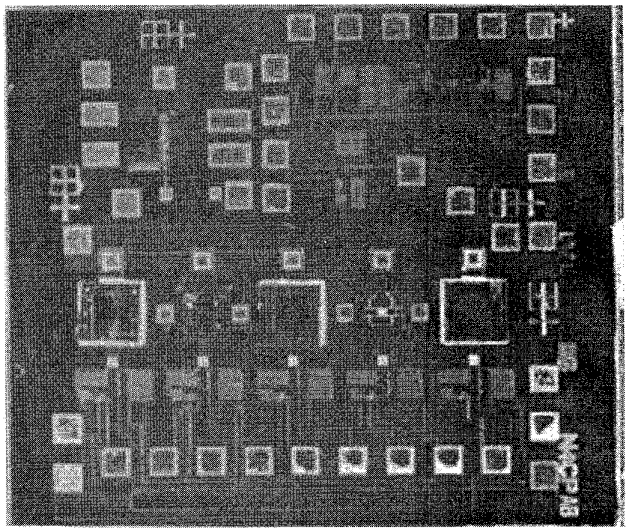


Fig. 6. Photomicrograph of three thin-film AlGaAs/GaAs emitters bonded to silicon CMOS driver circuitry.

Fig. 7. Photomicrograph of a thin-film AlGaAs/GaAs photodetector bonded to a polyimide/metal movable micromachine.

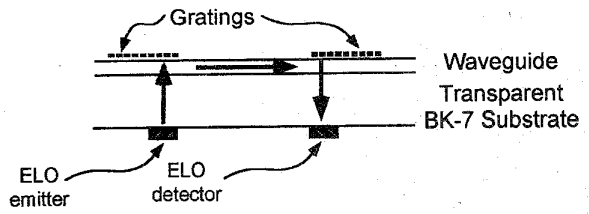


Fig. 8. Thin-film emitters and detectors have been integrated onto a BK-7 glass substrate for waveguide interconnect.

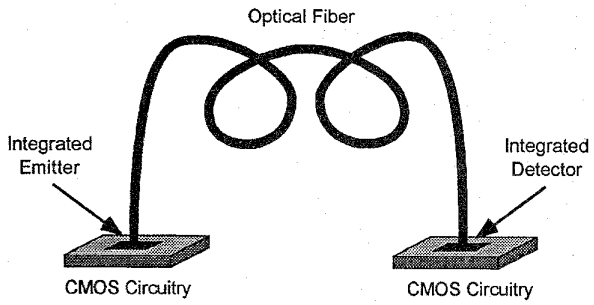
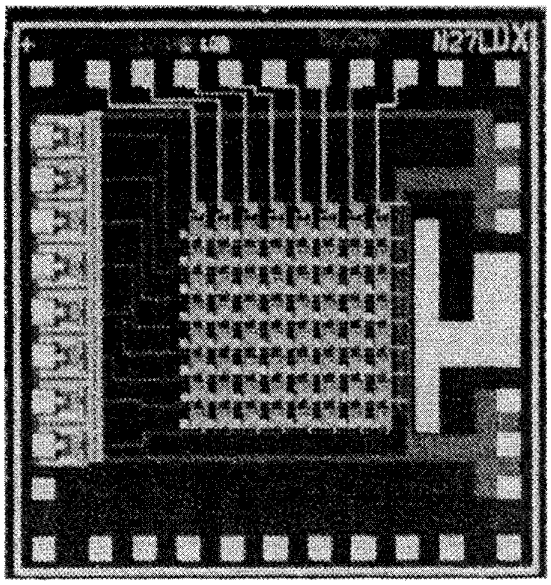


Fig. 9. Schematic diagram showing a vertical fiber optic interconnect between two CMOS circuits with integrated emitters and silicon detectors.

with multiple layers of metallization) limits processing density, and projections indicate that interconnection on and between integrated circuits is a burgeoning problem. The integration of thin-film devices for three-dimensional interconnect to circuitry is one approach which can alleviate the interconnection bottleneck. Three types of three-dimensional integration have been demonstrated: integrated emitters and detectors which use a waveguide for interconnection [28]–[32], the use of vertical electrical interconnections between layers of devices [33]–[35], and vertical optical interconnections between layers of stacked silicon circuits [36], [37]. The integration of thin-film emitters and detectors for chip-to-chip interconnect using waveguide interconnect has been demonstrated as illustrated in Figs. 8 and 9. For vertical electrical integration, the thin-film devices are bonded directly on top of polyimide-planarized silicon circuitry, and each thin-film device is electrically connected to the silicon circuitry below through a metallized via in the insulating polyimide. Likewise, the integration onto silicon host substrates of thin-film InGaAsP emitters and detectors which emit at wavelengths to which these silicon host substrates are transparent has led to the demonstration of vertical optical interconnection of layers of silicon using the silicon as a transparent host substrate and has expanded silicon parallel processing architectures into the realm of three-dimensional computation "cubes." This three-dimensional implementation technology is better suited to realize multicomputer interconnection networks than traditional planar wire-based techniques.

Thin-film ELO devices offer a unique opportunity for three-dimensional vertical electrical integration of layers of devices: these devices can be integrated directly on top of silicon circuitry with a layer of planarizing, insulating material which lies between the thin-film devices and the silicon circuitry. This vertical electrical three-dimensional integration of thin-film devices directly on top of circuits has been reported in two instances: first, the integration of a single GaAs-based MSM detector directly on top of a silicon amplifier circuit [36]; and second, an 8×8 array of thin-film GaAs-based p-i-n double heterostructure detectors bonded directly on top of a 8×8 array of luminance to frequency converter oscillator circuits [37]. Figure 10 is a series of photomicrographs of the steps in this integration process. The standard silicon chip, shown in Fig. 10(a) (from the MOSIS foundry) was planarized with DuPont polyimide PI2611, vias were etched in the polyimide using a reactive ion etch to reveal connection pads internal to the silicon circuitry, the vias (and top pads for the thin-film devices) were metallized, the thin-film devices were bonded onto the pads on top of the metallized vias, the devices were



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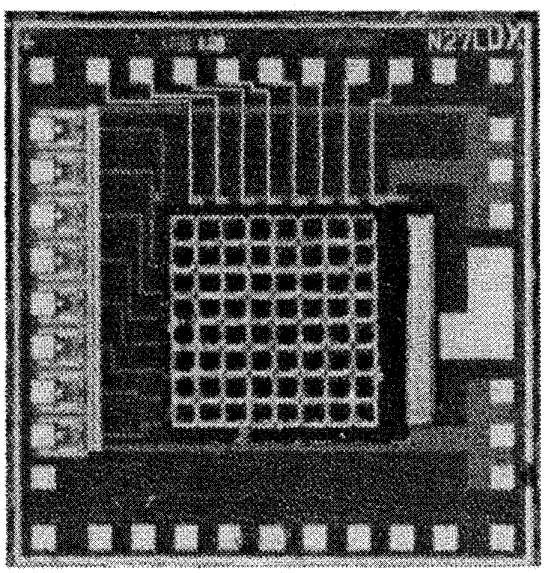

(b)

Fig. 10. Photomicrographs of an 8×8 array of photodetectors integrated onto silicon luminance to frequency converters. (a) Circuit prior to integration. (b) Completed OEIC.

planarized again to isolate the top and bottom contacts of the devices, and a top contact (with window) was deposited, as shown in Fig. 10(b). The circuits were simple current-controlled oscillators, loosely fashioned on the first layer of an inverted retinal neuron: with increasing incident light, the oscillator frequency increased (i.e., the neuron "fired" faster when more light was incident on the detector). All of the devices were operational, and a majority of the pixels exhibited 50 dB of dynamic range.

Vertical optical communication through stacked silicon (or GaAs) wafers enable high throughput multicomputer interconnections for massively parallel architectures. Optical interconnects can be high bandwidth, low crosstalk, low capacitance, provide isolation, and, for point-to-point interconnect (not using coherent interconnections), impervious to the flow of coolant. The integration of InP based thin-film emitters and detectors which emit and detect at wavelengths to which silicon (and GaAs) is a transparent host substrate enables this three-dimensional optical interconnection. Three-dimensional through-silicon wafer interconnection has been demonstrated with InGaAsP-based emitters and detectors integrated onto silicon host substrates using stacked silicon wafers, a single silicon wafer in a front to back of wafer communication scheme, and in a bidirectional manner using silicon circuits, as illustrated in Fig. 11 [36], [37].

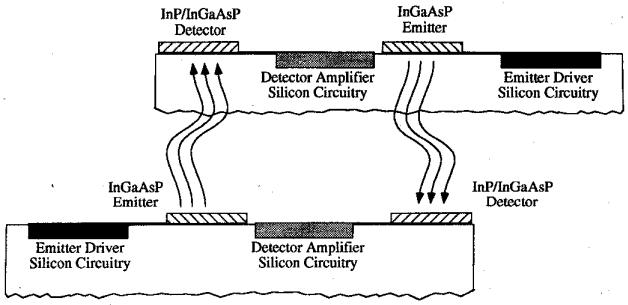

Fig. 11. Bidirectional communication through stacked silicon circuitry.

The extension of three-dimensional interconnection to parallel processing hardware is already underway [38]. Pica, a fine-grain, scalable, message passing architecture, has been designed to efficiently support high throughput parallel applications such as image processing and image generation (for virtual reality). This focus on high throughput applications allows a small local memory, but requires a high bandwidth interprocessor network. Several applications have been developed for this network and architecture, including JPEG image compression, positron emission tomography medical image reconstruction, thermal relaxation, and matrix multiplication. These applications have been implemented and executed using an instrumented instruction-level simulator. The simulation results suggest that Pica wil provide high performance and efficiency. High throughput applications and a low memory processing node make I/O a critical aspect of this architecture. Conventional wire-based interconnect technologies are inadequate for supporting dense, three-dimensional arrays of multinode chips at the required communication rate (3.2 Gb/s/chip), and cannot be easily when furture integrated circuit technologies offer more and faster transistors per chip. As an example of the power of this type of parallel processing system, a 4096 node Pica architecture is found to solve a positron emission tomography (PET) medical image reconstruction problem in 18.4 s, which is superior to the reported performance of parallel architectures based on a 4096-node DAP and a 4096-node MasPar, which take five minutes, and one minute, respectively. Compared to current workstation-based PET reconstructions, a total speedup of three orders of magnitude is achieved.

V. Conclusions

Thin-film integration is an attractive option for realizing multimaterial systems, in which the system designer can now access the cost and performance opportunities of silicon for circuitry, glass, lithium niobate and polymers for waveguides, and micromachines for motion, and three-dimensionally interconnected structures. The performance of thin-film devices separated from the growth substrate is comparable, and, in some cases, better, than on-wafer counterparts. Integration of thin-film devices with circuits to form OEIC's offer a high potential for added value to silicon, particularly in the area of interconnection. Three-dimensional vertical electrical and optical interconnections, which enables the stacking of layers of silicon processing circuitry for parallel processing, leads to exciting hardware and architectural possibilities, which promise to leap beyond the capabilities of silicon alone.

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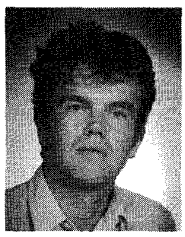

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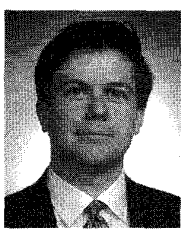

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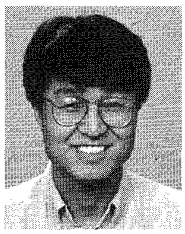

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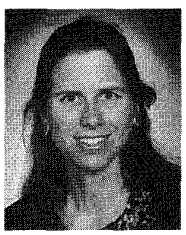

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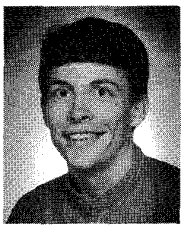

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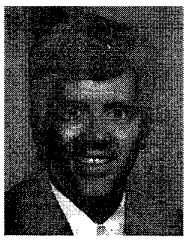

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