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CMOS Optical Receiver with Integrated Compound Semiconductor Thin-Film Inverted MSM Detector Operating at 155 Mbps

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Low cost silicon digital CMOS foundry circuitry is a prime candidate for low cost, high performance optoelectronic receivers for cost considerations, and also since digital circuitry can also be incorporated with the analog receiver circuitry on the same chip. Silicon detectors, however are not as efficient as compound semiconductor detectors. Hybrid packaging of compound semiconductor detectors and silicon circuitry places limitations on the silicon circuitry due to the package terminations, which are usually 50 Ω. To utilize high efficiency, high speed compound semiconductor circuits with silicon circuitry, and to relax the circuit design constraints which are imposed by 50 W terminations, we report herein the integration of a double heterostructure GaAs-based high efficiency inverted (fingers on the bottom) metal-semiconductor-metal (I-MSM) thin film photodetector [1] bonded directly onto the silicon receiver circuit.

The use of MSMs is attractive for receiver optoelectronic integrated circuits (OEICs) due to their low capacitance per unit area. The integration of P-i-N detectors with a silicon circuitry has been reported previously [2]. However, MSMs are preferable in that, to achieve the capacitance specification dictated by the silicon circuit, the MSM will have a larger area than a p-i-n with the same capacitance, resulting in a higher alignment tolerance. The I-MSMs overcome the major drawback to MSMs (the low efficiency due to finger shadowing) since the fingers are on the bottom of the MSM, without degrading the speed or capacitance of the device. Thus the OEIC integrated with I-MSMs is suitable for low incident light power and high data rates, thus reducing the trades off between sensitivity, speed and optical alignment tolerances.

The thin film I-MSM structure consisted of a double heterostructure with a sacrificial etch layer: GaAs (substrate)/AlAs (sacrificial etch layer)/$Al_{.3}Ga_{.7}As$/GaAs/$Al_{.3}Ga_{.7}As$, with all layers nominally undoped. Fingers of Ti/Pt/Au 2 μm wide separated by 2 μm were defined on the 50 μm diameter MSMs before mesa etching and separation of the MSMs from the growth substrate. After an Apiezon W handling layer was applied, HF was used to separate the thin film MSMs from the growth substrate. These I-MSM photodetectors exhibited high efficiency (65 %) and low dark current (< 5 nA at 10 V bias), as shown in Fig. 1. Using a transfer diaphragm, the thin film I-MSMs were inverted and bonded to Cr/Au/In/Au pads defined on the silicon circuits as shown in Fig. 4, with a subsequent anneal at 200 °C for multilayer reflow to insure high quality bonding between the circuit and the thin film MSM. The circuit was then encapsulated with polyimide, and optical and electrical vias through the polyimide were etched using RIE.

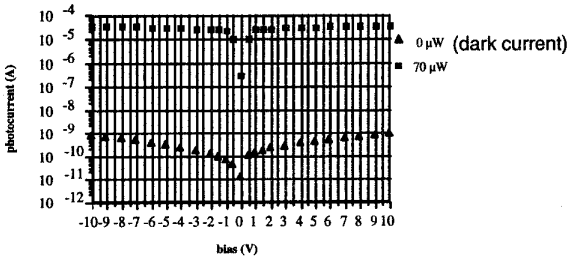

Figure 1. I-V characteristics of I-MSM detectors.

The front-end transimpedance amplifier was designed and fabricated through the MOSIS foundry 0.8μm standard digital CMOS process. A multi-stage, low-gain per stage, and open-loop design was used to increase the

bandwidth of the circuit. The amplifier consists of 5 identical stages, as shown in Fig. 2. Each stage, as shown in Fig. 3, has a current gain of 3. The total transimpedance gain is about 12KΩ under a 50 Ω load.

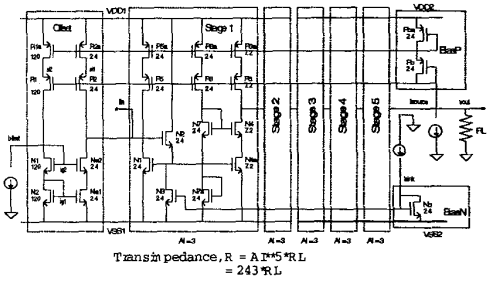

Figure 2. Overall block diagram of the digital CMOS transimpedance amplifier.

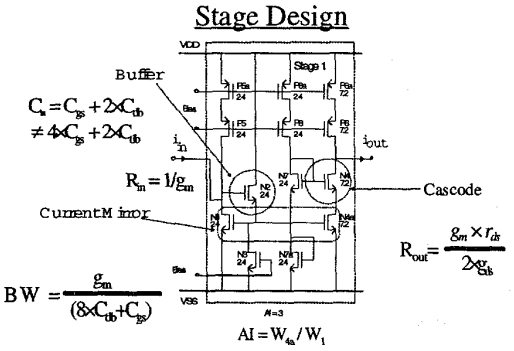

Figure 3. Circuit diagram of a single stage.

Since the amplifier is used in the current-mode, the signal current from the MSM photodetector is sent directly into the input of the amplifier without requiring any bias resistor. Therefore, we can minimize parasitic effects.

Fig. 4 is a microphotograph of the completed OEIC. The power supply rails are split to prevent the larger output signal swings from generating small feedback signals in the sensitive small signal parts of the circuit. Another aspect of the design that reduces unwanted coupling into input signal is the long, thin left-to-right geometry of the layout. Small input signals enter on the far left, while the output signal exit on the far right. This maximizes the separation of the sensitive input stages from the larger signal output stages.

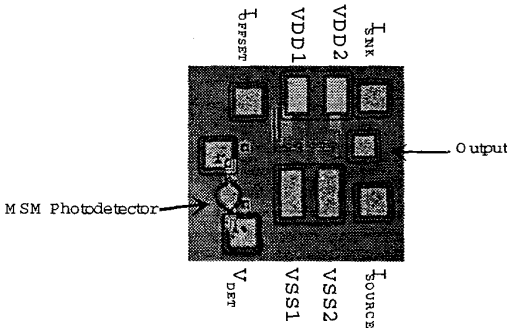

Figure 4. Chip photograph after integration.

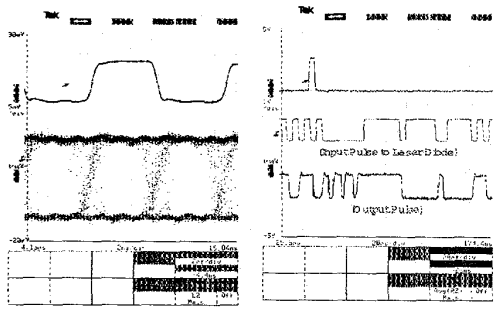

Figure 5. Eye diagram and output pulse.

The eye diagram of this integrated receiver OEIC, shown in Fig. 5, was measured at 155 Mb/s using NRZ pseudorandom data and a pulsed waveform operating at 170Mb/s. Power dissipation was about 25 mW and ± 2.5V power supplies were used. For the test, a commercial 1mW CW laser diode was modulated by a current source and the pseudorandom signal was fed through a bias tee. The magnitude of the output pulse in Fig. 5(b) was about $20mV_{p-p}$. The uniformity of the output amplitude at several different frequencies indicated that the device operated well within bandwidth specification.

References

[1] Olivier Vendier, Nan Marie Jokerst, Richard P. Leavitt, "High efficiency inverted MSM photodetector", *Technical digest CLEO 95*, vol 15 pp 177-178, May 1995.

[2] M. Lee, C. Camperi-Ginestat, M. A. Brooke, and N.-M. Jokerst, "Silicon CMOS optical receiver circuit with integrated compound semiconductor thin-film P-i-N detector," *Tech. Dig. LEOS '94 Summer Topical Meeting*, pp. 58-59, July 1994

[3] M. Lee and M. A. Brooke, "Design, Fabrication, and Test of a 125Mb/s Transimpedance Amplifier Using MOSIS 1.2mm Standard Digital CMOS Process," *Proc. 37th Midwest Sym. Cir. and Sys.*, Lafayette, LA, pp. 155-157, Aug. 1994.