8 × 8 Array of Thin-Film Photodetectors Vertically Electrically Interconnected to Silicon Circuitry

S. M. Fike, B. Buchanan, N. M. Jokerst, *Member, IEEE*, M. A. Brooke, T. G. Morris, and S. P. DeWeerth

Abstract— This paper reports the integration of an 8 × 8 array of thin-film GaAs–AlGaAs photodetectors onto a silicon-oscillator array circuit for massively parallel-image processing applications. Each detector was electrically connected to the oscillator below it using vertical electrical interconnections. Both sides of the thin-film devices were metallized for electrical contact, which minimized the interconnection density on the silicon circuit, thereby maximizing the available signal processing area. The yield of this integrated array and associated circuit was 100%, with the majority of pixels demonstrating a dynamic range of 50 dB.

I. INTRODUCTION

IMAGES are effective modes of communication of information and, with advanced image processing, the transmission and processing of image information is increasingly pervasive. Since image information is inherently parallel, the most efficient mode of image capture and processing is parallel. Other image capture systems such as bump-bonded focal plane arrays have achieved a high level of parallel data processing through the interconnection of each detector to focal-plane image processing circuitry [1]. Inherent limitations to bump-bonded systems include the coefficient of thermal expansion (CTE) mismatch which often exists between the detector material and the circuitry, limiting the surface area of the detector array and the fact that the substrate used for the detector array must be optically transparent. The use of thin-film compound semiconductor device arrays in conjunction with three-dimensional integration on top of silicon circuitry, addresses both of these issues. The individual devices are separate from one another, creating less strain on the bonds due to CTE mismatch. Also, there is no substrate, hence, the substrate transparency issue does not apply. In addition, since the semiconductor devices are contacted on both sides, in comparison to devices with planar contacts, the structure can be optimized, and device fabrication simplified, which can have a significant impact on yield and cost.

This paper reports the integration of an array of thin-film compound semiconductor detectors directly on top of silicon processing circuitry, enabling massively parallel processing of image information. The use of epitaxial lift-off [2] with a

transfer diaphragm [3] enables individually addressable pixels with a minimum interconnect density on the silicon circuit. An 8 × 8 array of thin-film p-i-n photodetectors was integrated directly on top of a silicon MOSIS tinychip using epitaxial lift-off and a transfer diaphragm. An insulating layer of polyimide was used to planarize the circuit, and the photodetectors were integrated directly on top of the polyimide. Using the p-i-n structure with this 3-D integration, realized separate layers of detection and processing with a common contact on the top of the detector array, maximizing the tinychip area dedicated to processing circuitry. This paper will discuss the fabrication of the detector array, integration of the array onto the silicon circuitry, and the testing of the completed optoelectronic integrated circuit (OEIC). The yield of this OEIC was 100%, with the majority of pixels demonstrating a dynamic range of 50 dB.

II. PROCESSING AND FABRICATION

The thin-film detector array was fabricated through removal of the growth substrate followed by bonding onto the planarized silicon circuit. The compound semiconductor detector array was fabricated from AlGaAs–GaAs–AlGaAs double heterostructure (DH) p-i-n material. The lattice-matched detector material, as grown, consisted of a semi-insulating GaAs substrate–AlAs (undoped, 2000-Å) sacrificial etch layer–$Al_{0.3}Ga_{0.7}As$ ($n_o = 10^{19}$ cm^{-3}, 5000 Å)–GaAs (undoped, 1.1 μm)–$Al_{0.3}Ga_{0.7}As$ ($p_o = 2.5 \times 10^{17}$ cm^{-3}, 5000 Å). To achieve the three-dimensional electrical interconnect, a silicon circuit consisting of an 8 × 8 array of oscillators [as shown in Fig. 1(a)] was spin coated with a layer of du Pont polyimide PI2611, baked at 130 °C in air for twenty minutes, and then cured at 350 °C in nitrogen for one hour. An aluminum mask with an 8 × 8 array of 25-μm vias centered over the circuit pads was vacuum deposited onto the polyimide. Vias were etched in the polyimide using a reactive ion etch (RIE) with 5% CHF_3 and 95% oxygen to expose the underlying metal pads on the circuit. The aluminum mask was then removed with a sodium hydroxide wet etch. Ti–Au (150 Å/3000 Å) was deposited onto the circuit to electrically connect the underlying circuit to the surface of the polyimide. The Ti–Au was then patterned into an 8 × 8 array of pads (100-μm pads spaced by 25 μm), with each pad centered over a via in the polyimide. These pads served as the bottom contact for the photodetectors.

To obtain the high quality GaAs devices necessary for the integration, epitaxial lift-off (ELO) was utilized [2]. This technique takes advantage of the wet-chemical etch selectivity
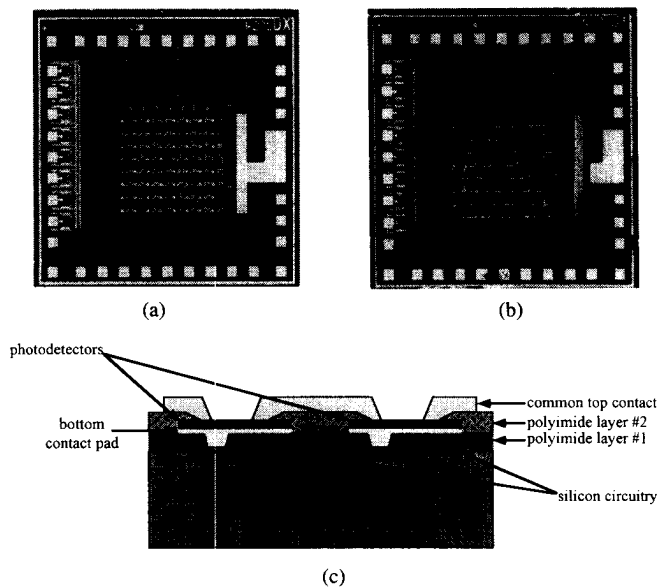
Fig. 1. Photomicrographs of (a) the MOSIS silicon tinychip, (b) the fully integrated OEIC, and (c) a cross-sectional drawing of the integrated OEIC.

between AlAs and $Al_xGa_{1-x}As$ with aluminum concentrations less than 30%. Prior to separating the detector epilayers from the GaAs substrate, a p-type ohmic contact was deposited onto the structure and patterned into an 8 × 8 array of 100 μm squares separated by 25 μm. Using a selective wet-chemical etch, the structure was mesa-etched to a depth of 0.5 μm, and the array was repatterned with a 50-μm connecting bar between each pixel. The connected array was then selectively mesa etched to the AlAs stop layer, separated from the substrate through a sacrificial etch of the AlAs layer in HF: H_2O (1:10), and transferred [3] to a transparent du Pont mylar diaphragm. Next, the connected array was aligned and contact bonded to the Ti–Au pads on the planarized circuit. To define 64 individual devices, the linking material was removed using $SiCl_4$ in the RIE. The photoresist was then removed, and a single layer of du Pont polyimide PI2611 was spun on top of the circuit and cured to electrically isolate the bottom pads of the array from the top. An 8 × 8 array of vias was etched in the polyimide using RIE; the via size was 75 μm, and each via was centered over a photodetector. A via was also opened over a common bias contact on the circuit for electrical connection of the common top contact of the detectors to the processing circuitry. A broad area n-type top contact was vacuum deposited on top of the array, which covered all of the array and the common bias contact on the circuit. This contact had a 60 μm window over each detector. The excess polyimide was then removed from the circuit using 100% oxygen in the RIE, as shown in Fig. 1(b). A cross-sectional view of the integration is shown in Fig. 1(c). The circuit was then wire bonded into a standard 40 pin dual-in-line package for testing.

Electrical contacts on both sides of the thin-film devices enabled the array pixels to be individually addressed through the bottom contacts and share a common top contact. Individual addressing of each detector was preserved while maximizing the silicon circuit processing density. The silicon circuit interconnect density is minimized through this single common connection, since only one pad on the circuit is dedicated to the common top electrical contact for the entire array. This is in contrast to integration techniques which use planar contacts [4], necessitating two contacts per device, and the associated silicon area devoted to this interconnection. In addition, the ability to optimize device structure and simplify device fabrication (which impacts yield and cost) is also greater with the option to contact both sides of the thin-film device. The common contact technique can also be extended to the first demonstration of thin-film devices integrated on top of a silicon circuit, which involved a thin film metal-semiconductor-metal photodetector [5].

III. TESTING

The circuit integrated with the p-i-n photodetectors was an 8 × 8 array of current controlled oscillators fabricated in 2-μm CMOS through the MOSIS foundry. The core of the oscillator was a loop of three digital inverters, with one of the inverters current limited through current mirrors controlled by the photodetector. The photodetector current regulated the switching speed of this inverter stage, which in turn regulated the frequency of the oscillator. Additionally, the current limited inverter was also slowed by the capacitor tied between the inverter input and output. The output of each circuit in the array was then passed through a column-wise selectable transfer gate so that an entire column at a time was connected to the output buffers where the signal was then amplified and driven off chip. The bilevel output signal of this circuit was designed to provide high-noise immunity by encoding the signal information in pulse width rather than amplitude. A high dynamic range, spanning many orders of magnitude, was inherent in this data format, with the lower limit of the oscillation frequency set by the amount of time that any of the following signal processing layers were capable of waiting, and the upper limit set by characteristics intrinsic to the fabrication technology, such as parasitic capacitances.

The circuit output an oscillation frequency for each pixel, which was a function of incident light intensity. The test setup consisted of a HP lightwave multimeter with an 850-nm laser, an attenuator, a digital oscilloscope, and connectorized multimode fiber. Measurements of the output intensity from the laser/attenuator/fiber were taken with a calibrated germanium detector. A micropositioner was used to align the fiber over each pixel to obtain device characteristics. A five volt bias was applied to the input of the circuit and the oscilloscope was connected to each pixel output pad sequentially, to measure the frequency response for varying optical input power. An example of the change in oscillation frequency due to changing the attenuation of the laser can be seen in Fig. 2: a) The attenuation is zero and the circuit is clearly slew rate limited, b) the attenuator is set for 8 dB and the circuit is still slightly slew rate limited and ringing is apparent, c) the attenuator is set for 48 dB and a clean square wave is apparent, and d) is a measure of the oscillation due to the dark current of the detector (zero incident light power). Because every pixel was electrically active while the data was taken one pixel at a time, crosstalk was evident. Some of the pixels may have a higher
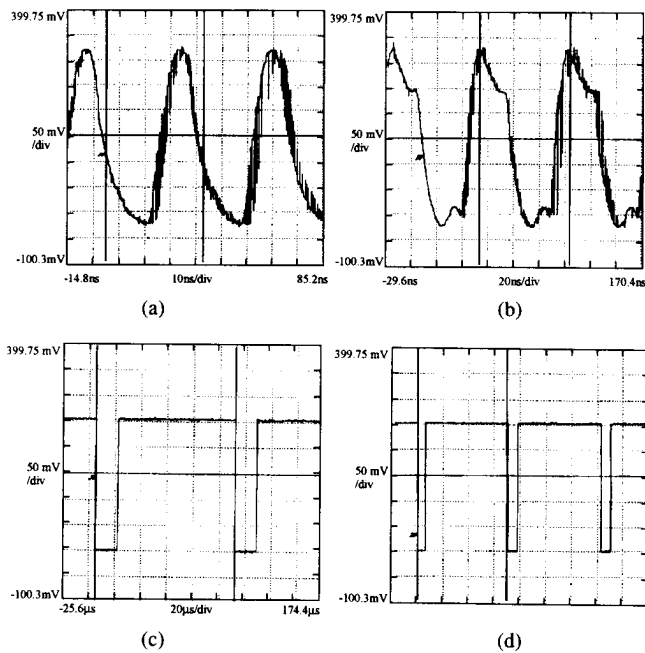
Fig. 2. Frequency response of a single pixel for varying laser output powers (a) incident power 374.8 μW, oscillating frequency 26.18 Mhz, (b) incident power 59.4 μW, oscillating frequency 14.2 Mhz, (c) incident power 6 nW, oscillating frequency 9.939 kHz, and (d) incident power 0 W (i.e., dark), oscillating frequency 5.682Hz.

Fig. 3. Oscillation frequency versus incident power for all 64 pixels of the array.

maximum oscillating frequency than recorded, but crosstalk problems precluded a clean trigger on the oscilloscope for some of the pixels.

While there were approximately four different maximum value ranges of oscillating frequencies in the array, the pixels followed a general trend in the slope of the frequency as a function of incident power, as shown in Fig. 3. Independent of the fact that the devices had a maximum oscillating frequencies in excess of 20 MHz, around 1–5 MHz, in the 100 kHz range, or under 100 kHz, the majority demonstrated seven decades (50 dB) of operation from 0 dB attenuation (maximum optical power input) to dark, and all of the pixels were functional.

IV. CONCLUSION

An array of thin film photodetectors has been integrated with vertical electrical interconnects onto standard foundry silicon circuitry. Using an 8 × 8 array of AlGaAs–GaAs–AlGaAs thin-film detectors and linking material, each detector was integrated directly on top of an oscillator with 100% yield on the fully integrated silicon circuit, with a majority of the pixels demonstrating 50 dB dynamic range. This three-dimensional, vertical electrical integration of thin-film devices onto silicon
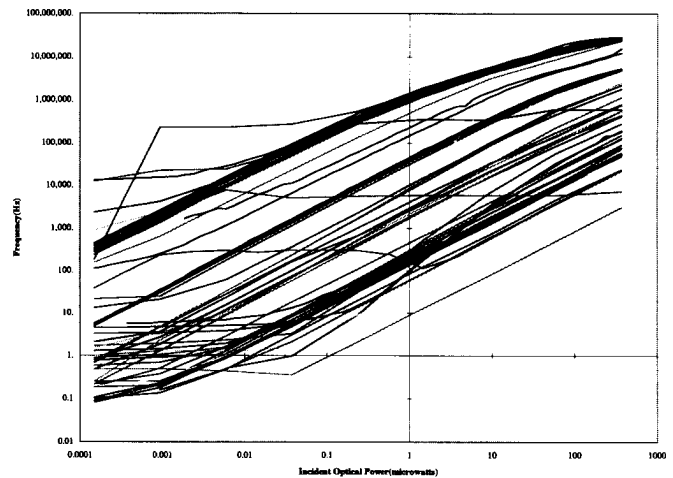
circuits, using contacts on both sides of the devices, is an attractive method for achieving massively parallel image capture and processing hardware with a high-silicon circuit processing density.

REFERENCES

[1] For a review of results see the "Special issue on solid state image sensors," IEEE Trans. Electron . Dev., vol. 38, 1991.
[2] E. Yablonovich, T. J. Gmitter, J. P. Harbison, and R. Bhat, "Double heterostructure GaAs/AlGaAs thin film diode lasers on glass substrates," IEEE Photon. Technol. Lett., vol. 1, pp. 41–42, 1989.
[3] C. Camperi-Ginestet, M. Hargis, N. Jokerst, and M. Allen, "Alignable epitaxial lift-off of GaAs materials with selective deposition using polyimide diaphragms," IEEE Photon. Technol. Lett., vol. 3, pp. 1123–1126, 1991.
[4] K. W. Goossen, J. A. Walker, L. A. D'Asaro, S. P. Hui, B. Tseng, R. Leibenguth, D. Kossives, D. D. Bacon, D. Dahringer, L. M. F. Chirovsky, A. L. Lentine, and D. A. B. Miller, "GaAs MQW modulators integrated with silicon CMOS," IEEE Photon. Technol. Lett., vol. 7, pp. 360–362, 1995.
[5] C. Camperi-Ginestet, Y. W. Kim, N. M. Jokerst, M. G. Allen, and M. A. Brooke, "Vertical electrical interconnection of compound semiconductor thin-film devices to underlying silicon circuitry," IEEE Photon. Technol. Lett., vol. 4, pp. 1003–1006, 1992.