Communication Through Stacked Silicon Circuitry Using Integrated Thin Film InP-Based Emitters and Detectors

N. M. Jokerst, *Member, IEEE*, C. Camperi-Ginestet, B. Buchanan, S. Wilkinson, and M. A. Brooke, *Member, IEEE*

***Abstract*— To demonstrate optical communication through stacked silicon circuitry, thin film InGaAsP-based emitters and photodetectors have been bonded directly onto silicon circuitry. These optoelectronic devices operate at a wavelength to which silicon is transparent. The thin film emitters and detectors were integrated onto a MOSIS foundry silicon CMOS integrated circuit which contained driver and amplifier circuits. Bidirectional vertical optical communication between two layers of circuitry was demonstrated by stacking the layers, exciting the emitter driver circuit on one layer with an electrical signal, and measuring the output electrical signal from the detector amplifier located on the other circuit in the vertical stack.**

I. Introduction

THE integration of compound semiconductor devices with silicon circuitry enables system designers to realize new optoelectronic interconnection options in silicon circuitry. Identification of the realms in which optoelectronic interconnection can realistically impact silicon signal processing circuitry (the acknowledged leader for low-cost, highly-complex signal processing) is currently a pressing need. In this paper, one application realm is discussed and experimentally demonstrated—the vertical, through-silicon optical interconnection of stacked planes of standard silicon-foundry circuits. This work addresses a current problem with silicon circuits which will continue to worsen with time: the processing density of silicon circuitry is limited by the two-dimensional nature of the interconnections on silicon circuits. Most foundry-based silicon circuits contain two to nine metallization layers, however, each additional layer adds significant complexity and requires additional chip area for vertical connections. The interconnection complexity of silicon processing circuitry dictates a need for much more interconnect. As a result of this interconnection need, increasing amounts of surface area on silicon integrated circuits are devoted to interconnection, thus limiting the area available for signal processing circuitry. Multichip modules (MCM's) address this interconnection issue through the use of multiple layers of interconnection metallization interleaved with dielectric [1], however, these MCM's are expensive and, in some parallel processing cases, long-metallized interconnection pathways can introduce signal latency problems. Parallel vertical-optical interconnection can address these problems in silicon circuits and can be used to realize massively parallel silicon-based processing topologies which are attractive architectures for many applications, in particular, image processing and generation. One application of the research, presented in this paper, is the utilization of these optoelectronic interconnections in a three-dimensional parallel processing architecture [2].

To extend the interconnectivity of silicon into the third dimension, the through-silicon vertical-optical interconnection of two low cost foundry silicon circuits is presented in this paper. Vertical-optical interconnection of layers of silicon circuits have been previously demonstrated using external light sources [3], and through-silicon wafer commnication, using integrated thin-film emitters and detectors, has also been demonstrated [4]. The vertical-optical interconnection reported herein is achieved with completely self-contained integrated thin film emitters, detectors, and silicon driver and amplifier circuitry. The only inputs to and outputs from this stack of silicon circuits are electrical; no external optical sources or detectors are utilized since the optical communication is completely contained in the thin film optoelectronic devices which are bonded directly to the silicon signal processing circuitry. The thin film InGaAsP-based emitters and detectors, which realize this optical interconnect, operate at a wavelength greater than 1.2 μm, to which the silicon is transparent. This three dimensional (3-D) optoelectronic integrated circuit (OEIC) is bidirectional, as illustrated in Fig. 1. Both communication down through the silicon circuit on the top, and up through the silicon circuit on the bottom, are demonstrated using two separate channels, which are both integrated into a single chip.

II. Processing and Fabrication

The InP-based compound semiconductor emitters and detectors were each grown lattice matched to an InP substrate using liquid phase epitaxy, and were subsequently separated from the growth substrate using selective etching, commonly referred to as epitaxial lift off or total substrate removal. The separation of thin film InP-based devices from the growth substrate for subsequent integration onto

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The authors are with the School of Electrical and Computer Engineering, Microelectronics Research Center, Manufacturing Research Center, Georgia Institute of Technology, Atlanta, GA 30332-0269 USA.

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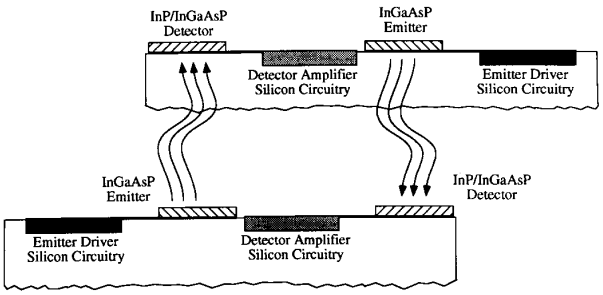

Fig. 1. Schematic of the bidirectional vertical-optical interconnection scheme using stacked silicon circuits. Each silicon integrated circuit contains a thin film emitter bonded to a driver circuit and a thin film detector bonded to a single driver/amplifier circuit.

host substrates has been reported by a number of groups, and usually employs a HCl etch for selective substrate removal [5]–[7]. The homojunction emitter was, as grown, InP (substrate)/$In_{0.70}Ga_{0.30}As_{0.64}P_{0.36}$ ($n_0 = 10^{18}\,cm^{-3}$, 2-μm thick)/$In_{0.70}Ga_{0.30}As_{0.64}P_{0.36}$ ($p_0 = 3 \times 10^{17}\,cm^{-3}$, 1.5-$\mu$m thick), designed to emit at a wavelength of 1.26 μm. The double heterostructure InP–InGaAsP–InP detector also included an extra InGaAsP stop etch layer in between the substrate and the thin film device to be integrated. The grown structure consisted of: InP (substrate)/$In_{0.70}Ga_{0.30}As_{0.64}P_{0.36}$ (process undoped stop etch layer, 5-μm thick)/InP ($n_0 = 10^{18}\,cm^{-3}$, 0.5-μm thick)/$In_{0.70}Ga_{0.30}As_{0.64}P_{0.36}$ (process undoped, 1-μm thick)/InP ($p_0 = 3 \times 10^{17}\ cm^{-3}$, 0.5-$\mu$m thick). Prior to the separation of the epitaxial devices from the growth substrate, a AuZn–Au (50/200 nm) p-type ohmic contact was vacuum deposited onto each of the structures. The metal was patterned to define 250 μm × 250-μm squares which also served as mesa etch masks. After mesa etching, windows in this metallization were opened in 50% of each type of the devices, which were the fraction that were to be inverted and integrated onto the top silicon circuit. The detector and emitter arrays were each bonded to a separate transparent Mylar diaphragm for transfer and bonding to the host silicon circuit. At this point, there were four types of devices on two separate transfer diaphragms: on the first diaphragm emitters with and without windows in the metallization, and on the second diaphragm, detectors with and without windows in the metallization. The mesa etch, substrate removal, and transfer diaphragm are described in detail elsewhere [4].

The emitter and driver circuits were both located on a single MOSIS foundry TinyChip fabricated in 2-μm CMOS. The driver circuit for the light emitting diode was a simple three stage transconductance amplifier, and the detector amplifier was a single diode-connected n-type MOSFET.

The thin film devices were integrated onto an overglass-coated section of the silicon circuit. For the top OEIC layer, these integration areas did not have underlying metal layers which would block optical signal transmission. To integrate the thin film detector onto the silicon amplifier and the thin film emitter onto the silicon driver, a Ti–Au (15/250 nm) metallization was vacuum deposited onto the Al CMOS circuit driver and amplifier pads with leads into the integration area. The Ti–Au metallization was used to prevent degradation which occurs over time at interfaces between Al and Au and to promote adhesion of the Au leads to the overglass areas. Windows were then opened in these metallization layers on the top circuit for optical signal transmission. A detector on the Mylar diaphragm was aligned and bonded to the lead connected to the amplifier, and an emitter on the other Mylar diaphragm was aligned and bonded to the lead connected to the driver circuit. The devices with windows were integrated onto the top circuit, and those without windows onto the bottom circuit. The thin film devices were inverted in the transfer process, thus contacts can be deposited onto both sides of the devices while under either growth or host substrate support.

The optoelectronic devices were planarized using spin coated polyimide (DuPont PI2611). An Al mask was vacuum deposited and patterned on the polyimide, and windows were opened in the polyimide using a reactive ion etch of O_2/CHF_3 (90%/10%). The n-type contact, AuGe–Ni–Au (50/15/200 nm), was then evaporated onto the top of the devices, connecting the n-type side of the detector to the positive amplifier bias and the n-type side of the emitter to the negative driver bias. Thus, the detector was reverse biased by the amplifier and the emitter was forward biased by the driver. Optical windows were patterned in the n-type contact metallization on the top of the emitter and detector for the circuit which constituted the bottom layer of the 3-D OEIC.

The result of these fabrication steps was two Si–InGaAsP OEIC's, one emitting to and accepting signals from above (bottom chip in the stack), and one from below (top chip). One OEIC was rotated relative to the other by 180° to align the emitter/detector pairs (as in Fig. 1), and the OEIC's were stacked to form the 3-D OEIC. The MOSIS foundry delivers silicon integrated circuits which are not polished on the back side, which will increase scattering of the signals as they pass through the top wafer. However, to reduce processing steps in this proof of concept 3-D OEIC, the back side of these circuits were left unpolished. The bidirectional optoelectronic interconnect demonstrated is alignment tolerant, since the two channels are separated by approximately 900 μm on the silicon circuits. Thus precise alignment was not necessary to demonstrate the function of the 3-D OEIC, and the two OEIC's were stacked and aligned by hand without the aid of a microscope.

III. Results and Discussion

The 3-D OEIC was tested to demonstrate bidirectional communication. The silicon driver circuit with integrated thin film emitter and the silicon amplifier circuit with integrated thin film detector were tested prior to stacking of the chips. The detectors exhibited responsivities of 0.5 A/W, the transresistance amplifier had variable output resistance in the MW range, and the LED's typically had efficiencies of less than 1%.

Bidirectional optoelectronic through-silicon communication was demonstrated using both dc and pulsed signals. Fig. 2 shows the measured output current from the integrated detector and amplifier as a function of input drive voltage and power supply current to the integrated LED and driver for one channel of the bidirectional system. This response is consistent

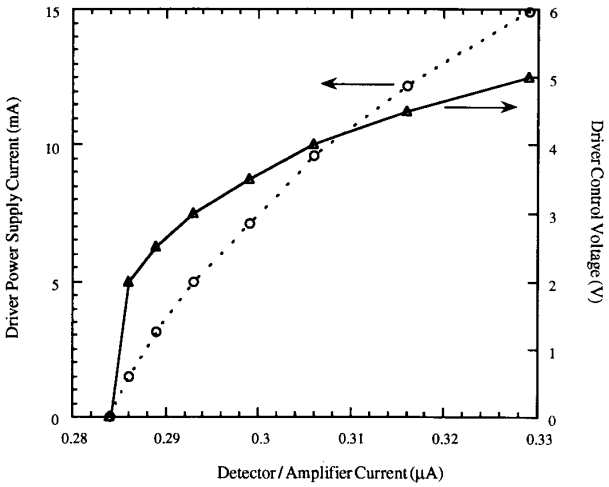

Fig. 2. Output of the amplifier circuit as a function of the input current to the emitter driver circuit.

with the circuit gain, with the efficiency of the optoelectronic devices, and with the optical coupling from emitter to detector. Analysis of the coupling from the emitter to the detector was performed using an LED dispersion angle of 23.7°, which is typical for similar GaAs-based thin film emitter devices [8]. Assuming 50–60% loss at the rough back surface of the top circuit, the amplifier output shown in Fig. 2 corresponds to an offset of 400 μm in any single direction (less if the offset is in more than one direction) [9]. Since the two circuits were manually aligned in this proof-of-concept device, an offset of 0.4 mm is plausible. With improved alignment and polished back surfaces, we expect to see a greater than 15 times improvement in the amplifier output.

The pulsed measurements for both channels of the interconnect are shown in Fig. 3. In Fig. 3(a), the lower trace is the current input to the LED driver, and the upper trace is the inverted output of the detector amplifier measured through a 1 MΩ external transimpedance amplifier. Unfortunately, the second channel of the 3-D OEIC was plagued by a noisy detector, as illustrated by the same measurement performed on the second channel, shown in Fig. 3(b). This problem is not inherent to this process or design; better quality detector material is necessary. These two measurements clearly indicate that the through-wafer interconnect is functional—that an electrical signal input to the lower silicon circuit exits as an electrical signal from the upper silicon circuit, and vice-versa, for the second arm of the bidirectional interconnect.

IV. Conclusion

The bidirectional, three-dimensional interconnection of two low cost, foundry silicon circuits has been demonstrated using thin film InGaAsP-based emitters and detectors bonded to silicon integrated circuits. This through-silicon wafer vertical optical interconnection was demonstrated through the use of emitters and detectors that operate at a wavelength to which the silicon is transparent. This type of 3-D OEIC holds promise for the implementation of massively parallel, three dimensional processing topologies realized in systems comprised of low

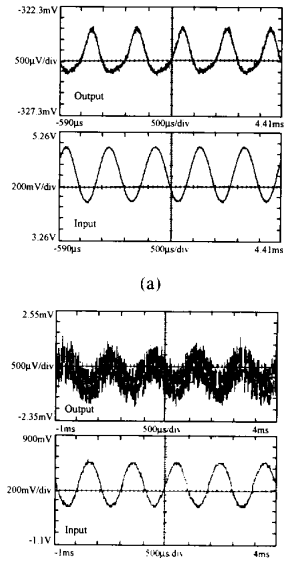

Fig. 3. (a) Response of the upper amplifier circuit for a pulsed input current to the lower emitter driver circuit (for the first vertical optical communication channel). (b) Response of the lower amplifier circuit for a pulsed input current to the upper emitter driver circuit (for the second vertical optical communication channel).

cost silicon circuitry integrated with thin film semiconductor devices for 3-D optoelectronic interconnections.

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