BEHAVIORAL SIMULATIONS OF A SELF-CORRECTING A/D CONVERTER ARCHITECTURE

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Abstract Behavioral simulations of an experimental A/D converter architecture using the Saber simulator are presented. Offsets, gain errors, and higher order nonlinearities of various converter components were modeled, and simulations confirmed the ability of the converter to calibrate around these nonidealities.

In the design of A/D converters, nonideal characteristics of the various converter components can be critical in determining the overall resolution achievable from a design. Offsets, gain errors, and higher order nonlinearities of these components often are significant enough to require corrective action to ensure the desired performance. Simulations can be quite useful in providing insight into the tolerance of a design to various nonidealities, but many converters are too complex to perform a full transistor level simulation with sufficient accuracy. In these cases, behavioral simulations using sufficiently robust models can provide valuable information that would otherwise be unavailable.

When implementing A/D converters in circuitry, the converters' components, such as sample-and-holds, internal D/A converters, residue amplifiers, and comparators, generally do not operate exactly as they were ideally intended. Instead, there are several nonidealities which arise in their performance, such as offsets, gain errors, or nonlinearities. Several A/D converter architectures have been developed which can tolerate many of these problems and still maintain the desired level of resolution. For example, self-calibrating charge redistribution A/D converters were developed in order to overcome the nonlinearity introduced by mismatch in the internal D/A converter [1]. Other techniques have been developed to deal with problems such as offsets and gain errors in comparators and residue amplifiers [2], [3]. However, very few architectures can accommodate significant levels of nonlinearity in components such as the S/H or a residue or buffer amplifier. Therefore, most converters have required these components to have nonlinearity error at or below the level of resolution desired from the converter.

While this requirement may not be a problem at low resolution, the design of these components becomes more difficult in a high precision converter. Although high precision components can be built, they often exhibit a much slower speed performance than less accurate designs. This comes from a speed versus precision trade-off that is evident in most analog circuit designs. Typically, low precision circuitry can be built with high speed, but high precision designs often result in lower speed performance. This carries over into the design of A/D converters, such that higher resolution converters yield lower conversion rates than lower resolution converters. Although some existing architectures have managed to avoid needing high precision circuitry [4]-[6], they are still not particularly well suited for high speed conversion. This is partly why they are rarely used at low or moderate resolution. Clearly, a high resolution A/D converter architecture that could tolerate the nonidealities associated with lower precision circuitry would be attractive for its potential for higher conversion speed.

In order to increase the speed potential of high resolution A/D converters, techniques were developed for nonlinearity correction, which enable a converter to tolerate not only offsets and gain errors but also nonlinearity errors in several converter components. Although some high precision components are still required to maintain high resolution, the speed performance of the converter has been decoupled from the speed of these components, so that conversion speed is determined instead by the speed of low precision circuitry in the main path of the converter.

The nonlinearity correction works by forming a piecewise-linear (PWL) approximation to the transfer curves of various components and calibrating each region. This is implemented by matching the output characteristic of a D/A converter to an amplifier output curve over a small range of output. The length of the PWL segments is determined by the amplifier nonlinearity and by the D/A output nonlinearity. If the amplifier output curves too much or the D/A output is too nonlinear, the deviation in the approximation can be too large, meaning that the PWL segments must be shortened until the deviation is acceptable. The use of this correction depends on the amplifier output characteristic being smoothly varying or with major discontinuities only at the PWL segment endpoints. High resolution is maintained by adjusting the offsets and slopes of the PWL segments during a calibration process.

The application of these techniques to a sample 16 bit converter is shown in figure 1. While a parallel or pipelined architecture would have more potential for high speed, a successive approximation topology was chosen for its simplicity to demonstrate the nonlinearity correction. During conversion, the analog input is sampled by the S/H and applied to the input of a residue amplifier. The top M bits are converted using the estimation D/A, the offset D/A and the comparator in a standard binary search. The estimation D/A is used to give a rough estimate of the analog signal to be subtracted from the sampled input at each cycle, and the offset D/A subtracts off a finer calibrated value before the bit decision by the comparator. The same successive approximation codes which are fed to the estimation D/A are also used to address RAM A, which stores the calibrated inputs to the offset D/A. The use of the estimation D/A reduces the necessary range of the offset D/A and thus the memory size required in RAM A, and the amplifier reduces the noise sensitivity of the circuitry past it. After the top M bits are determined, they are used to address RAM B, which applies a code to the reference D/A to adjust the slope of a multiplying D/A (MD/A) by altering its reference input. The lower N-M bits are then converted using the MD/A and the comparator. This effectively divides the input region up into 2^M PWL segments, each with length of 2^{N-M} LSBs.

Calibration is performed by applying precise inputs from the calibration D/A corresponding to the endpoints of the PWL segments, which fall on transition points of the top M bits. For each calibration input code $D_{CD/A} = n2^{N-M}$, $n \in \{0, 2^M-1\}$, the estimation D/A input is set to $D_{ED/A} = n2^{N-M}$ and a binary search is performed using the offset D/A input and the comparator. The resulting offset D/A input is then stored in RAM A at address n. The slope calibrations require the application of codes $D_{CD/A} = n2^{N-M}$, $n \in \{1, 2^M\}$, to the calibration D/A and sampling its output. For each code $D_{CD/A} = n2^{N-M}$, the estimation D/A input is set to $D_{ED/A} = (n-1)2^{N-M}$ and the offset D/A input is set to the calibration code stored at address (n-1) in RAM A. The MD/A input is set to 2^M by taking its bits high and adding one extra LSB to its output, and a binary search is performed on the reference D/A input using the comparator. The resulting reference D/A input code is then stored in RAM B in location (n-1).

The resulting converter is tolerant to comparator offset and static offsets, gain errors, and nonlinearities in the S/H and residue amplifier. In addition, the estimation D/A, offset D/A, and reference D/A do not require high linearity but only fine adjustability at their output. This is easily attainable by using redundancy in their design [7], which requires the use of extra bits to cover the same range of output. The linearity

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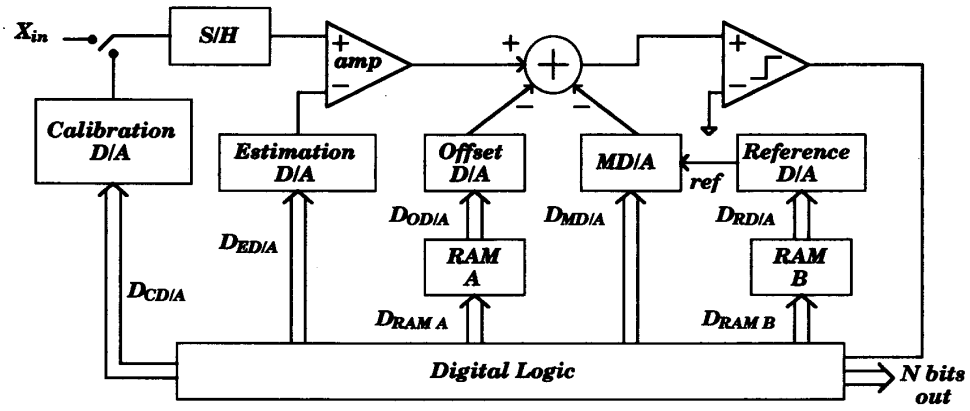


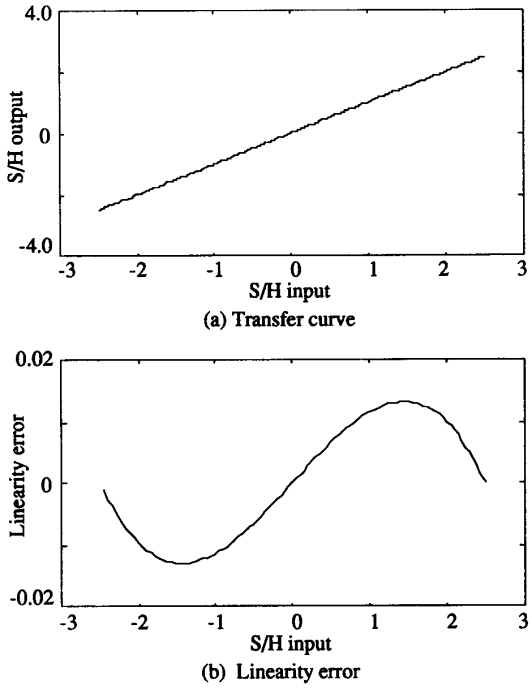
Figure 1. Sample successive approximation A/D converter architecture using nonlinearity correction

requirements on the MD/A are also relaxed, with approximately N-M+1 bit linearity needed. The converter has an attractive feature in that circuit precision in most of the components can be traded for calibration memory. For example, if the residue amplifier or MD/A nonlinearity is too large and would reduce converter resolution, then the number of PWL segments can be increased until the desired resolution is attainable. Similarly, if mismatch in the D/A converters is expected to be too severe, then more redundancy can be designed in the converters to preserve adequate adjustability at their outputs. The cost of these modifications is increased memory requirements, whether through more calibration addresses needed for more segments or through more bits needed at each point for the extra redundancy. The calibration D/A is the only component which requires high precision that cannot be traded for memory. However, since the speed of this D/A does not limit the conversion speed, its design can focus instead on attaining the necessary high precision without concern for speed.

The converter shown in figure 1 was simulated behaviorally using Saber [8], and several nonidealities were modeled, including S/H and residue amplifier offset, gain error, and nonlinearity, comparator offset, and mismatch in the offset D/A, estimation D/A, reference D/A, and MD/A. The error associated with the calibration D/A was the only main error source that was not modeled, since it's effect on converter performance was fairly obvious. The PWL approximation was formed by dividing the input region into 1024 segments, requiring 1024 offset and 1024 slope calibrations. The S/H was modeled with 7 bit linearity over the [-2.5, +2.5] input range, and its transfer curve and linearity error are shown in figure 2. Similarly, figure 3 shows the transfer function and linearity error from X_{in} to the residue amplifier output with the estimation D/A output set to zero. The combined amplifier and S/H characteristic had linearity error of approximately ±20 LSBs over the range $X_{in} \in \{-0.1, 0.1\}$, but the error over each PWL segment was within ±1/10 LSB. Six bit converters were used for the estimation D/A and MD/A, each of which had 7 bit accuracy. The differential and integral nonlinearities of the simulated MD/A are shown in figure 4. The offset and reference D/As were constructed using 7 bit accuracy internally, and extra bits were included for redundancy to ensure sufficient adjustability. The 18 bit offset D/A covered a range of ±2048 LSBs, with 1/16 LSB adjustability and two bits used for redundancy. The 10 bit reference D/A used one bit for redundancy and had a range of ±32 LSBs with 1/8 LSB adjustability.

Using Saber, the converter was first fully calibrated in simulation, which required approximately 30 hours of simulation time on a Sun 3/260 and 28.7kbits of simulated RAM to hold the calibration data. The accuracy of the calibrated converter can be evaluated by determining the input level for every digital output code's switching point. This can be achieved by sweeping the converter input in fractions of an LSB and noting when the digital output code changes state. However, using only 1/8 LSB resolution in this evaluation was estimated to require approximately one year of simulation time on the same platform. Therefore, the input signal was instead swept in 1/8 LSB increments over short ranges of 25 LSBs at several points along the overall A/D input range. From this data, the differential and integral nonlinearities were computed and are displayed in figure 5. The integral nonlinearity plots were calculated using the same ideal straight line approximation for each case rather than one optimized for each short range.

Due to mismatch in the internal D/A converter, most successive approximation converters experience their worst errors at major bit transitions [9]. However, because of the calibration at each of these major bit transitions, the errors at those points are reduced, as can be seen



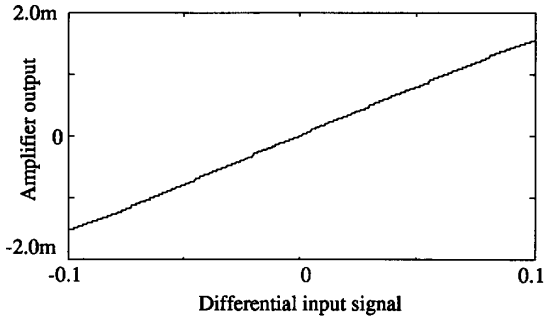
(a) Transfer curve

(b) Linearity error

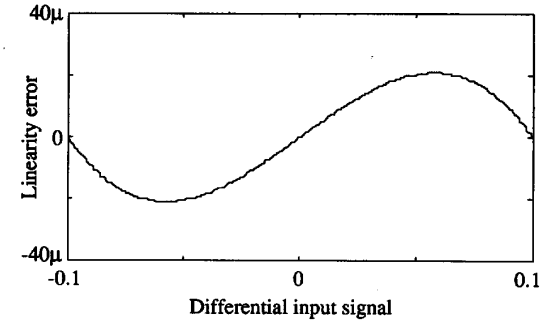
Figure 2. Simulated sample-and-hold characteristics

in figure 5(c) and (d) at code 32768 (the MSB transition point). The maximum errors in this converter tend to occur instead at points where the MD/A has its maximum error, which can be seen in figure 4 to be at the 1/4, 1/2, and 3/4 full scale points. These errors correspond to the error in code 5(e) and (f) at code 32799, where the MD/A is at 1/2 full scale. Similarly, the MD/A is at 3/4 full scale when the maximum error occurs in figure 5(g) and (h). However, if the rest of the converter range is assumed to be no worse than these small segments, then overall converter nonlinearity falls within ±0.4 LSBs. A mathematically derived error budget for the converter predicted a similar maximum error of ±0.48 LSBs using the level of nonidealities included in the simulation models.

The ability to behaviorally simulate a complex system like this A/D converter is extremely useful for identifying the effects of various nonidealities on system performance. In many cases, a system this size could not be realistically simulated using conventional circuit simulators. In the case of a top-down design process, the transistor level circuitry may not even exist yet, so this capability allows exploration of the system performance before the time and energy is expended on the low level circuit design. Although a mathematical analysis was able to be performed on this converter architecture, in many situations this would be intractable. Then this behavioral simulation capability becomes an invaluable tool in helping to assure a successful design. However, an important issue that remains crucial to the validity of the simulations is the accuracy and robustness of the models used. All critical parameters of the components included must be modeled sufficiently, which can be difficult to ensure.

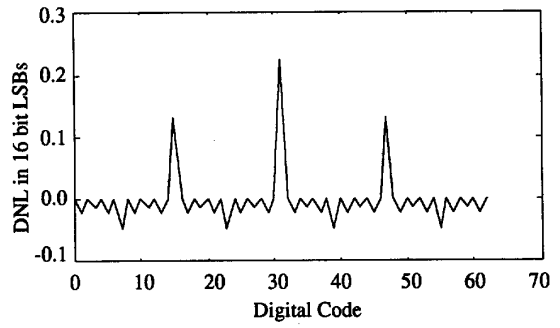


(a) Transfer curve

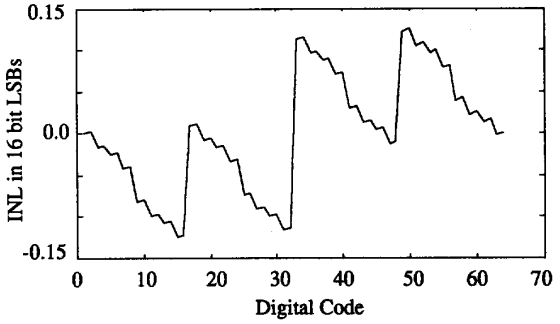


(b) Linearity error

Figure 3. Simulated amplifier characteristics



(a) Differential nonlinearity



(b) Integral nonlinearity

Figure 4. Simulated MD/A nonlinearity characteristics

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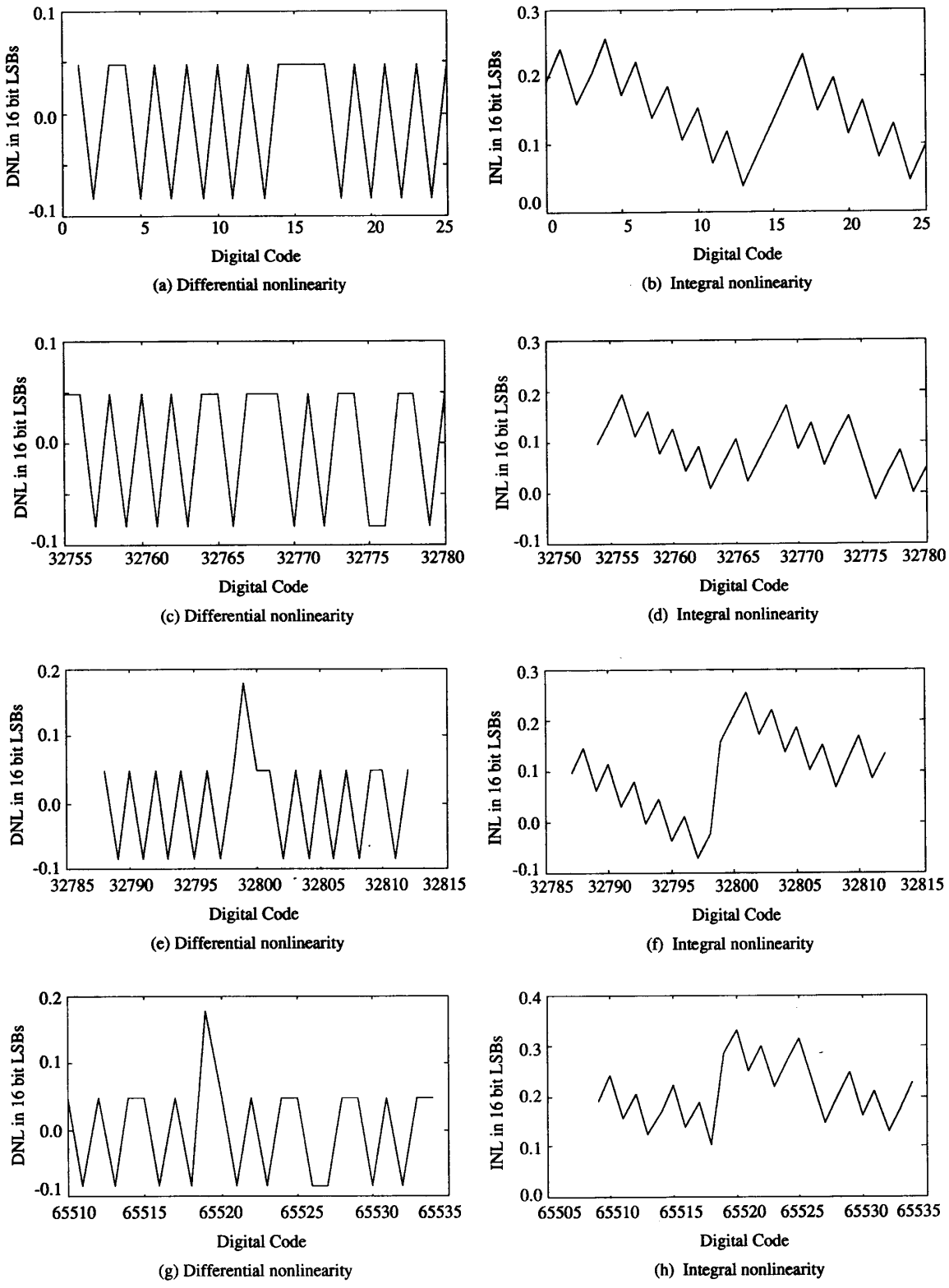

(a) Differential nonlinearity

(b) Integral nonlinearity

(c) Differential nonlinearity

(d) Integral nonlinearity

(e) Differential nonlinearity

(f) Integral nonlinearity

(g) Differential nonlinearity

(h) Integral nonlinearity

Figure 5. Nonlinearities of simulated 16 bit converter after calibration