Solution of Massively Parallel Systems of Nonlinear Equations Using Analog Circuits

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Abstract

A parallel analog computing scheme is presented which finds solutions to very large sets of coupled equations using a massively parallel analog computing structure. The viability of the proposed scheme, is demonstrated by solving the power flow (load flow) equations for a power system. The proposed scheme will solve the power flow equations for a large system at least four orders of magnitude faster than digital computers currently being used by utilities. The added speed will make the solution of the power flow equations a viable method of determining power system stability online in utility control centers. The proposed parallel analog architecture will employ intergrators, multipliers, and feedback to find the solution of the nonlinear, algebraic power flow equations as the the steady state solution of a dynamical analog circuit.

1 Introduction

Because of their size and complexity, power systems have always been a prime candidate for computer based analysis and simulation [1, 2]. One of the fundamental analysis and planning tool used by power utilities is the solution of the power flow equations. The power flow, or load flow, equations are a set of nonlinear algebraic equations whose solution represents the steady state operating point of the system [3]. The power flow equations are coupled, nonlinear, and of high order. For a power system with n buses there will be $2n-2$ equations. The traditional method of solving the power flow equations is by an iterative search technique, such as Gauss-Seidel or Newton-Raphson. Currently, utilities solve these equations on work stations. For a typical power system with 2500 buses and 4000 lines, the solution requires about 15-30 cpu seconds. In a planning environment, where the analyst is looking for solutions to future needs of the utility, the time of solution is not a primary concern. However, the power flow solution is also of use to power system operators, the personnel who actually operate the system on a minute to minute basis. For system operators the power flow would be most useful if the solution can be done in a matter of milliseconds, rather than tens or hundred of seconds as is currently the case with digital computers.

If the power flow could be solved in milliseconds, then the system operator could very quickly investigate how the system will react to a set of potential problems or disturbances, called 'contingencies.' [4]. If the system is stable for most of the contingencies, then the operator feels confident that the system is operating in a satisfactory fashion.

In this paper we will show that the power flow equations can be rewritten so that they can be solved in parallel using a combination of analog and digital circuitry. The emphasis will be on the analog portion of the proposed hardware, but it is worth emphasizing that the overall approach is a hybrid technology that provides the necessary flexibility to model any power system topology. In particular, this mean the flexibility to reconfigure the busses and lines of the power system arbitrarily and to adjust all system parameters and variables such as line impedances and real and reactive generation and load. In short, the proposed computing technology will have the same capabilities as current digital systems.

The clear advantage of the proposed approach is that it will be many times faster than current single digital, or even parallel, digital computer systems. The reason is that the power flow equations are solved *totally* in parallel. Thus, no matter what the size of the power system, the solution time will be essentially the same. Even a parallel digital computing system cannot offer this level of parallelism.

The success of this approach, as demonstrated by both SPICE [16] simulations and an actual realization of the circuitry using discrete components, results from the following properties of the power flow equations. First, the dynamic range of the power system problem matches that of current analog circuitry. Second, it is possible to realize the power flow equations in terms of mathematical operations than can be done quickly with minimum analog circuitry. Basically, this means writing the power flow equations in Cartesian coordinates instead of the usual polar coordinates, thereby eliminating the evaluation of sine and cosine functions, operations that cannot be done efficiently with analog circuits. In Cartesian coordiates the power flow equations can be evaluated using only summing and multiplying operations that can be realized with simple, analog circuits that do not require much space on an integrated circuit. As an example of analog circuit density, Intel currently offers a single chip with 10,240 analog six bit precision multipliers [13].

It should be emphasized that even though the solution is achieved by the analog part of the system, the initial configuration of the topology, the setting of all system parameters and variables and the retrieval of the solution is done digitally. In a typical scenario a 'case,' consisting of a topology, the system parameters and known variables would be retrieved from the memory of a digital computer and used to initialize the analog circuitry. The analog circuitry would then solve the power flow; the solution would be retrieved by the digital computer.

The analog scheme is the source of the potential increases in speed, and is the main topic of this paper. Three main issues will be addressed: stability, accuracy, and speed. The primary concern is stability. The analog circuit which will be used to solve the power flow equations finds a solution through the application of analog feedback [14]. That is, we create an analog dynamical system whose steady state solutions are the solution of the power flow equations. Although we can easily guarentee that the critical points of such a circuit are solutions to the power flow equations, it is not assured that these solution points are stable equilibrium points of the analog circuit. This is because some of the solution points may be unstable equilibria.

Due to the particular architecture employed, the proof of stability of the analog circuit remains an open issue, currently being studied. However, as pointed out in the sequel, extensive testing has shown the analog circuit to be remarkably stable. A more practical and important aspect of stability, is the introduction of circuit parasitics when the circuit is actually fabricated. As discussed later, this issue has been addressed by building a prototype circuit using discrete components.

Also of concern is the accuracy of the individual processors. Accuracy will be limited mostly by the quality of the multipliers, which form the heart of the circuit topologies employed. Current technology realizes analog multipliers with accuracies of 0.3% and bandwidths of 30 Mhz in 100 square microns of chip area. For our purposes, fifty multipliers with adequate accuracy may be easily realized on a single chip. While superior performance could be obtained with bipolar circuitry, CMOS technology was used to take advantage of the cheaper price and lower power consumption.

2 Parallel Analog Solution of the power flow Equations

The power flow equations are a set of algebraic equations that balance the power consumed by known loads and transmission line losses against the power produced by the generators.

These algebraic equations are determined by the toplogy of the power system network, that is the transmission lines and transformers that interconnect the loads and generators, through a collection of nodes, or busses, and six quantities at each bus k. The six quantities are: real and reactive load, PL_k and QL_k; real and reactive generation, PG_k and QG_j; and the bus voltage magnitude and angle, $|V_k|$ and θ_k. Of the six quantities, four are specified and two are left unspecified, and for an n-bus power system there will be $2n-2$ load flow equations, since the the voltage angles at the buses are all referenced to one bus, called the *slack* [5, 3].

Of the six quantities at each bus, PG_k, PL_k, and QL_k are always known, or specified. Of the three remaining quantities θ_k is always treated as an unknown. If QG_k is specified, then the bus is called a PQ-bus and the solution of the load flow equations yields the $|V_i|$ and θ_i. If, $|V|_k$ is specified, than the bus is called a PV-bus and the solution yields PQ_k and θ_k.

As we remarked in the introduction, the power flow equations have traditionally been solved on a digital computer using some iterative search technique. There have been a number of advances in the algorithms used on digital machines. Of particular importance has been the work on so-called fast decoupled power flows [6, 7], and sparsity techniques [8, 9, 10]. However, this work is mainly a refinement of previous iterative techniques. Further, the fast decoupled algorithm can experience convergence problems [11, 12].

Our approach is to solve these equations completely in parallel using a specialized analog circuit, that is digitally programmable so that is can accomodate changes in the power system topology, parameter values and

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variables. As stated earlier, the idea is to design a dynamical analog circuit whose steady state solutions are also the solutions of the algebraic power flow equations. The matter of constructing a circuit whose equilibrium points correspond to the solutions of a specific set of algebraic equations is straightforward. The difficulty is encountered in guaranteeing that the equilibrium points of the analog circuit are stable. That is, the dynamical equations of the analog circuit can be written as

$$\dot{x}(t) = f(x(t)), \tag{1}$$

where $x(t)$ is a vector of the states of the dynamical system, and f a vector function. Then, the equilibrium 'points' are the values of $x(t)$ for which

$$\dot{x}(t) = 0,$$

or

$$f(x(t)) = 0 \tag{2}$$

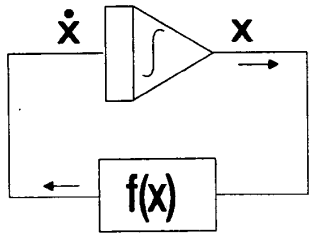

Figure 1: Implementation of $\dot{x}(t) = f(x(t))$

An implementation of equation 1 is shown in Figure 1.

The important question, of course, is whether the system in Figure 1 will converge to a stable solution. That is, given some initial state $x_0 = x(t_0)$, does $x(t) \rightarrow x_{ss}$ where x_{ss} is a constant value, i.e. an equilibrium point?

There are two basic approaches to determining the stability of a system represented by equation 1. One is to find a Lyapunov function $V(t)$ for the system, and then show that $\dot{V}(t) \leq 0$ [15]. If the stability points are known, a second approach is to linearize the system about a stability point and look at the stability of the resulting linear system. Initially, we studied the stability properties of the dynamical system that solves some low order power flow equations, where it is feasible to do eigenvalue analysis, and the results uniformly confirm that the system is stable. More recently we have shown that the dynamic equation for the circuit can be written

$$\dot{x} = Ax + N(x), \tag{3}$$

where A is a constant matrix whose entries can be written explicitly in terms of circuit parameters and N is a nonlinear term. The goal is to show that by proper choice of circuit values, the circuit is locally stable about any viable power flow solution.

3 Application to the Solution of the power flow Equations

We have already discussed the general form of the power flow equations. We now discuss in more detail two specific power systems of low order. Figures 2 and 3 represent, respectively, the topologies of two and fourteen bus power systems.

We include the diagram of the fourteen bus system, because we will subsequently present simulation results for this system. For an n-bus power system, we choose the slack bus to be bus n. We first decompose the complex current $I_{k\ell}$ flowing bewteen busses k and ℓ into its real and imaginary parts:

$$I_{k\ell} = \mathrm{Re}\{I_{k\ell}\} + j\mathrm{Im}\{I_{k\ell}\}, \tag{4}$$

where Re{ } and Im{ } signify the real and imaginary part of $I_{k\ell}$. Then the real and imaginary parts of the current in the line can be expressed in terms of the conductance $g_{k\ell}$ and susceptance $b_{k\ell}$ of the line as follows.

$$\mathrm{Re}\{I\} = -g_{k\ell}(\mathrm{Re}\{V_2\} - \mathrm{Re}\{V_1\}) + b_{k\ell}(\mathrm{Im}\{V_2\} - \mathrm{Im}\{V_1\}) \tag{5}$$

and

$$\mathrm{Im}\{I_{12}\} = -b_{k\ell}(\mathrm{Re}\{V_2\} - \mathrm{Re}\{V_1\})) - g_{k\ell}(\mathrm{Im}\{V_2\} - \mathrm{Im}\{V_1\}) \tag{6}$$

The voltage at bus ℓ is given by:

$$V_\ell = \mathrm{Re}\{V_\ell\} + j\mathrm{Im}\{V_\ell\} \tag{7}$$

The complex power at Bus ℓ, S_ℓ, can then be written

$$\mathrm{Re}\{S_\ell\} = \mathrm{Re}\{V_\ell\}\left[\sum_{\substack{k=1\\k\neq\ell}}^{n-1} \mathrm{Re}\{I_{k\ell}\}\right] + \mathrm{Im}\{V_\ell\}\left[\sum_{\substack{k=1\\k\neq\ell}}^{n-1} \mathrm{Im}\{I_{k\ell}\}\right] \tag{8}$$

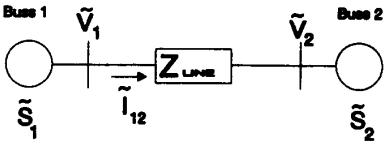

Figure 2: Two Bus Power System

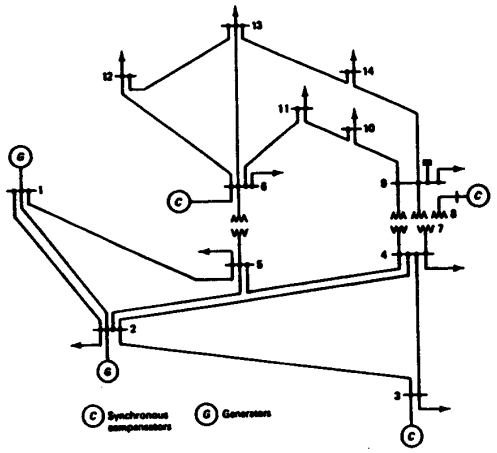

Figure 3: Fourteen Bus Power System

and

$$\mathrm{Im}\{S_\ell\} = \mathrm{Im}\{V_\ell\}\left[\sum_{\substack{k=1\\k\neq\ell}}^{n-1} \mathrm{Re}\{I_{k\ell}\}\right] - \mathrm{Re}\{V_\ell\}\left[\sum_{\substack{k=1\\k\neq\ell}}^{n-1} \mathrm{Im}\{I_{k\ell}\}\right] \tag{9}$$

As noted before, the voltage at the slack bus is taken to be $1\angle 0°$.

Equations 8 and 9 constitute a set of $2n-2$ real equations in $2n-2$ unknowns. As noted earlier, the choice of fixed and free variables at each bus can vary, but we always have exactly $2n-2$ free, or unknown variables.

4 Experimental Results

We present simulation results for the IEEE 14–Bus system. A circuit to solve this system has been simulated on SPICE to demonstrate the stability of the proposed architecture when modeling a large system. This simulation has been used to demonstrate that for any reasonable starting point, the parallel analog computer will be stable, and will find an accurate solution. In constructing the SPICE simulation, we used 'bus' and 'line' sub-circuits that allow the topology to be reconfigured as desired by the user. This choice also makes it possible to accomodate off-nominal tap transformers that may appear in the network.

Figure 4 shows the results of a simulation in which the initial values of $\mathrm{Re}\{V_\ell\}$ and $\mathrm{Im}\{V_\ell\}$, $\ell = 1 \ldots 14$, were set to 1 and 0, respectively. Figure 4(a) and (b) show the real and imaginary parts of the fourteen bus voltages. Figure 4(c) shows the error currents being integrated by the analog circuit. As can be seen, these error currents all approach zero when the solution is found, indicating that the solution of the SPICE simulations are equal to the solutions computed by conventional power flow methods.

5 Parasitic Considerations

Having demonstrated the stability of the circuit empirically, it remains to show that parasitics in the fabricated circuit will not lead to instability. For this reason, a dedicated hardware implementation of the two bus system was

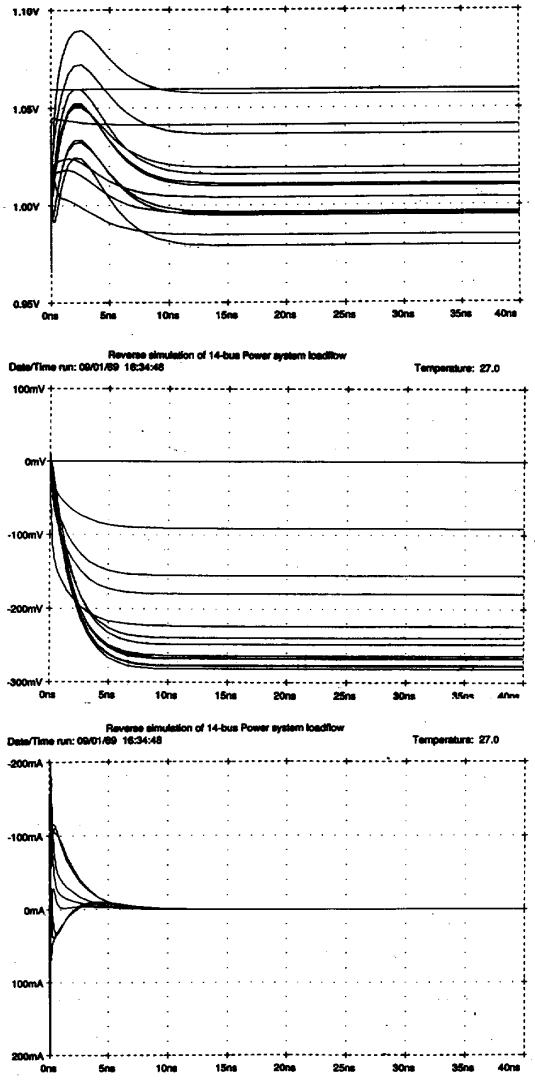

Figure 4: Results for SPICE Simulation of IEEE 14-Bus System (a) Real Voltages (b) Imaginary Voltages (c) Error Currents

built using discrete components to determine the effect of parasitic elements on the performance of the parallel computer. The actual multipliers employed were manufactured by Burr-Brown (MPY534). The stated precision of these devices is $\pm 0.25\%$ maximum error.

In the implementation, the errors are limited to local feedback loops and show up as an error in the local computed bus power. It is estimated that the parasitic capacitances of the prototype circuit were two orders of magnitude smaller than the actual circuit elements used in the implementation. The parasitic resistances in the circuit were too small to measure.

The results obtained for the implementation are validated by accompanying SPICE simulations of each test. As a first step, a static solution was run, to demonstrate that the system would remain settled when given the correct solution initially.

Next, progressively worse inital guesses of the solutions were used to determine the system's capability to find the correct solution. The computer failed to find a solution only for cases of very bad initial guesses. It is worth noting that a conventional power flow solution executed on a digital computer will behave similarly. That is, it will not converge for very poor initial guesses.

Three progressively worst guesses, for which the system *does* converge, are shown in Figures 6, 7, and 8

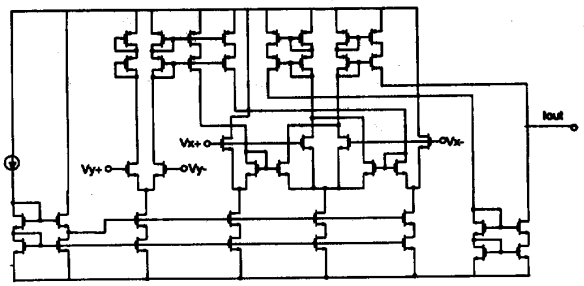

Figure 5: Schematic of Transconductance Multiplier

Note in the case of Figure 8 there is an obvious difference in implementation and simulation results due to the fact that the initial guess of the solution was very close to instability, emphasizing the small differences between the dynamics in the hardware and the simulated system. However, the steady state solutions are correct. The final values of the implementation and the simulation are almost exactly the same.

6 VLSI Fabrication Issues

Based on the results of the SPICE simulations and the discrete component validation, work in now underway on fabricating small, precise and sufficiently fast multipliers that will allow the topologies of large interconnected systems, such as a power system, with VLSI technology. In other words, the goal is to develop digitally reconfigurable 'chip sets' that could solve a large scale problem. Initially we will concentrate on using the multiplier to develop 'line' and 'bus' subcircuits to solve the power flow problem, but the ideas are clearly generalizable to other large scale dynamic systems.

The multiplier is based on a linear transconductance cell, and has differential inputs and a current output [17, 18]. The design differs from that in [18] in that cascaded current mirrors are used for improved current tracking. Also, cascaded current sources have been employed to allow a wider voltage swing range. Figure 5 is a schematic of the mulitplier

To achieve the necessary precision in the fabricated mulitpliers, EEPROMs will be used as pre-emphasis devices [19]. The effectiveness of this approach has been explored in [20]. The EEPROM devices make it possible to use very compact multiplier cells which otherwise would not have the necessary accurcay.

7 Conclusions

A new approach to the solution of the power flow equations has been presented that can increase the speed of solution by many orders of magnitude over current approaches. Both stability and parasitic influences involved in realizing the necessary circuitry in CMOS technology have been investigated. It has been demonstrated that the proposed method may be constructed in a manner which will be superior to existing hardware in cost, speed, and size. The development of parallel analog processors to solve systems of equations representing large scale power systems has been investigated using the IEEE 14-Bus system via SPICE simulation. The viability of the simulation is supported by test results on a dedicated hardware implementation for a two bus system. Current efforts are being focused of the construction of a dedicated CMOS circuit to perform these calculations for large scale systems.

References

[1] A.F. Glimn, G. W. Stagg, "Automatic Calculation of Load Flows," *Trans. AIEE*, vol. 78, pp. 817-828, Oct. 1957.

[2] J. E. Van Ness, "Iteration Methods for Digital Load Flow Studies," *Trans. AIEE*, vol. 78, pp. 583-588, Aug. 1959.

[3] O. I. Elgerd, *Electric Energy Systems Theory*, McGraw Hill, New York 1971.

[4] T. A. Mikolinnas, B. F. Wollenberg, "An Advanced Contingency Selection Algorithm,' *IEEE Trans. on Power Apparatus and Systems*," PAS-100, pp. 608-617, Feb. 1981.

[5] C. A. Gross, *Power System Analysis*, John Wiley & Sons, New York, 1979.

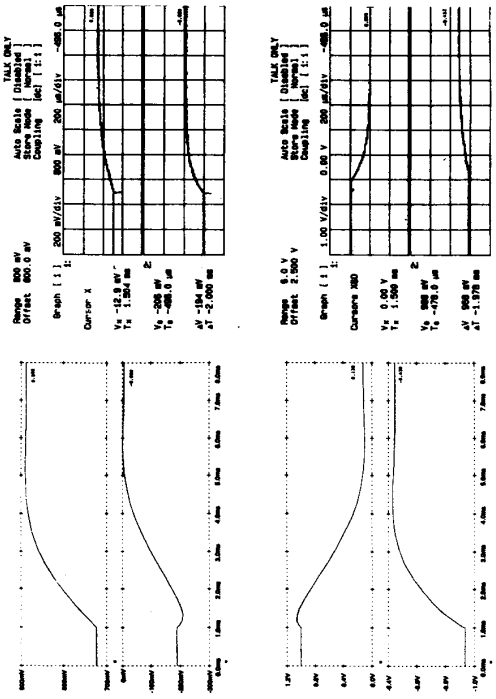

Figure 6: Results for Best Initial Guesses (a) Implementation (b) SPICE Simulations

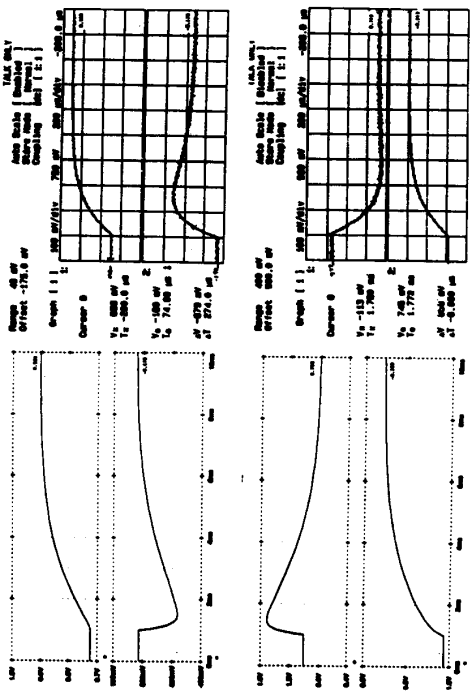

Figure 8: Results for Worst Initial Guesses (a) Implementation (b) SPICE Simulations

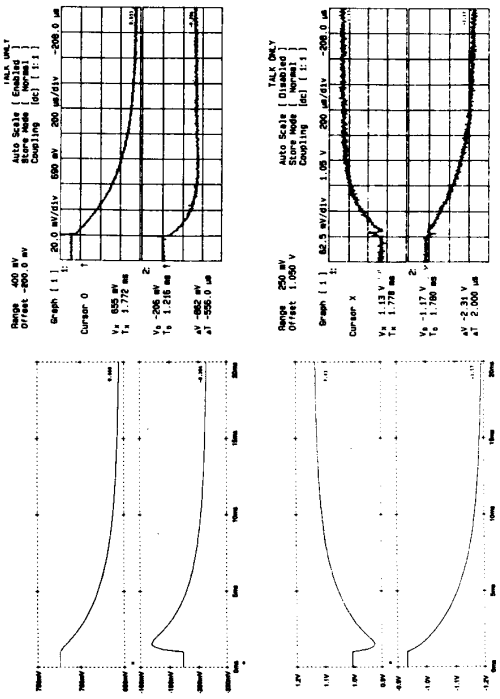

Figure 7: Results for Middle Initial Guesses (a) Implementation (b) SPICE Simulations

[10] B. Stott, O. Alsac, "An Overview of Sparse Matrix Techniques for On-line Network Applications," *Proc. IFAC Conference on Power Systems and Power Plant Control*, pp. 19-25, Beijing, 1986.

[11] F. F. Wu, "Theoretical Study of the Fast Decoupled Load Flow," *IEEE Trans. on Power Apparatus and Systems*," vol. PAS-96, no. 1, pp 268-275, Jan./Feb, 1977.

[12] J. Nanda, D.P. Kothari, S. C. Srivastava, "Some Important Observations on Fast Decoupled Load Flow Algorithms," *Proceedings IEEE*, vol. 75, no. 5, pp. 732-733, May 1987.

[13] Intel publication no. 290408-002, "80170NX Electrically Tunable Analog Neural Network," Intel Corp., June 1991.

[14] *Nonlinear Circuits Handbook*, 2nd Ed., Analaog Devices, Inc., Norwood, MA, Jan. 1976.

[15] D. W. Jordan and P. Smith, *Nonlinear Ordinary Differential Equations*, 2nd Ed., Clarendon Press, Oxford, 1987.

[16] L. W. Nagel, "SPICE2: A Computer Program to Simulate Semiconductor Circuits," Memorandum NO. M520, University of California Berekely, May 1975.

[17] Z. Wang and W. Guggenbuhl, "A Voltage-Controllable Linear MOS Transconductor Using Bias Offset Technique," *IEEE Journal of Solid-State Circuits*, vol. 25, no. 1, February 1990.

[18] Z. Wang, "A CMOS Four-Quadrant Analog Multiplier with Single-Ended Voltage Output and Improved Temperature Performance, *IEEE Journal of Solid State Circuits*, vol. 26, no. 9, September 1991.

[19] A. Thomsen and M. Brooke, "A Floating-gate MOSFET with Tunneling Injector Fabricated Using a Standard Double-polysilcon CMOS Process, *IEEE Electron Device Letters*, vol 12., no. 3, pp. 111-113, March 1991.

[20] A. Thomsen and M. Brooke, "A Programmable Piece Wise Linear Large Signal CMOS Amplifier, to appear *IEEE Journal of Solid-State Circuits.*