A NEW STRUCTURE FOR AN ANALOG DIVIDER

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A new structure for an analog divider is proposed. It allows the use of short-channel devices for high speed without loss in accuracy due to second order effects. It consists of 13 parallel modules that each approximate a division in a small region. The weighed sum of all outputs approximates a division for ratios between 1/4 and 4. The design of the modules and the complete circuit is explained.
The circuit has been fabricated in a 2 µm CMOS-technology. The accuracy is better than 10% and the maximum operating frequency is about 2 MHz.

Introduction

The key to faster analog circuits is the use of short channel devices, but for these devices second order effects become more significant. Thus usual analog circuits, that rely on device physics, become inaccurate. The new structure proposed here shows a possible solution to this dilemma. The transfer function is defined solely by geometric parameters.
The basic idea is the following: The plane of possible input values gets divided into several segments. The segments have to be chosen such that an approximation of the desired operation becomes as simple as possible. The available building blocks restrict the boundaries to be straight lines. In each segment one module approximates the operation and has a constant output outside this segment. Then the weighed sum of all neuron outputs approximates the operation over the full range of desired input values (see fig. 1).
For a divider the lines of constant ratio were chosen as segment-boundaries. These are straight lines through the origin of the plane of input values as shown in fig. 2. Each module has the following properties:
-It has an exact output at the center of its segment, its value and location are define solely by geometric parameters. This line is referred to as the decision line.
-Around this line it approximates the division. This can be understood as interpolation between two exact points, an exact approximation by a single module is not required.
-Outside the region of approximation the output of the module is constant, other modules do the approximation.

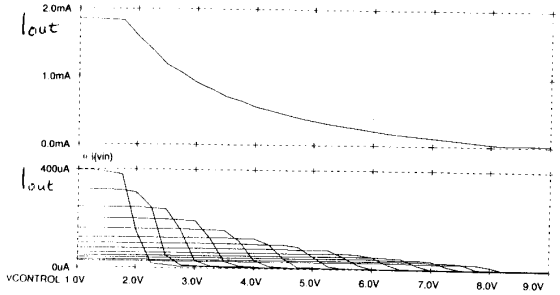

Fig. 1: The principle of operation: The transferfunction (top) is composed of the weighed sum of the comparator outputs (bottom) (Ia=10µA-Vcontrol, Ib=Vcontrol, Iout=K1*Ia/Ib+K2)

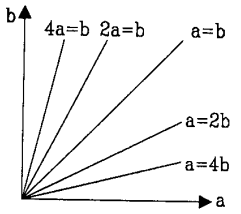

Fig. 2: The plane of input values with decision lines for various input-ratios

Circuit Building Blocks

In this parallel analog circuit three basic operations have to be performed: summation and constant multiplication at the input and output and a nonlinear function, that is similar to a sigmoid.
In this current-based design, summation is simply realized by connecting wires.
Multiplication of currents by a constant can be realized by using scaled current mirrors (see fig. 3a). For a number Win of input devices and a number Wout of output devices the relation between input and output current is

$$Iout = Wout / Win * Iin.$$

Cascoding of the output devices is necessary to increase the output resistance of the output current source. The current mirror works independent of process parameters, but relies on good matching of input and output devices.
For the divider-module a CMOS current comparator (fig 3b) and a differential transconductance amplifier (fig. 3c) are used. The small signal behavior (see 3d) of the comparator is suitable for a divider neuron: Using the Shichman-Hodges model we get

$$gdsp = \lambda p * Ip , \quad gdsn = \lambda n * In$$

where λ is the channel-length modulation coefficient, I is the large signal current and gds the small signal conductivity at the output for p and n-device respectively. At the operation point In = Ip. With a small signal variation ip

$$vout = 1 / (\lambda p + \lambda n) * ip / In.$$

The ratio ip / In determines the output voltage.
The resulting voltage is converted to a current by a differential amplifier. It has exactly no output current for V+ = V- , a linear region around V+ = V- and saturates to the positive or negative source current I for large differences. The combination of current comparator and differential amplifier (see fig. 3e) thus satisfies all requirements for a divider module, an exact output at In = Ip the approximation of a division in the vicinity of In = Ip and the constant output outside this region. The comparator with interchanged inputs serves as a voltage reference for the differential amplifier. Since the gain of

the differential amplifier can be adjusted by changing the current I, independence of process-parameters can be achieved.

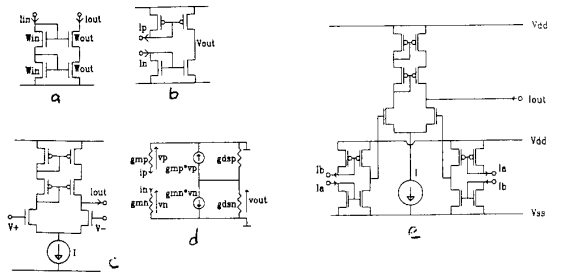

Fig. 3: circuit building blocks: a)scaled current mirror b) current comparator c) differential transconductance amplifier d) small signal model of comparator e)module for a divider: 2 comparators with interchanged inputs and a differential amplifier

The Complete Circuit

To synthesize the complete circuit, comparator decision lines have to be distributed over the desired range of valid input ratios. This is done by comparing different multiples of the input currents in different modules. The number of modules depends on the expected width of the active region of the comparator, because the divider can only work properly, if active regions are at least adjacent. Here a distribution of decision line ratios r

$r_n=2^{n/3}$, n=-6...0...6

was chosen based on a simulation of the comparator-characteristic. Furthermore, $2^{1/3}$ can be approximated within 1% by 5/4, so that scaled current mirrors are easy to implement. The width of the active region is adjustable through the current I over a wide range of process-parameters.
The weights for the output summation are determined by the upper and lower bound of the active region and are proportional to the decision line ratio r_n for the distribution chosen here.
A schematic of the complete system with 13 modules and the required constant multipliers is shown in fig. 4.

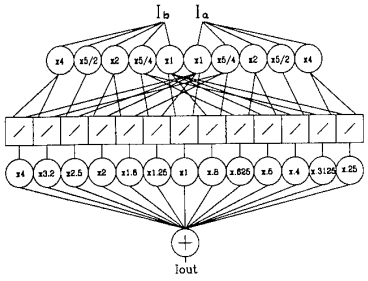

Fig. 4: schematic of the complete circuit. Squares represent modules, circles constant multipliers

Experimental Results

The circuit was fabricated in a 2µm CMOS technology. Fig. 5 shows the output current of a single module for the ideal case and from simulation and experimental results. The influence of mismatch on the experimental results is obvious, but the module is approximating a division near the decision line of the comparator.
Fig. 6 shows the output current of the complete circuit from simulation and experimental results. The relative error (see fig. 7) was calculated from comparison to a linear change of the output current between the values for input ratios of 1/4 and 4. The high errors that appear in both simulation and experimental results are due to input ratios exceeding the valid range and are thus not significant to characterize the performance.
The simulation displayed an error below 2%, whereas the experimental results show an error of about 5% with a higher error for certain inputs. This is due to threshold-mismatch in current mirrors. Mismatch leads to a shift in decision lines. It is especially significant for low input currents, which explains the high error for low Ia in the plot of the experimental results. Since no special layout techniques for reduced mismatch were used, the error is within the expectations.
The settling time of the circuit for large signal variations was measured for changes in both I_a and I_b.
The output reached 95% of its final value after about 400ns, which corresponds to a maximum operation frequency of about 2 MHz (see fig. 8).
The layout was not optimized with regard to speed and mismatch. Thus a higher speed can be achieved by changing device geometries at high capacitance nodes and a higher accuracy by improved layout.
Further improvements in speed are possible by using a faster technology such as a smaller CMOS process or a bipolar technology. This should not reduce the accuracy of the circuit due to the proposed structure.

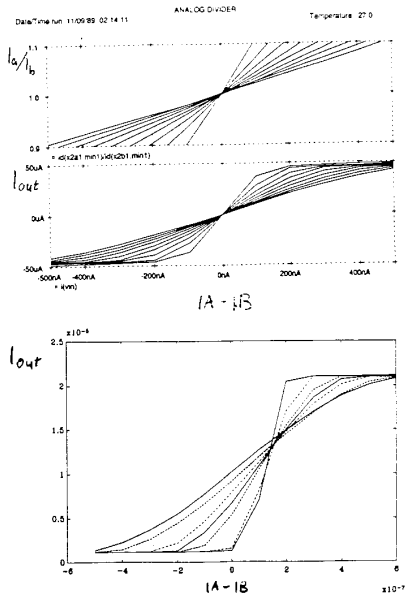

Fig. 5: output current of a single module: ideal (top), simulated (middle) , experimental (bottom)

The problem of higher accuracy is reduced to the problem of better matching of transistors. A possible solution, that has to be further investigated is the use of adjustable devices.

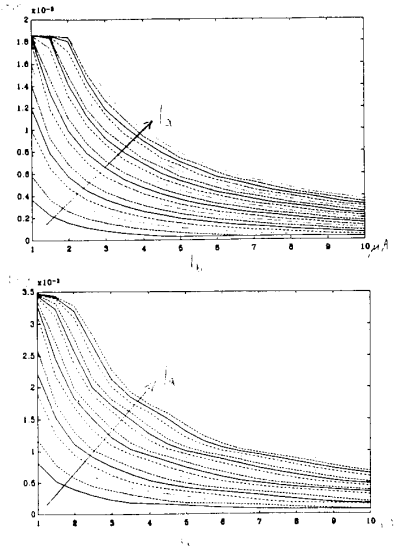

Fig. 6: Output current of the divider: simulated (top) and experimental (bottom)

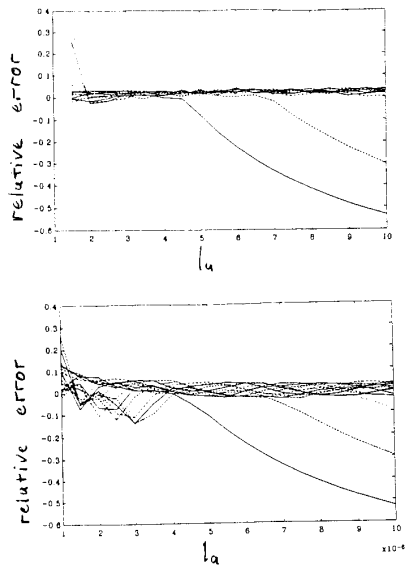

Fig. 7: relative error of the output current: simulated (top) and experimental (bottom)

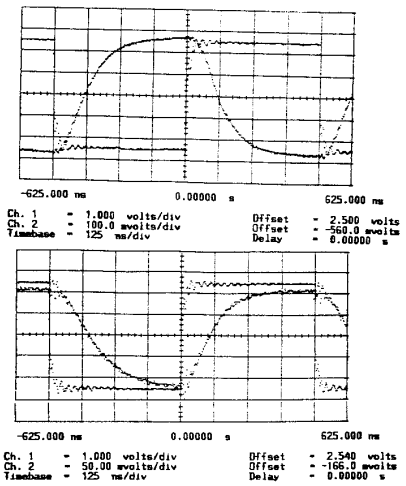

Fig. 8: step response for variations in the numerator (top) and the denominator (bottom) at 1 MHz. Settling time is about 400ns

Conclusions

A new structure for an analog divider has been proposed, implemented in a 2μm CMOS-technology and tested successfully. It operates up to a frequency of 2 MHz and displayed an error of below 10%. The main source of error is mismatch in current mirrors. The advantages of the circuit are its independence of process parameters, the use of short channel devices and thus high speed. The problem of accuracy is a problem of good matching, which might be solved by using tunable devices.