A Floating-Gate MOSFET with Tunneling Injector Fabricated Using a Standard Double-Polysilicon CMOS Process

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Abstract—**A floating-gate MOSFET, which is programmable in both directions by Fowler–Nordheim tunneling, has been fabricated using an inexpensive standard 2-μm double-polysilicon CMOS technology that is accessible for MOSIS[1] customers. Tunneling occurs at a crossover of polysilicon 1 with polysilicon 2. Device layout and basic device characteristics are presented and recommendations for efficient programming given. This is the first floating-gate FET with tunneling injector fabricated in standard technology that has close to symmetric programming characteristics for both charging and discharging of the gate.**

I. Introduction

THE floating-gate MOSFET or EEPROM has received a lot of attention for applications in analog circuits. It has been used for circuit trimming [1], [2], as weight storage in neural networks [3], and as analog memory [4]. When used for digital memory, EEPROM devices are optimized for small area, high writing speed, and low failure rate. In applications like circuit trimming, other requirements like accurate control of the floating-gate charge and good charge retention properties are important. Devices that are programmable by Fowler–Nordheim tunneling in both directions are preferred because of the exponential relation of programming voltage and current, which allows accurate programming. It is also desirable to avoid use of the drain of the transistor for programming of the floating gate. Usually the fabrication of these devices requires special processing to achieve ultrathin oxide layers [2]–[4] or textured polysilicon surfaces [5] to build tunneling injectors. For many researchers special EEPROM processes are not easily accessible or expensive. The goal of this research was to avoid special processes and build a tunneling injector in a process that is generally accessible. A previous attempt to build a tunneling injector in a standard CMOS process [1] by using field enhancement at the corners of a polysilicon slab over a diffusion region has the disadvantage of very different programming characteristics for charging and discharging of the floating gate. This resulted from relying solely on field enhancement to achieve sizable tunneling currents. The significant differences made bidirectional programming very difficult. The tunneling injector presented here has similar characteristics for charging and discharging, due to a mixture of field enhancement and a thin oxide.

II. Device Layout

The floating-gate MOSFET presented here was built in a 2-μm, p-well, double-poly process at the ORBIT-Semiconductor foundry. It consists of a minimum-geometry (W/L = 3 μm/2 μm) MOSFET, a 100-fF coupling capacitor that couples the floating gate to a control gate, and a tunneling injector (see Fig. 1). A SEM micrograph of the tunneling injector is shown in Fig. 2. The two polysilicon layers are isolated by an oxide of approximately 75 nm thickness that usually serves as a dielectric in capacitors. From Fig. 2 it can be seen that, unlike in a capacitor layout, the upper polysilicon layer overlaps the edge of the lower layer. Two significant features are visible in the SEM where the lower polysilicon slab ends: the sharp edge of the bottom polysilicon slab that causes the field enhancement, and the thinning of the oxide. A quantitative estimate of the oxide thickness from the SEM is very difficult. Experimentally, when a high voltage of more than 12 V is applied between the two polysilicon layers, bidirectional conduction occurs. Significant trap-up [7] and the asymmetry in the programming voltage indicate that field enhancement is present. The possibility of reverse programming with slightly higher voltages indicates that the oxide is thin enough to enable tunneling without field enhancement.

The device has been successfully fabricated in four different fabrication runs. Of approximately 100 devices tested, only one was defective.

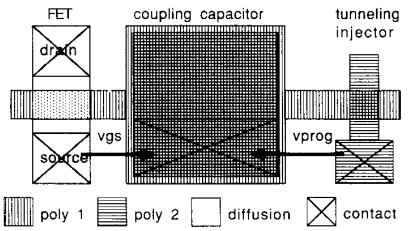

Fig. 1. Schematic drawing of the device with the connections for programming voltage v_{prog} and operating voltage v_{gs}.

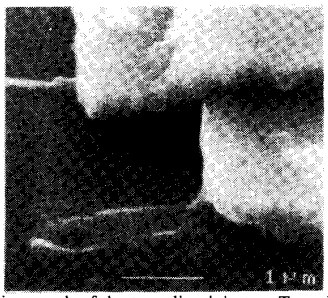

Fig. 2. SEM micrograph of the tunneling injector. Tunneling occurs at the corner of the lower polysilicon slab. The sharp edge of this slab causes field enhancement and the isolating oxide is thinned.

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TABLE I
CHARGE RETENTION MEASUREMENTS: RVTD FOR DIFFERENT BAKE TEMPERATURES AND BAKE TIMES BEFORE AND AFTER FREQUENT W/E CYCLES

Temperature [K]	423	423	423	473
Time [h]	96	192	96	96
W/E cycles	< 100	< 100	> 1000	< 100
RTVD [%]	1.7	2.6	6	12

III. CHARGE LOSS

For applications in analog circuits, the most important characteristics are the accuracy to which programming is possible and the stability of the stored value over time. The characteristic parameter measured here is the threshold voltage as seen from the control gate. Since the accuracy to which an EEPROM can be programmed for analog applications is only limited by the algorithm and the time used for programming [6], the most important accuracy limitation is the charge retention.

Charge loss was observed at two different temperatures as shown in Table I. The change in threshold voltage V_T observed was relative to the deviation of the initial threshold voltage $V_{T\,\text{start}}$ from the equilibrium threshold $V_{T\,\text{equil}}$. The value shown in the table is the relative threshold voltage drift (RTVD) given by RTVD = $(V_{T\,\text{start}} - V_T)/(V_{T\,\text{start}} - V_{T\,\text{equil}})$.

Based on these results an apparent activation energy of 1.1 eV was calculated from the Arrhenius equation. This suggests a charge loss of 0.1% in approximately 26 years. At room temperature no variation of the threshold voltage could be observed after six weeks. Due to the limited number of data points this estimate could be wrong by one order of magnitude but it is better than results for FLOTOX EEPROM's [3], probably because of the thicker insulating oxide. This suggests that EEPROM's like those presented here are preferable for applications like circuit trimming. Charge loss for aged devices has been observed after 1000 write/erase (W/E) cycles. As measurements show, the oxide becomes more leaky after frequent programming steps.

IV. WRITE-ERASE ENDURANCE

Aging of the tunneling structure after frequent write and erase procedures as, for example, during neural network training, was observed after 1000 cycles. The threshold swing for constant programming voltage was reduced due to trapped electrons in the tunneling oxide, called trap-up.

As in previous experiments, trap-up could be reduced by reducing the maximum electric field in the oxide by increasing the rise time of the programming pulse [8]. A significant reduction was observed for a rise time of 1 ms (see Fig. 3).

It should be mentioned here that trap-up is not a failure mechanism if an iterative programming procedure with variable programming voltage is used as required in most analog applications. Increased programming voltage will overcome the trap-up effect.

V. PROGRAMMING CHARACTERISTICS

The typical programming characteristics of the floating-gate FET are shown in Fig. 4. The threshold voltage was measured after the application of programming pulses of different length and amplitude, where the starting threshold was less than −4 V for positive and more than 4 V for negative programming voltages. The figure shows the exponential dependence of the threshold voltage with the programming time. This allows very accurate programming if a programming algorithm with variable programming voltage is used [6]. The programming pulse length required is significantly longer than for special-process EEPROM's, probably because of the thicker oxide in the tunneling injector.

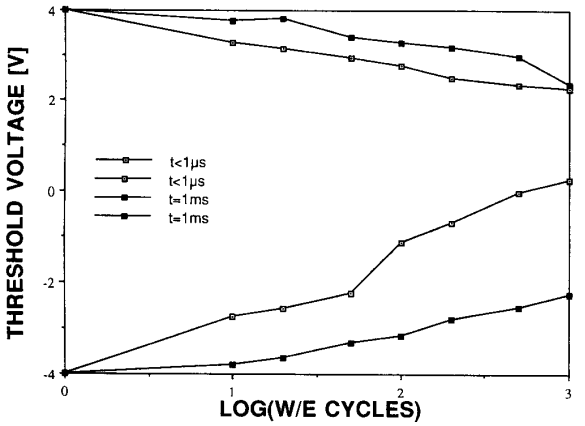

Fig. 3. Typical reduction of the threshold voltage swing after frequent write and erase cycles due to trap-up for programming pulse rise times t of less than 1 μs and 1 ms.

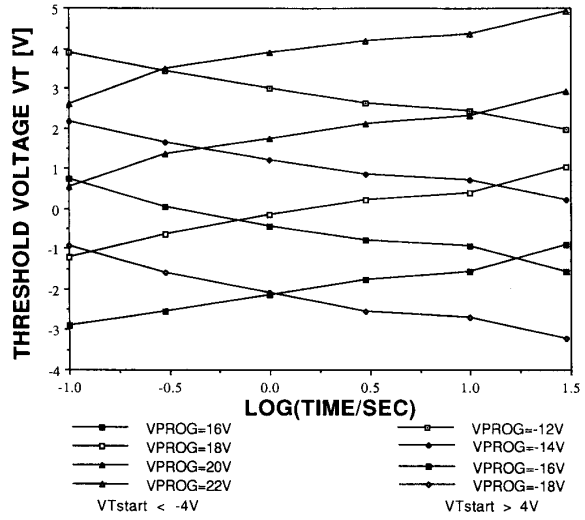

Fig. 4. Typical programming characteristics: threshold voltage V_T versus programming time for various programming voltages V_{PROG}.

The threshold voltage could be varied between −10 and +10 V without damage to the device with programming voltages of −29 and +31 V, respectively.

VI. CONCLUSION

A floating-gate MOSFET with tunneling injector was built using a standard double-polysilicon CMOS process. It is programmable in both directions with voltages above 12 V. Charge loss of 0.1% in 26 years is estimated from high-temperature measurements. The device characteristics are more suitable to analog circuits applications than digital memory. Programming with variable voltage and a slow pulse rise time is recommended. The availability of an EEPROM in this process, which has widespread and inexpensive access for MOSIS customers,

offers the opportunity for increased research for applications of EEPROM's in analog circuits.

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