4-Bit DAC

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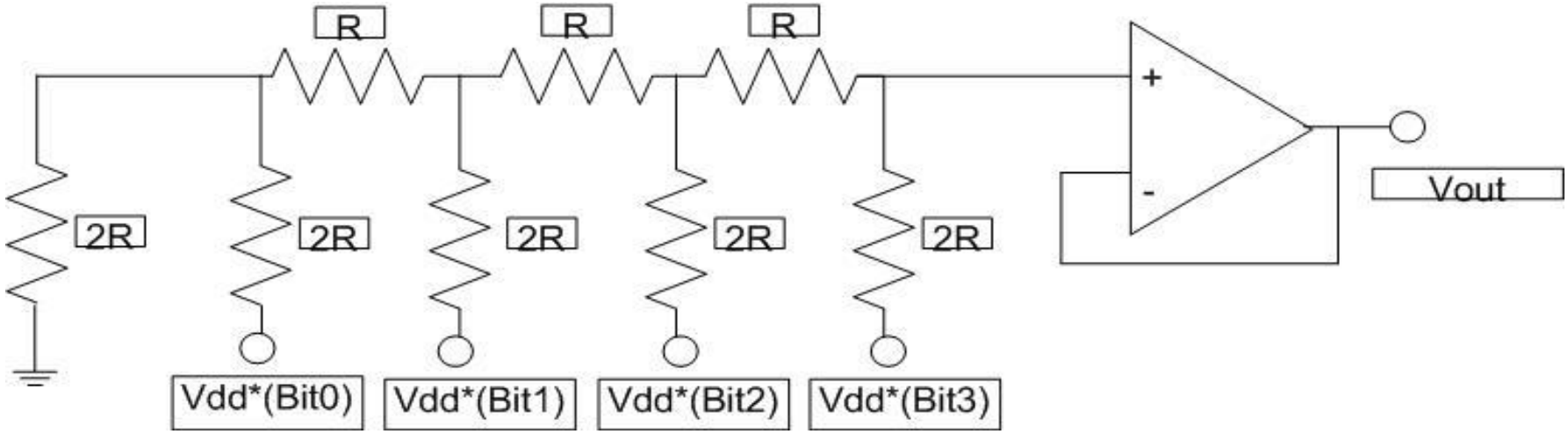
Outline

- Abstract
- Schematic
- Output
- Simulation Plan and Results
- Layout
- Final Specifications

Abstract

- The objective is to design a device that will extract an analog signal given a series of digital codes with the proper time delay.

Schematic

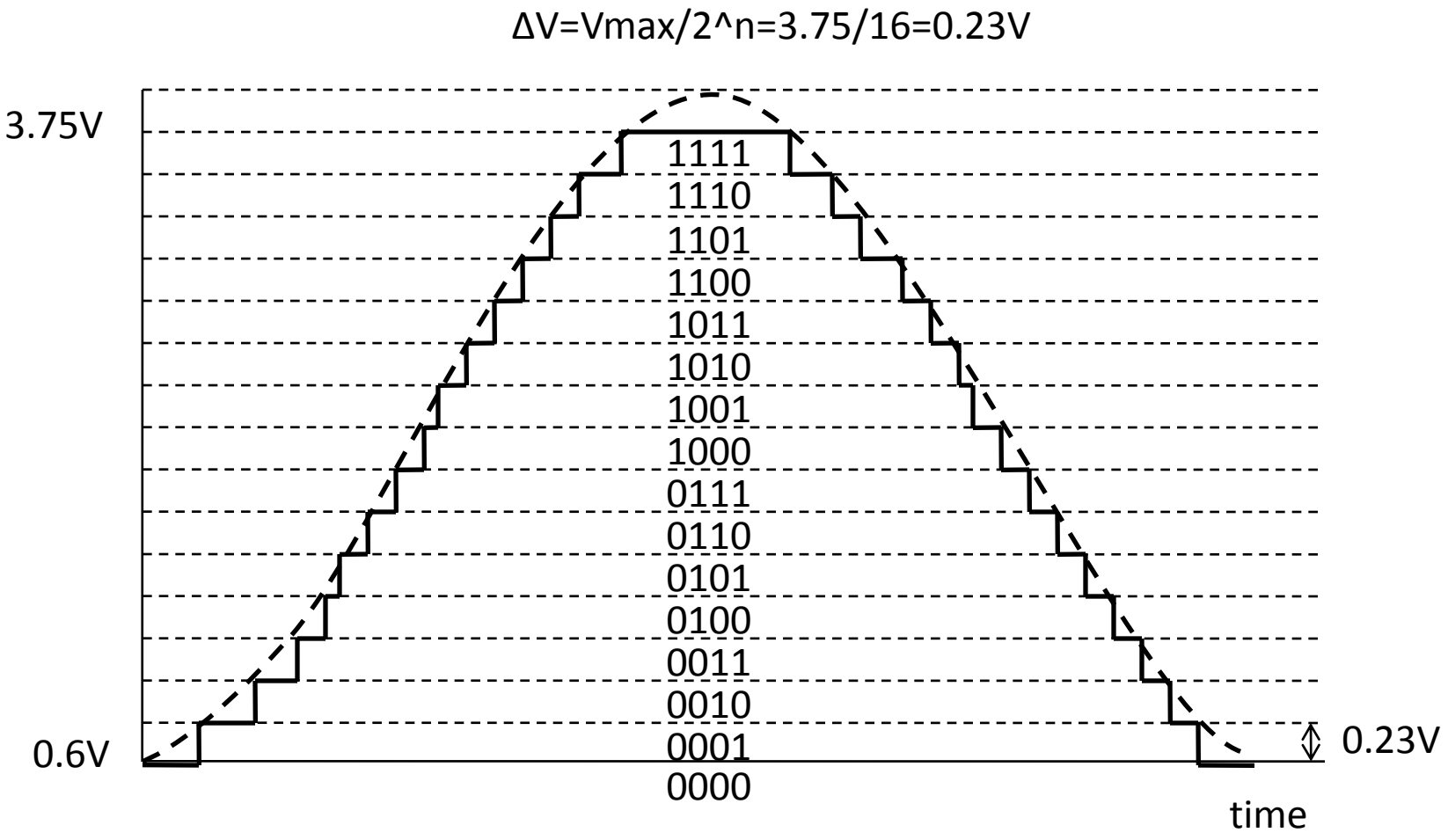


$$V_{out} = \frac{V_{dd}}{2^N}\left(Bit_{N-1}2^{N-1} + Bit_{N-2}2^{N-2} + \ldots + Bit_0 2^0\right) = \frac{V_{dd}}{16}\left(8\left(Bit_3\right) + 4\left(Bit_2\right) + 2\left(Bit_1\right) + Bit_0\right) =$$

$$V_{dd}\left(\frac{1}{2}Bit_3 + \frac{1}{4}Bit_2 + \frac{1}{8}Bit_1 + \frac{1}{16}Bit_0\right)$$

R = 8kOhm

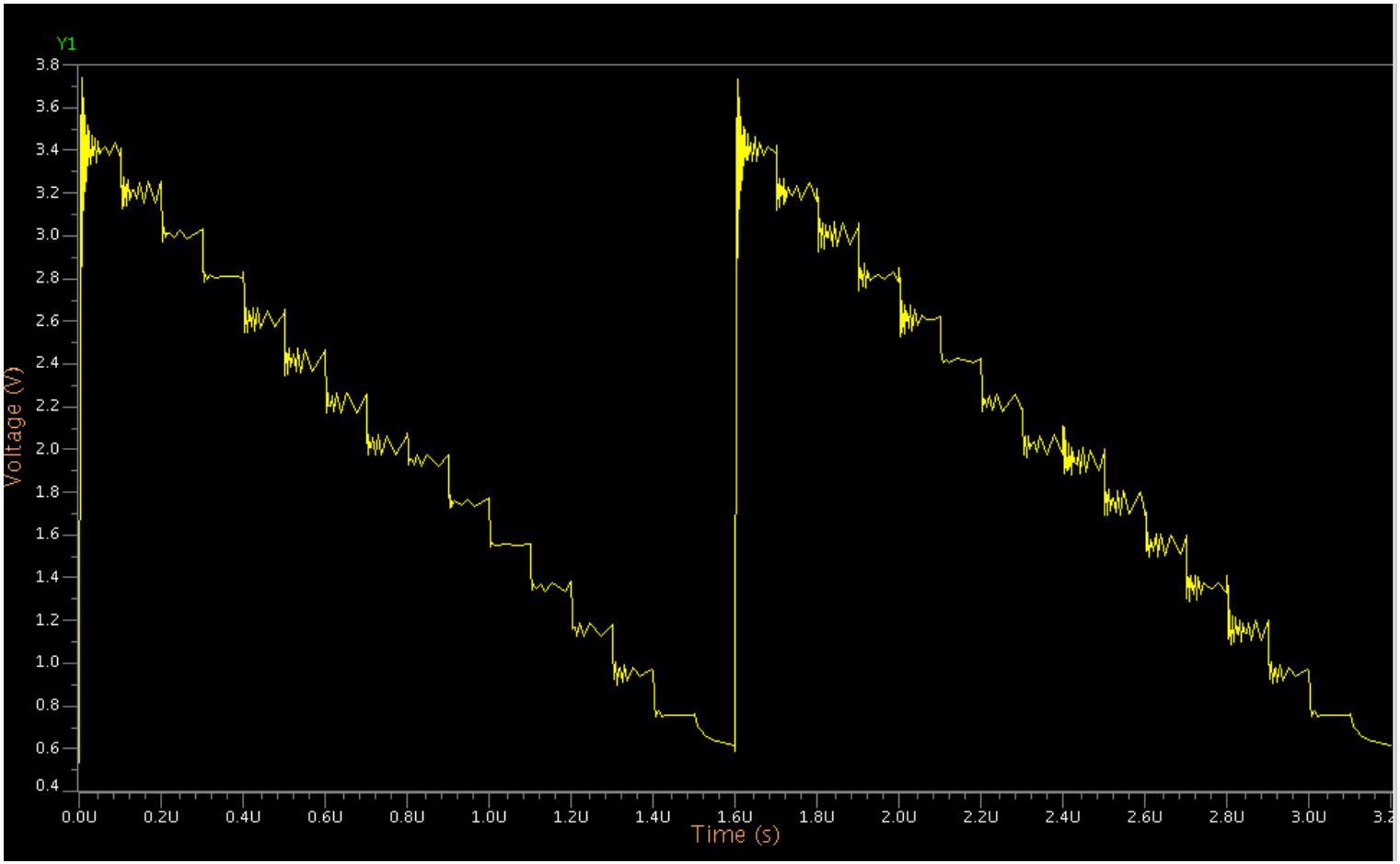
Output


ΔV=Vmax/2^n=3.75/16=0.23V
3.75V
1111
1110
1101
1100
1011
1010
1001
1000
0111
0110
0101
0100
0011
0010
0001
0000
0.6V
0.23V
time

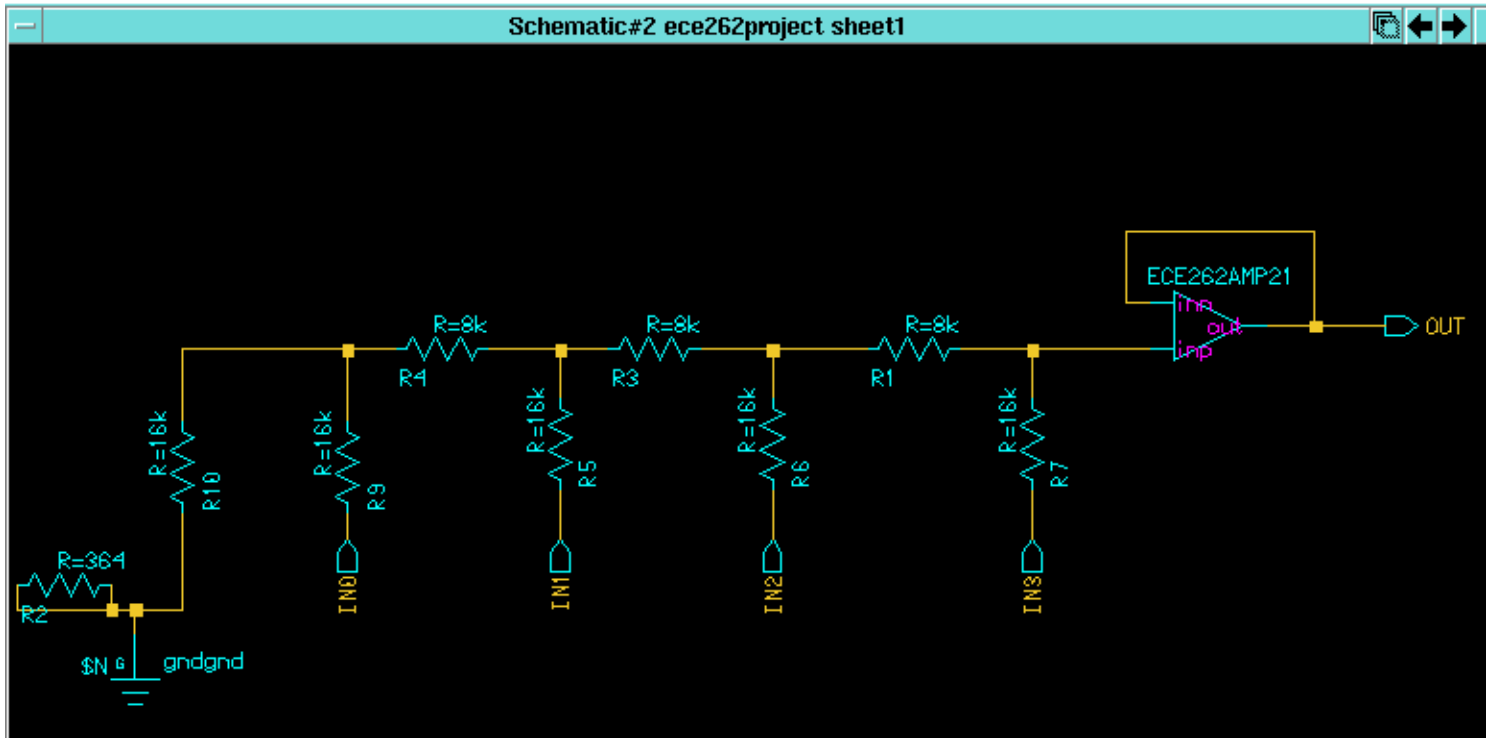
Simulation Plan

- Test the linearity
- Use pulse sources on each input to run through all possible input combinations
- Generate an approximation of a ramp function.

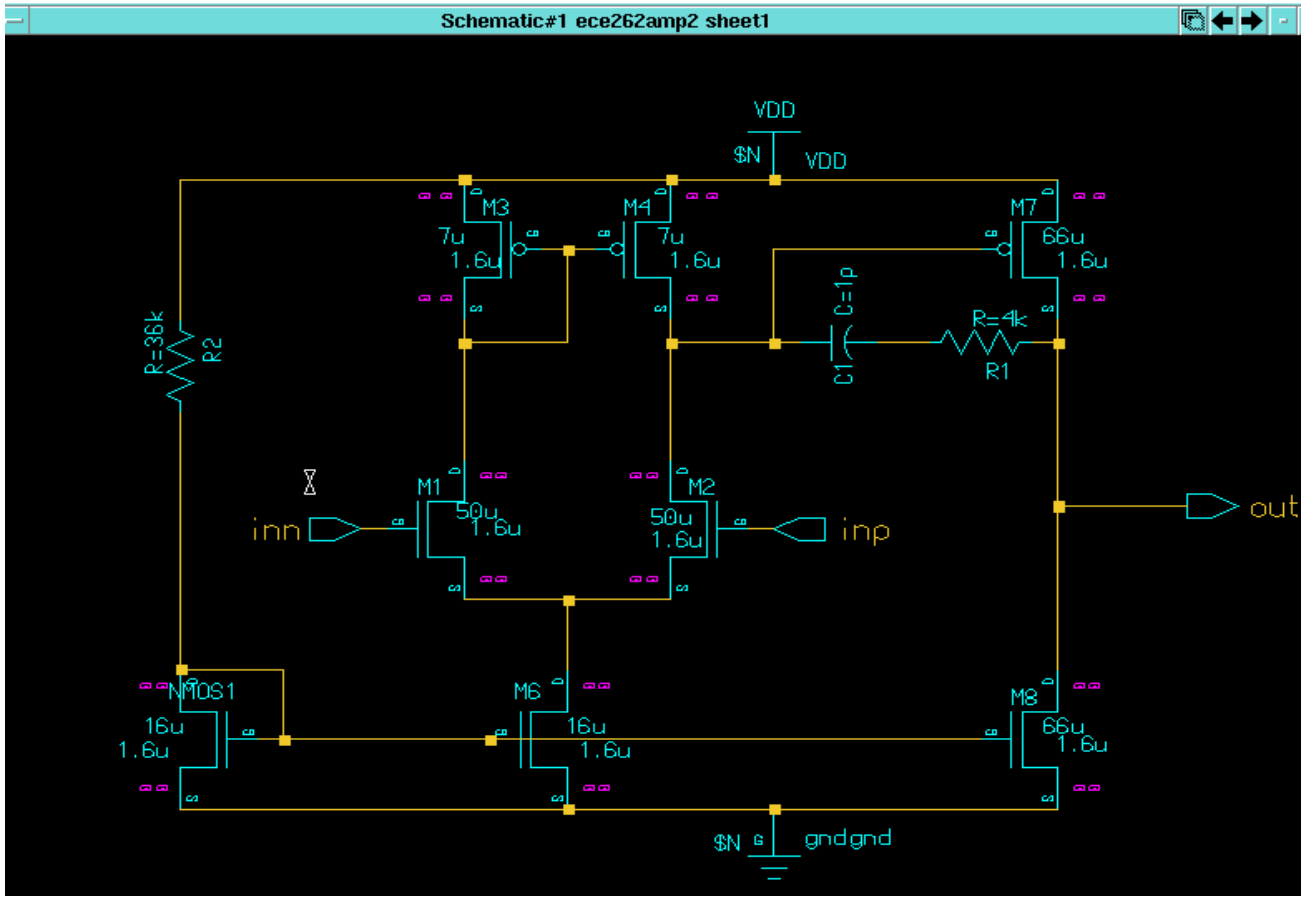
Simulation Results - Output



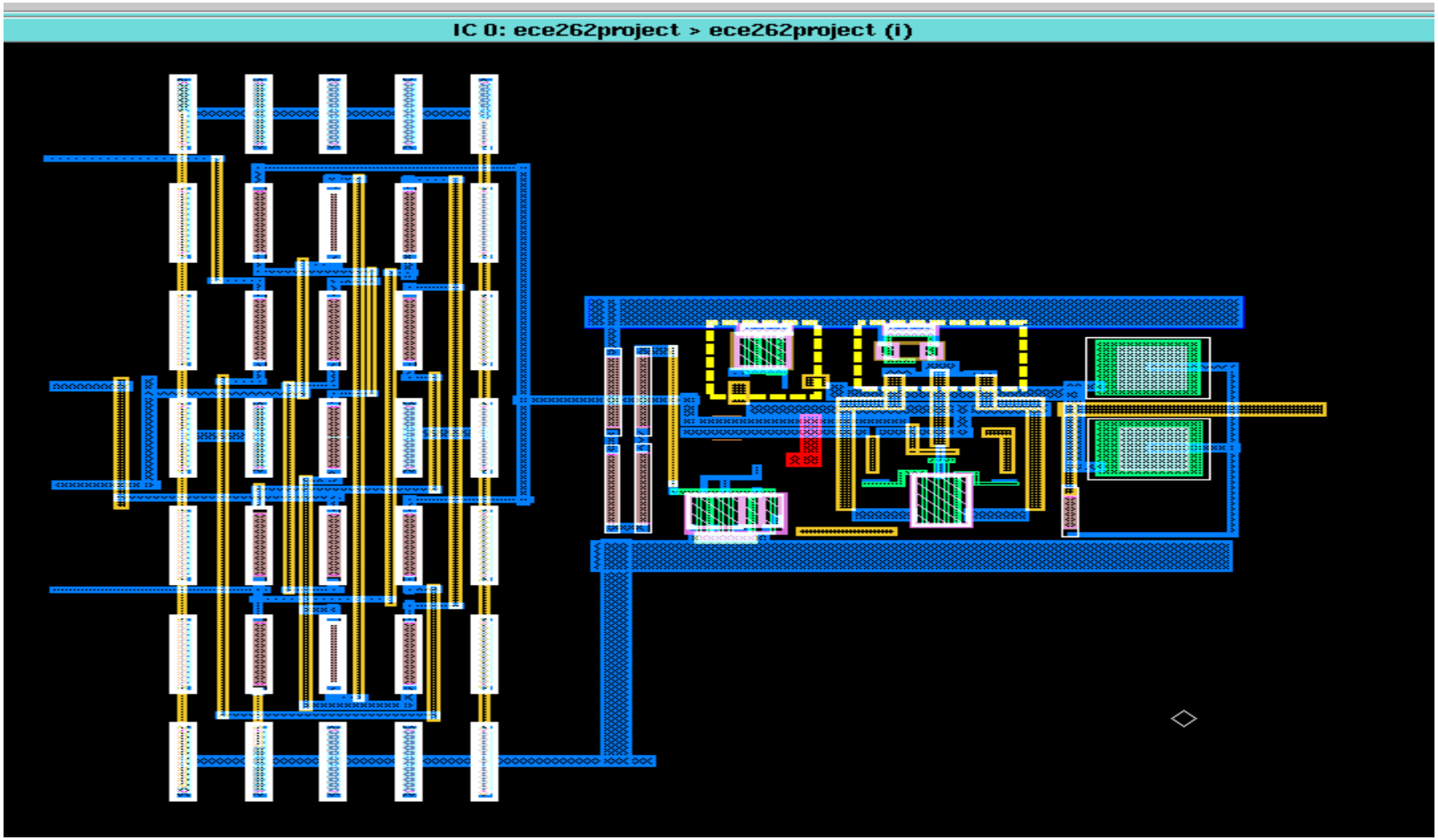
Overall Schematic



Op-amp schematic



Layout



Final Specifications

- Vdd = 5V
- Amplifier Power Dissipation = 5V*0.6mA=3mW
- Resistor power dissipation (WC) – (5V)^2/24kOhm=1mW
- Total Power Dissipation – **4mW**
- For the output stage: The following spec was met

$$\Delta t < \frac{T_{\min}}{2^{N+1}}; \frac{\Delta V}{SR} = \frac{V_{dd}}{2^N SR} < \frac{1}{f_{\max} 2^{N+1}}; \frac{V_{dd}}{SR} < \frac{1}{2 f_{\max}}; SR > 2V_{dd} f_{\max} = 2 \times 5V \times 100MHz$$

$$SR > 1 \frac{mV}{ps}$$

Final Specifications (cont.)

- Components
  - 5 resistors with resistance 2R
  - 3 resistors with resistance R
  - Op-amp
    - 8 transistors
    - 2 resistors
    - 1 capacitor
- Unit Resistance (R) = 8kOhm
  - 2R = 16kOhm
- Area of layout = 390um*458um = 178,620(um)^2=0.18 (mm)^2

Design Challenges

- The biggest design challenge was figuring out some LVS problems with device models.
- It was also a challenge to modify an existing op-amp layout to suit my purposes and to hook up a large number of resistors in a common-centroid layout.
- The rest of the design process went very smoothly