Advanced Topics

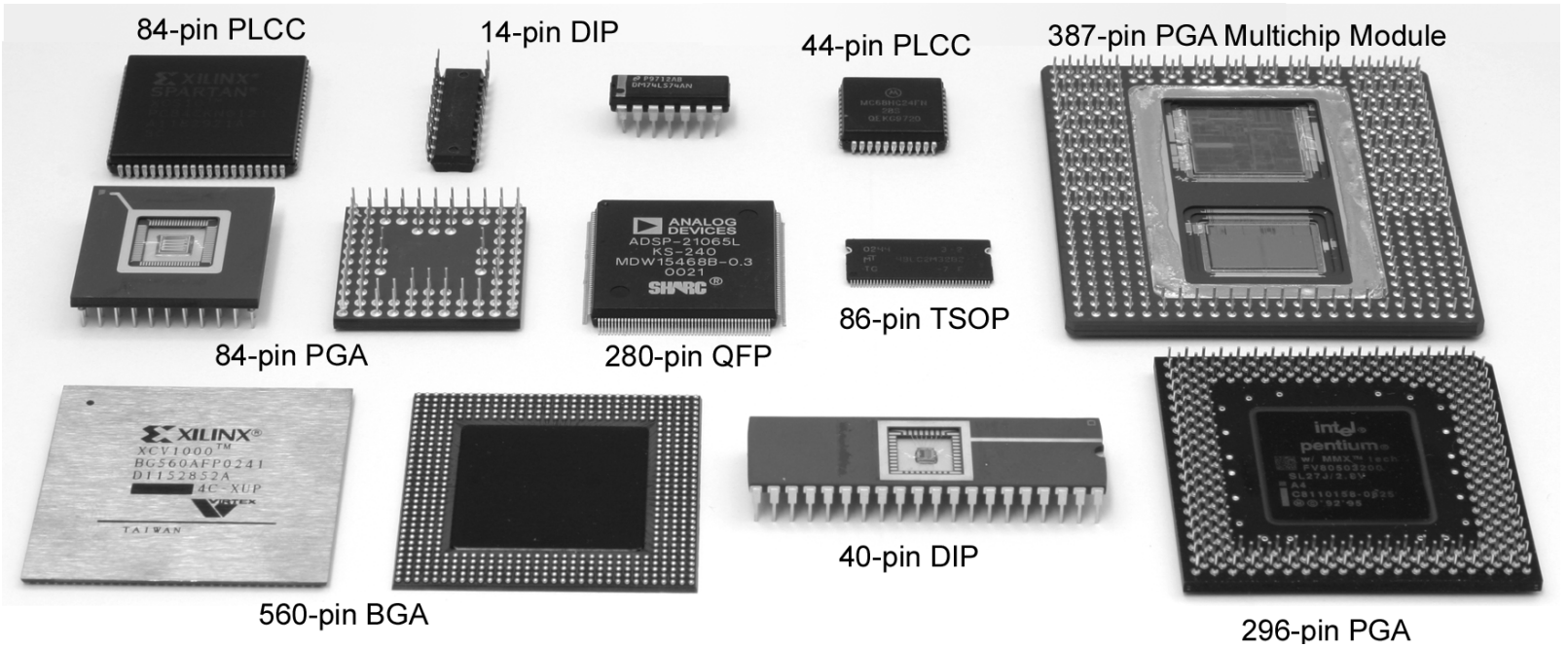
- Packaging
- Power Distribution
- I/O

Packages

- Package functions
  - Electrical connection of signals and power from chip to board
  - Little delay or distortion
  - Mechanical connection of chip to board
  - Removes heat produced on chip
  - Protects chip from mechanical damage
  - Compatible with thermal expansion
  - Inexpensive to manufacture and test

Package Types

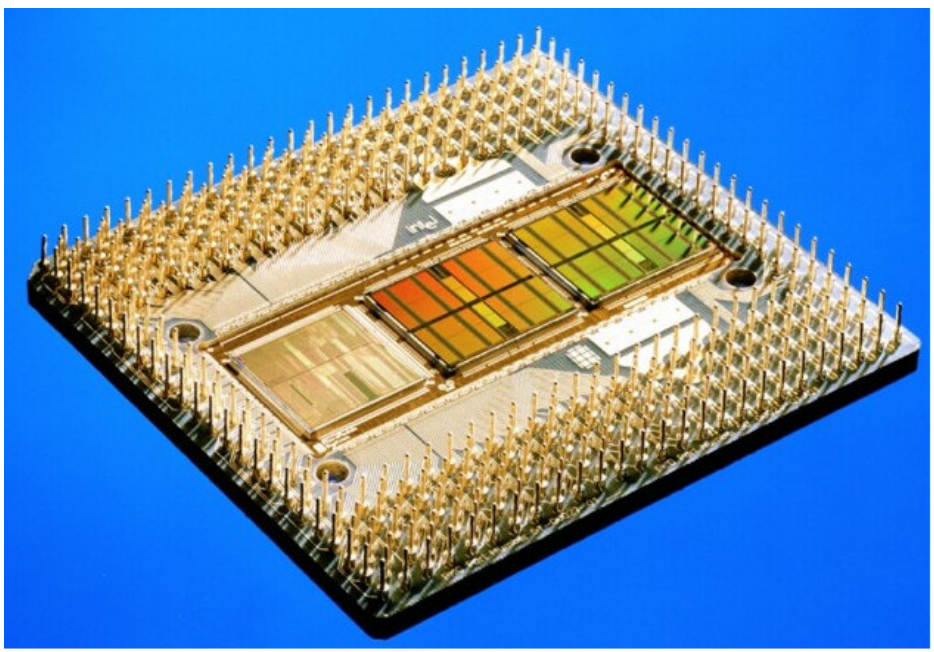
- Through-hole vs. surface mount



DIP: Dual-inline package, PGA: Pin grid array; PLCC: Plastic leadless chip carrier
BGA: Ball grid array, QFP: Quad flat pack, TSOP: Thin small outline package

Multichip Modules

- Pentium Pro MCM
  - Fast connection of CPU to cache
  - Expensive, requires known good dice

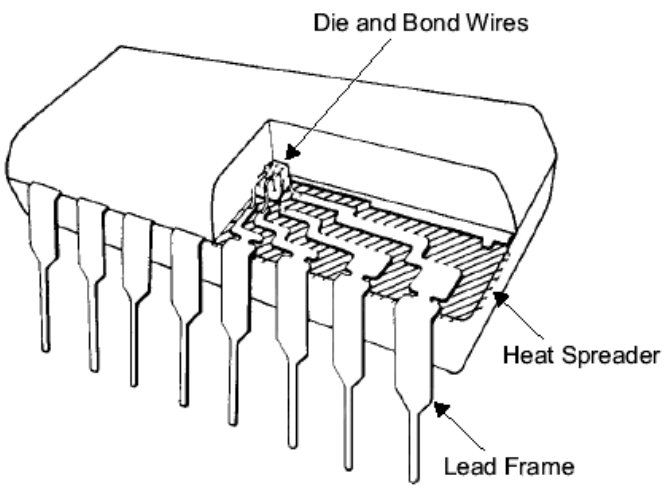


Microprocessor +
one or two external cache die

IBM z900 mainframe:
20 CPUs, 8 cache chips, 1km of Interconnect, 127mm on a side, 1.3 kW power

Chip-to-Package Bonding

- Traditionally, chip is surrounded by *pad frame*
  - Metal pads on 100 – 200 μm pitch
  - Gold *bond wires* attach pads to package
  - *Lead frame* distributes signals in package
  - Metal *heat spreader* helps with cooling



Advanced Packages

- Bond wires contribute parasitic inductance
- Fancy packages have many signal, power layers
  - Like tiny printed circuit boards
- *Flip-chip* places connections across surface of die rather than around periphery
  - Top level metal pads covered with solder balls
  - Chip flips upside down
  - Carefully aligned to package (done blind!)
  - Heated to melt balls
  - Also called *C4* (Controlled Collapse Chip Connection)

Heat Dissipation

- 60 W light bulb has surface area of 120 cm^2
- Itanium 2 die dissipates 130 W over 4 cm^2
  - Chips have enormous power densities
  - Cooling is a serious challenge
- Package spreads heat to larger surface area
  - Heat sinks may increase surface area further
  - Fans increase airflow rate over surface area
  - Liquid cooling used in extreme cases ($$$)
  - Smart and active cooling using microfluidics (our project as Duke University)

Example

- Your chip has a heat sink with a thermal resistance to the package of 4.0 ° C/W.
- The resistance from chip to package is 1 ° C/W.
- The system box ambient temperature may reach 55 ° C.
- The chip temperature must not exceed 100 ° C.
- What is the maximum chip power dissipation?

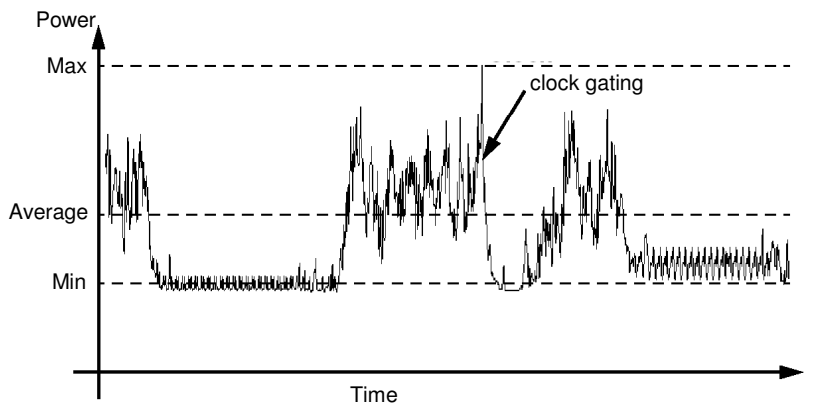
- (100-55 C) / (4 + 1 C/W) = 9 W

Power Distribution

- Power Distribution Network functions
  - Carry current from pads to transistors on chip
  - Maintain stable voltage with low noise
  - Provide average and peak power demands
  - Provide current return paths for signals
  - Avoid electromigration & self-heating wearout
  - Consume little chip area and wire
  - Easy to lay out

Power Requirements

- $V_{DD} = V_{DDnominal} - V_{droop}$
- Want V_{droop} < +/- 10% of V_{DD}
- Sources of V_{droop}
  - IR drops
  - L di/dt noise
- I_{DD} changes on many time scales



Input / Output

- Input/Output System functions
  - Communicate between chip and external world
  - Drive large capacitance off chip
  - Operate at compatible voltage levels
  - Provide adequate bandwidth
  - Limit slew rates to control di/dt noise
  - Protect chip against electrostatic discharge
  - Use small number of pins (low cost)

I/O Pad Design

- Pad types
  - V_{DD} / GND
  - Output
  - Input
  - Bidirectional
  - Analog

Output Pads

- Drive large off-chip loads (2 – 50 pF)
  - With suitable rise/fall times
  - Requires chain of successively larger buffers
- Guard rings to protect against latchup
  - Noise below GND injects charge into substrate
  - Large nMOS output transistor
  - p+ inner guard ring
  - n+ outer guard ring
    - In n-well