

Basal Metabolic Rate Calculator

ECE261 Full-Custom VLSI Design
Project
Fall 2008

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Basic Predictive Equation for BMR Calculator

- ▶ For male subject :

$BMR = (-790 + 3 \times \text{age} + 9 \times \text{Heart Rate} + 3 \times \text{Weight})$
calories/hour


For female subject :

$BMR = (-290 + \text{age} + 6 \times \text{Heart Rate} - 2 \times \text{Weight})$
calories/hour

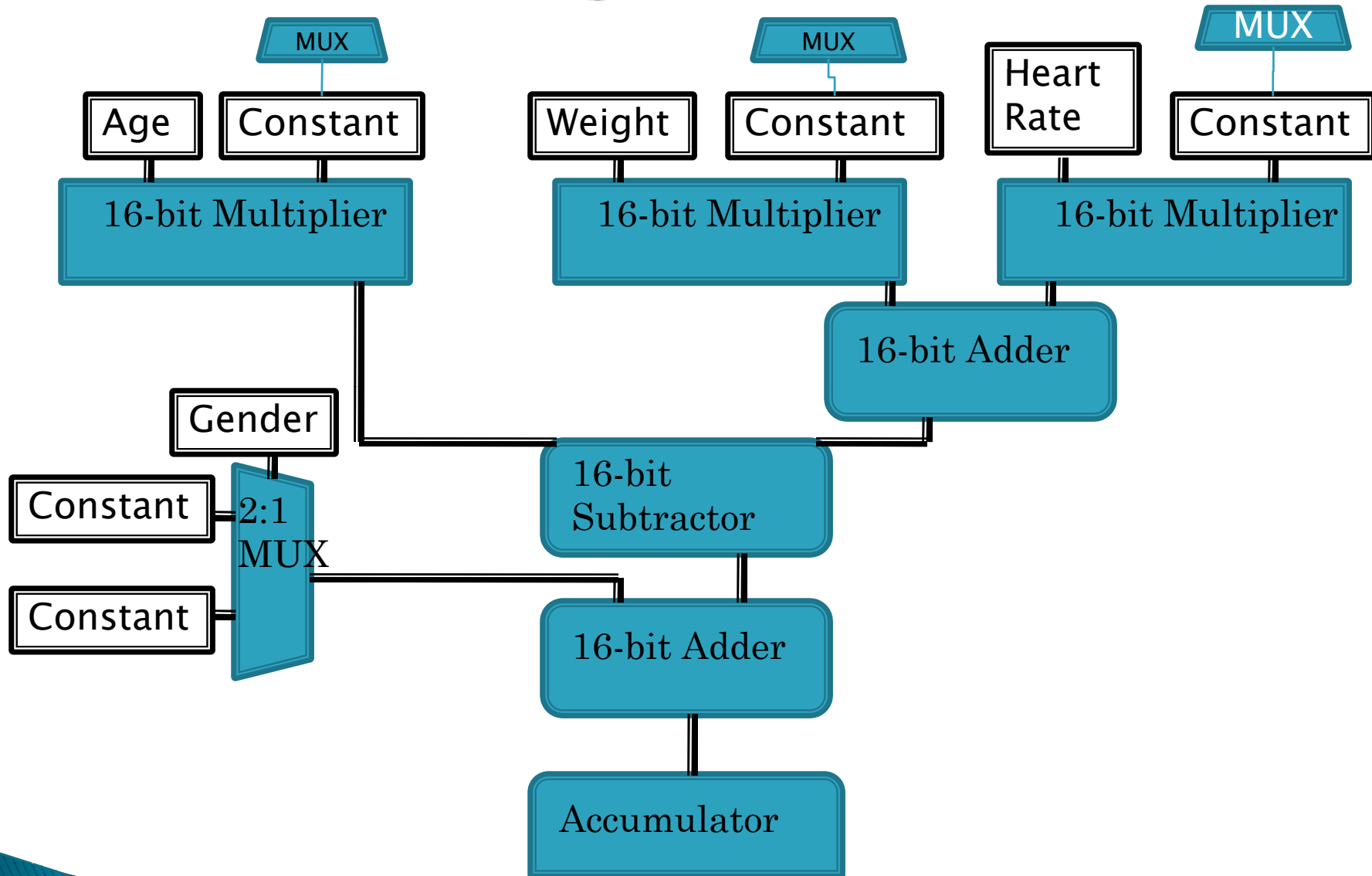
Found on: Wikipedia

Verified from:

MD, Mifflin. "A new predictive equation for resting energy expenditure in healthy individuals." The American Journal of Clinical Nutrition 51 (1990): 241-247 .

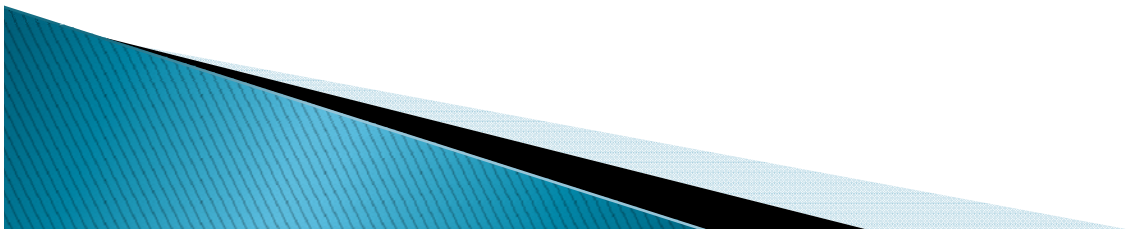


Initial Block Diagram for BMRCalculator

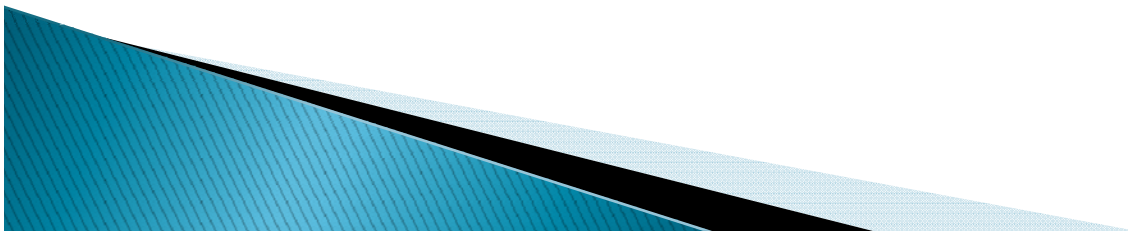


Implementation

- ▶ To generate the whole circuit, we talk about the individual sub-circuits in the form of :
- ▶ 1) The multiplier – To create a 16 bit multiplier we use two 8-bit multipliers with carry propagation from the LSB to the MSB. The multiplier is a hierarchical structure composed of full adders arranged in stages to perform the cascaded multiplication operation.
- ▶ 2) We also use a 16 bit adder subtractor circuit consisting of 16 full adders.



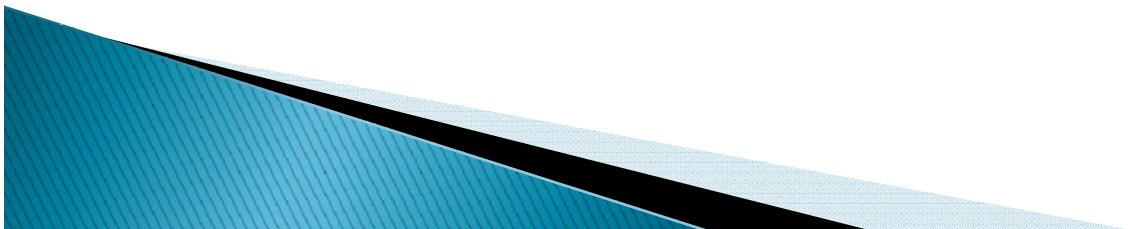
Schematics



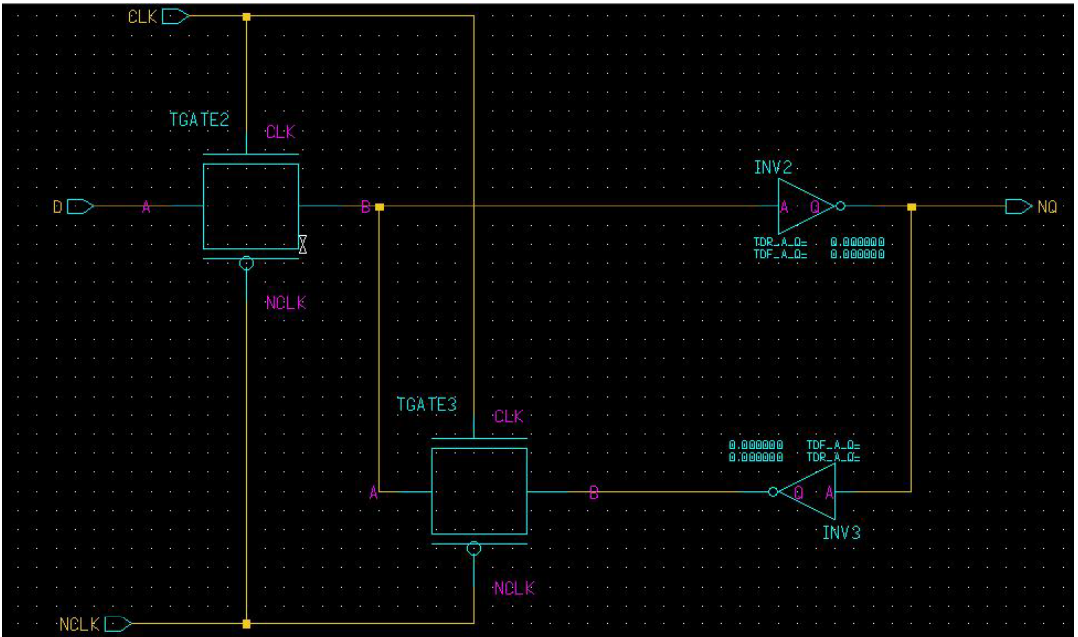
General Information

The basic devices used in designing the various complex devices in our circuit include 2-input AND gate, 2:1 Multiplexer, 2-input OR gate, inverters and transmission gates.

The p-D latch and n-D latch units are designed so that they can together be used to work as the Master Slave D Flip-flop.

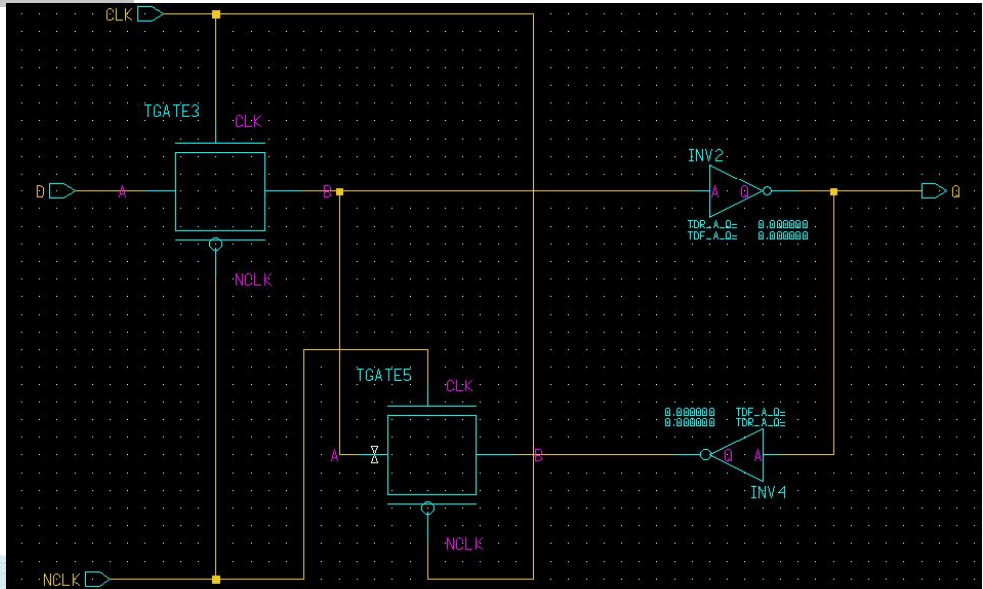


Master and slave devices

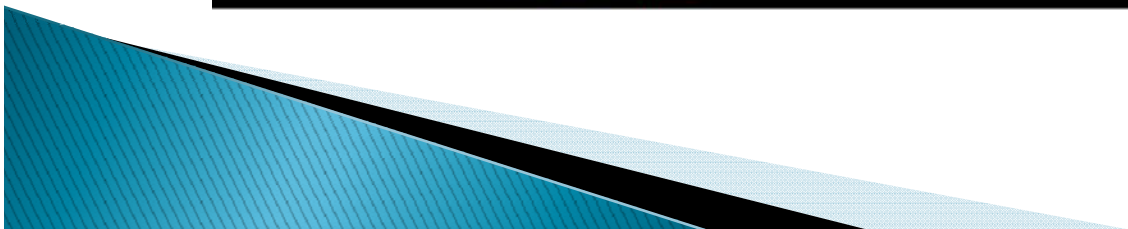
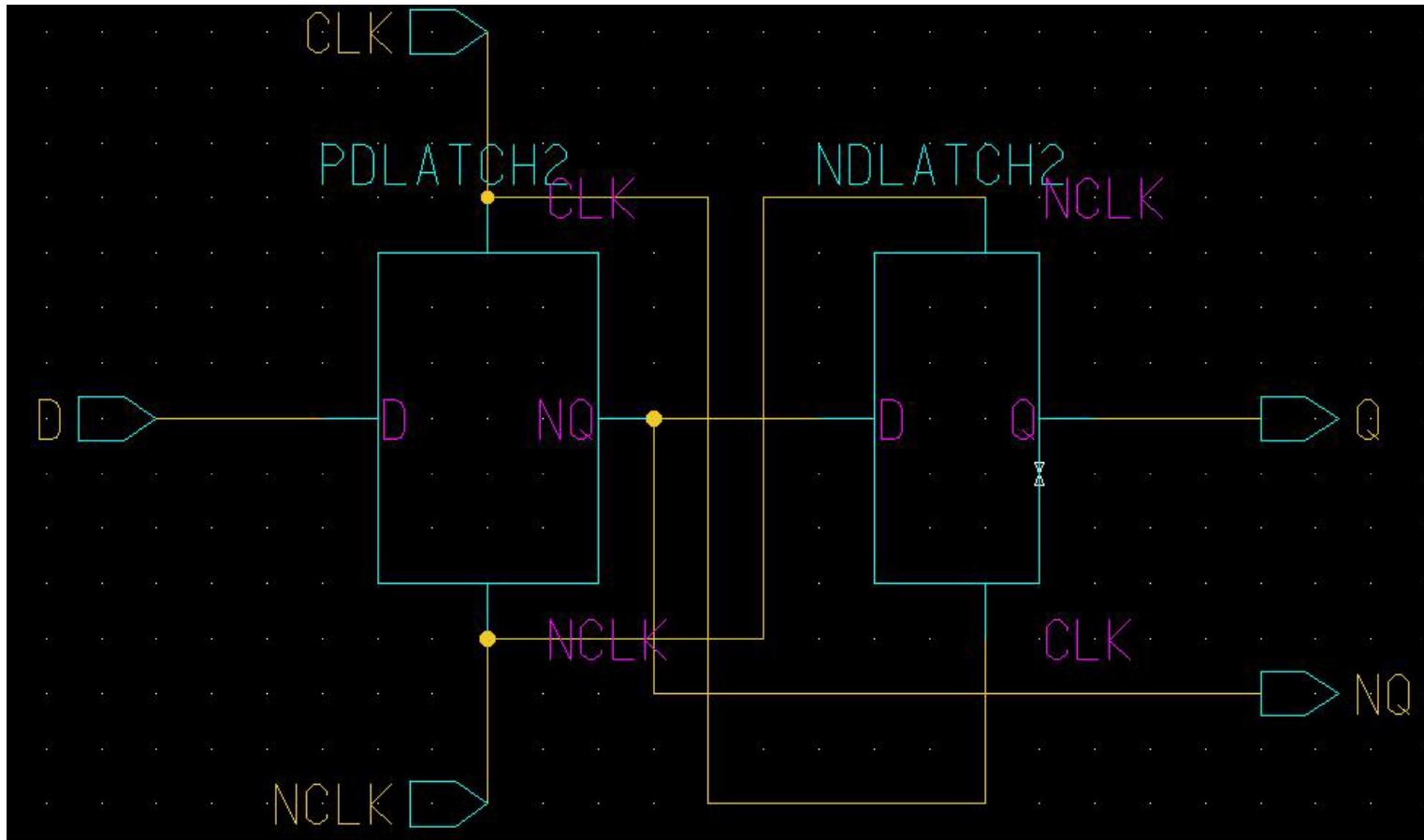


The Master D Latch

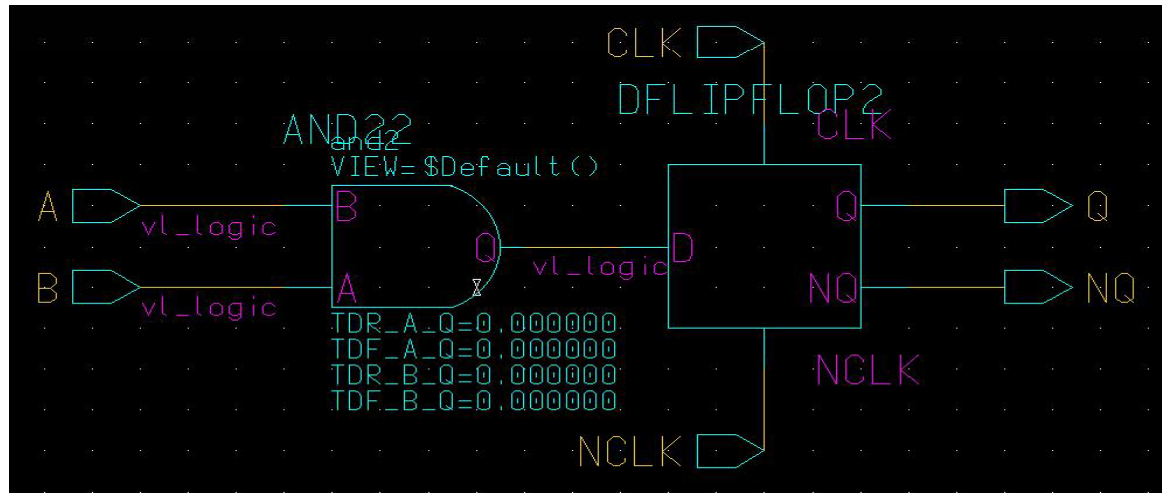
The Slave D Latch



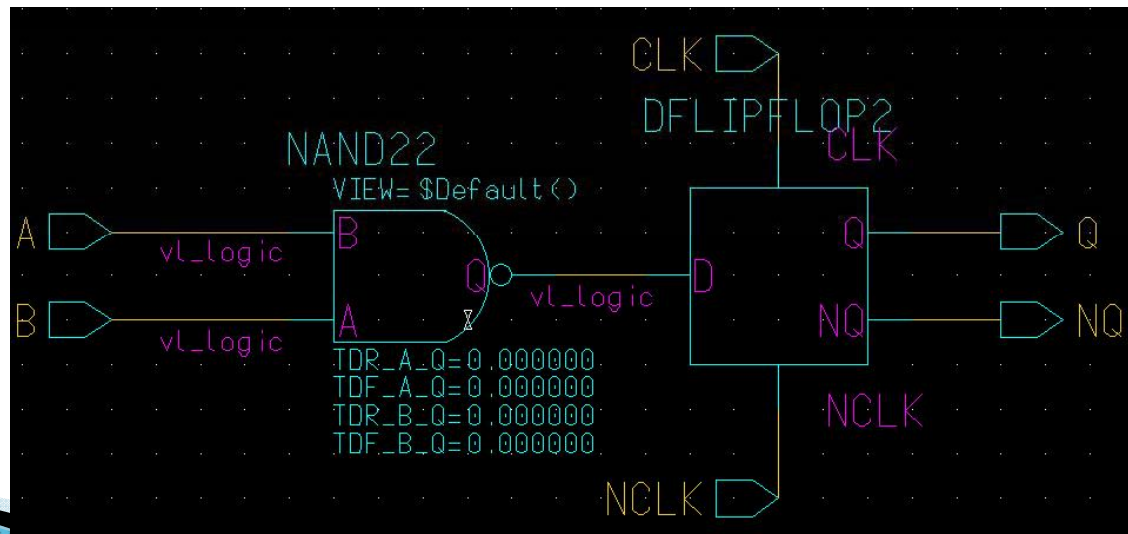
D Flip-flop



AND Flip-flop and NAND Flip-flops

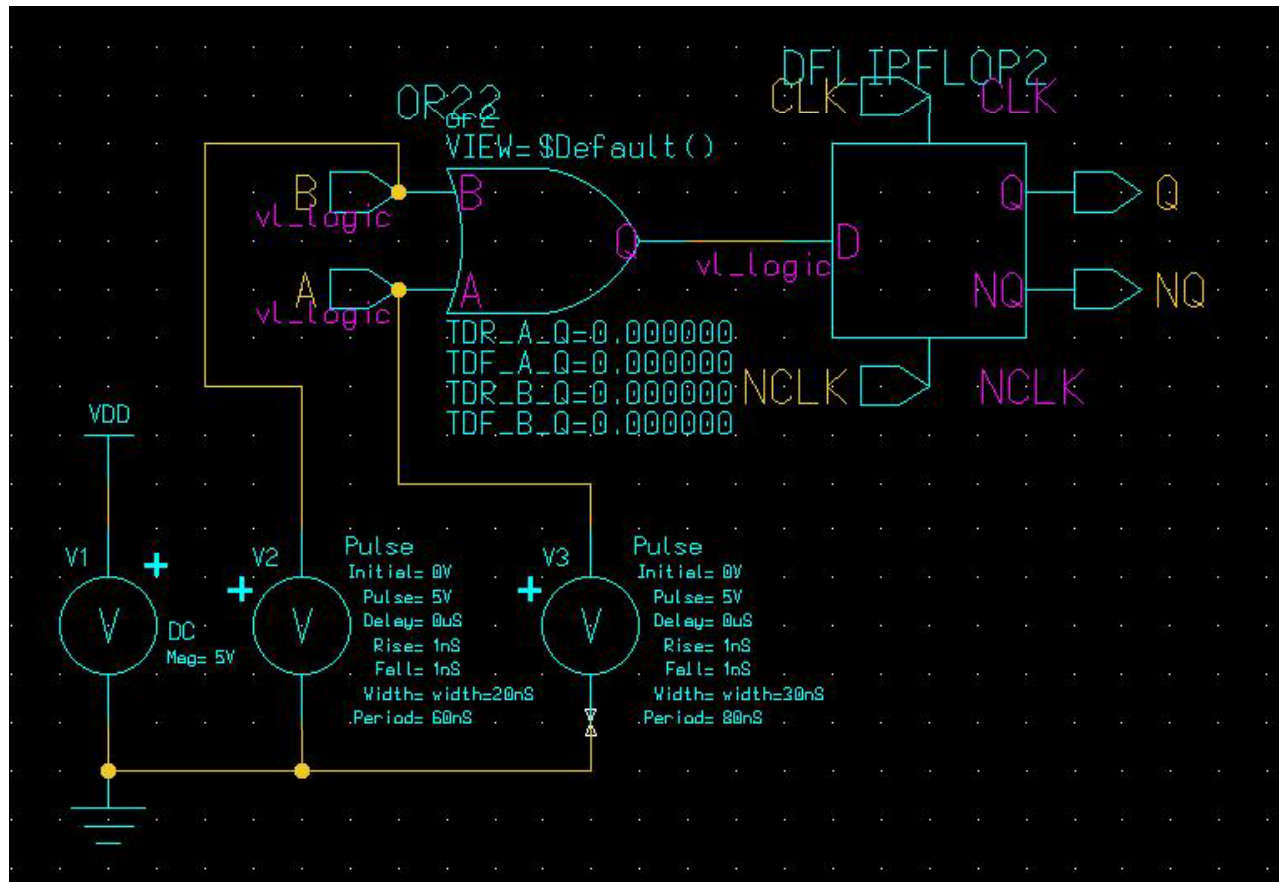


AND Flip-flop



NAND Flip-flop

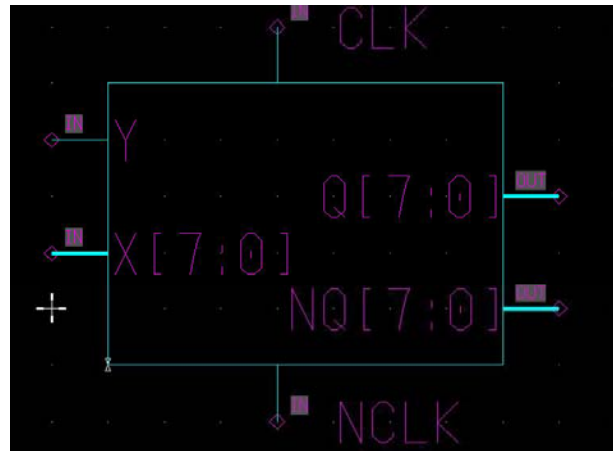
OR Flip-flop



OR Flip-flops

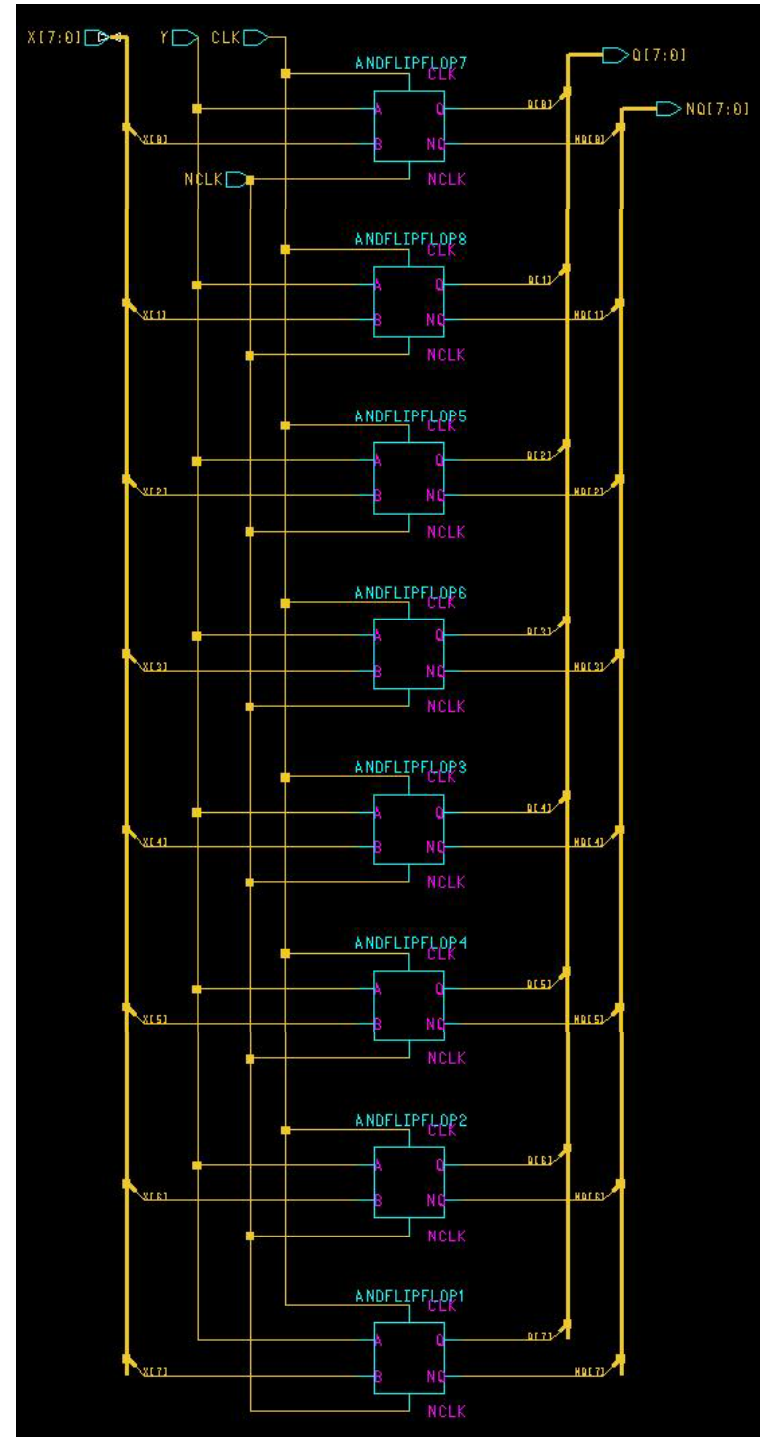
They have two inputs A & B with two clocks - CLK and negation of CLK. The output Q is the OR of A & B. O & NQ are the outputs. The OR of A & B gets stored in the

8 - input AND gate

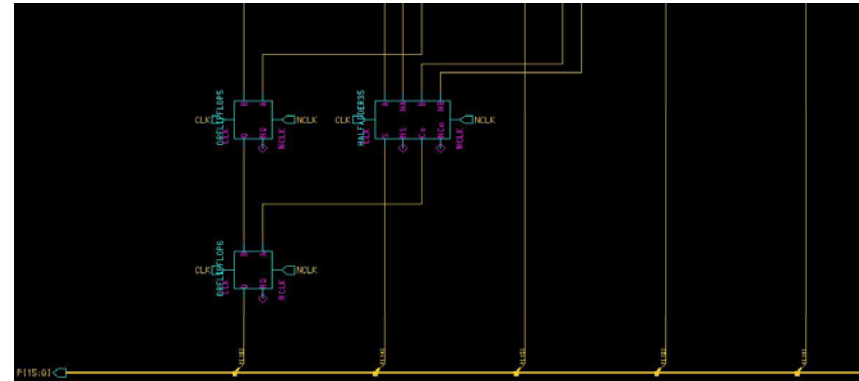
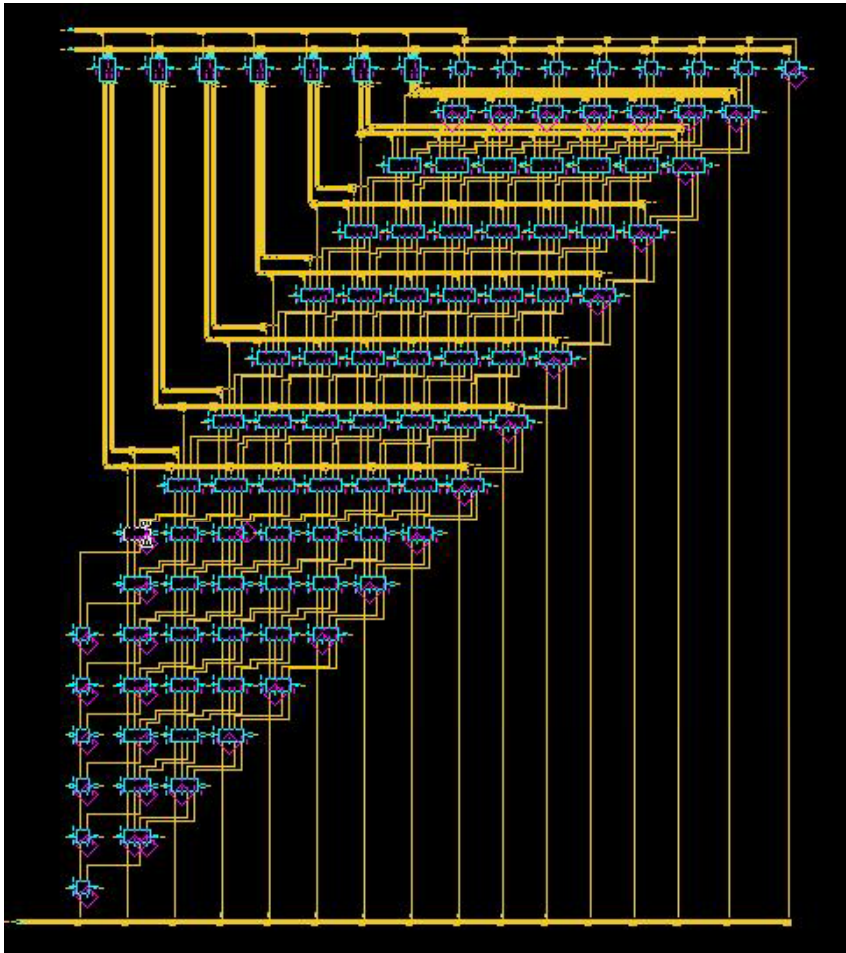


8 - input AND symbol

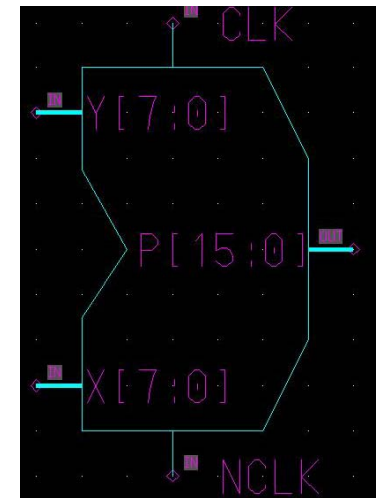
The 8-input AND gate has two 8 bit inputs and an 8 bit output and two clock inputs. It is essentially composed of 8 AND flip-flops.



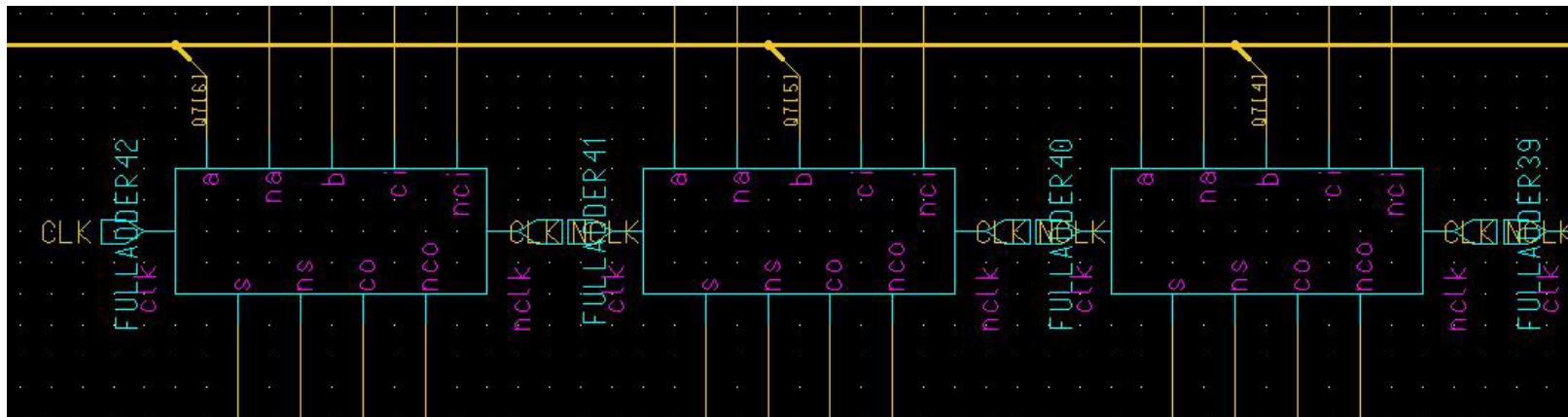
8-bit Multiplier



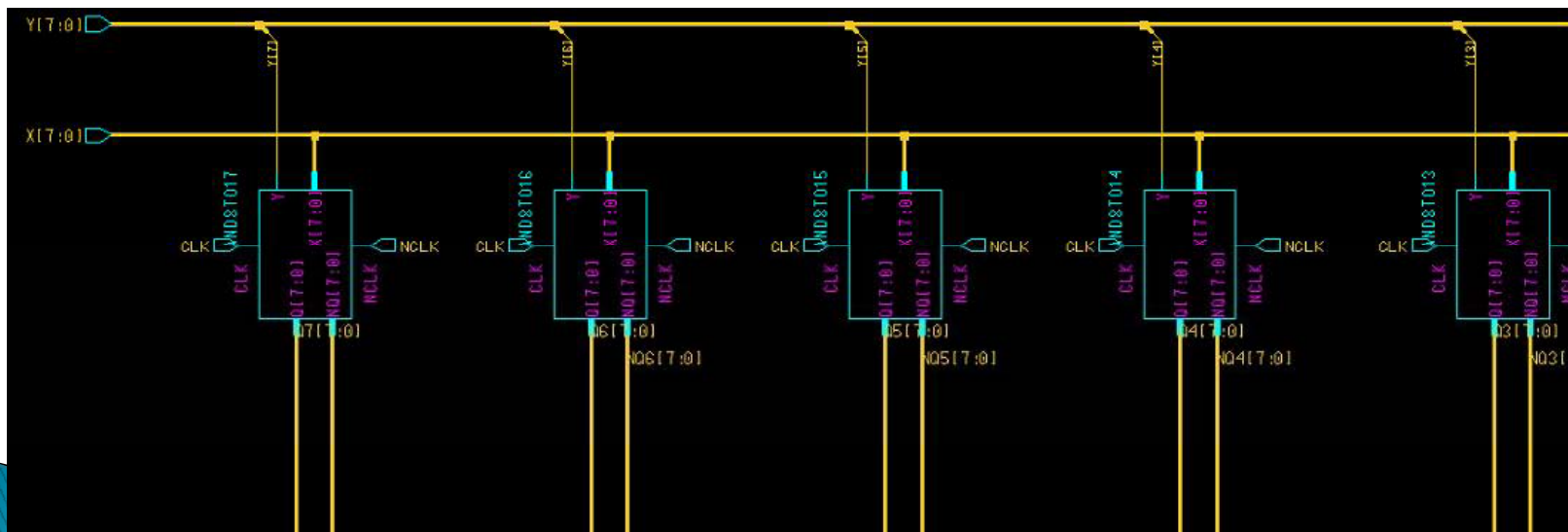
We have implemented an 8 bit multiplier for multiplying each pair of each decimal digits. The output is the 16-bit product. As shown in the symbol it has two 8 bit inputs for the multiplier and the multiplicand and a 16-bit output denoting the product. It has two clock inputs too.



Multiplier (continued)

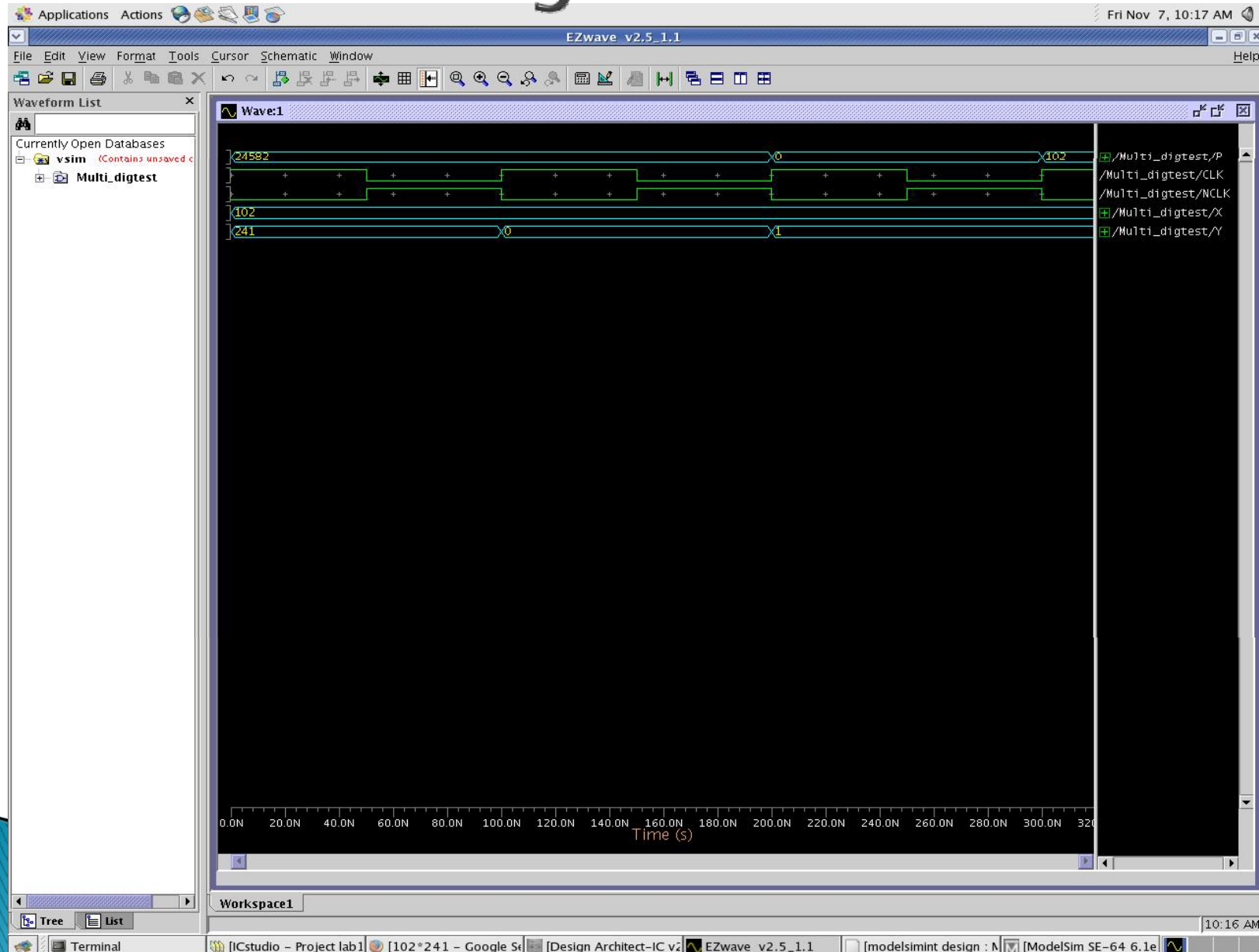


View of one of the rows of the multiplier



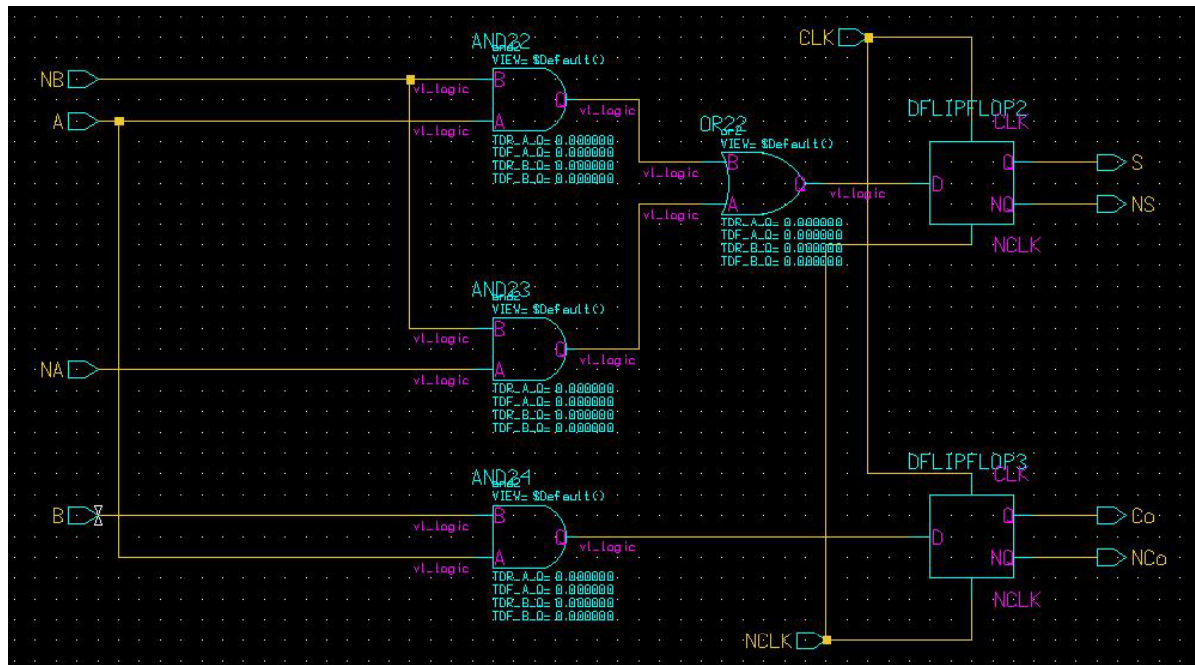
View of the top row of and flip-flops followed by half adders to perform the first step of multiplication.

Digital Simulation for the multiplier using ModelSim

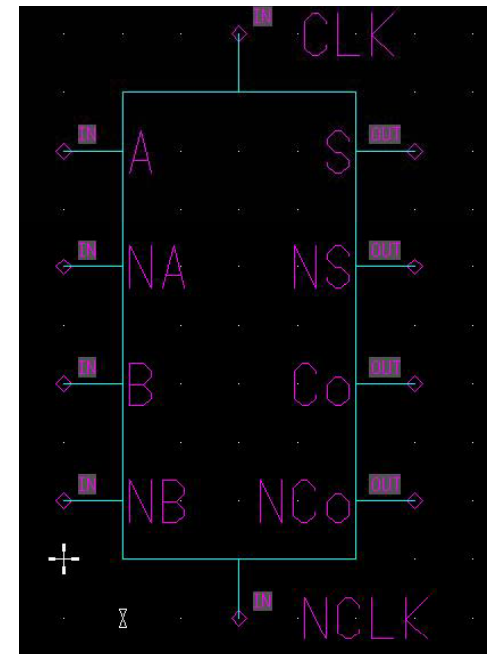


Adders

1) Half Adder Flip flop

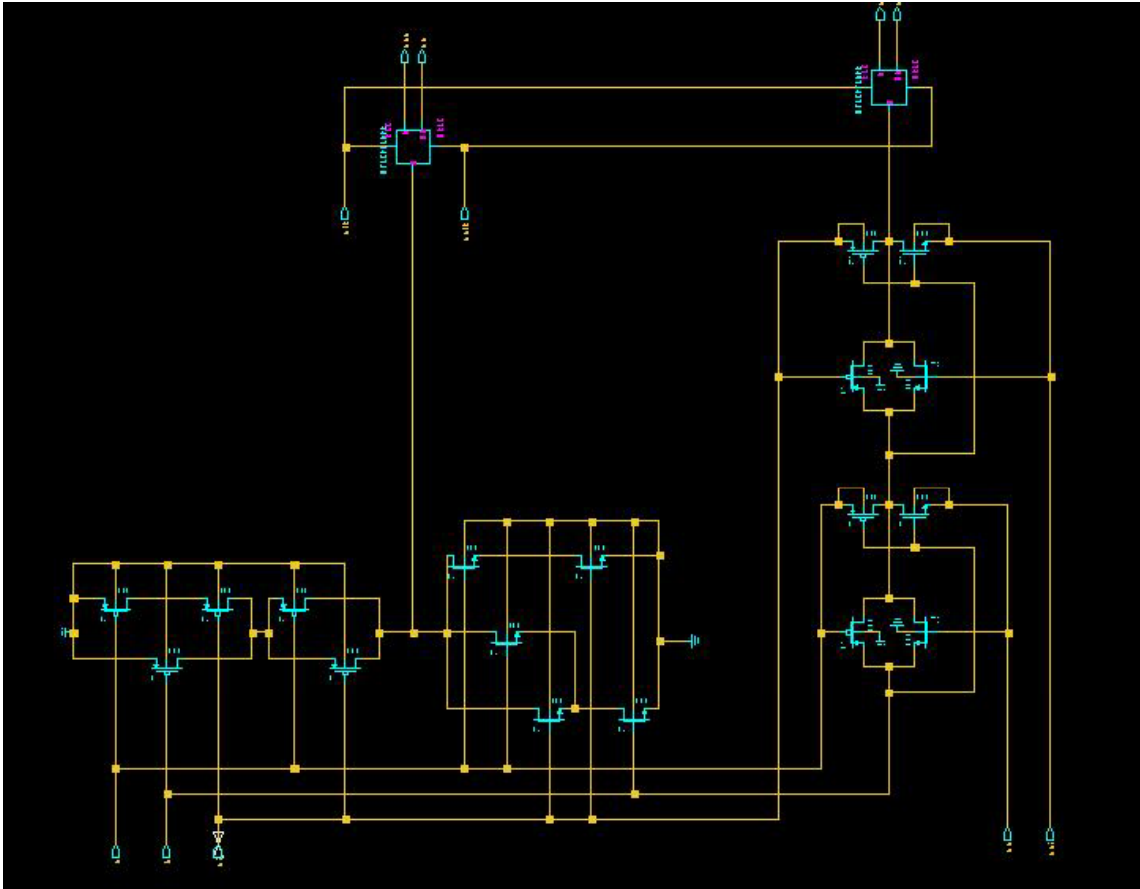


Half Adder Flip-flop Schematic

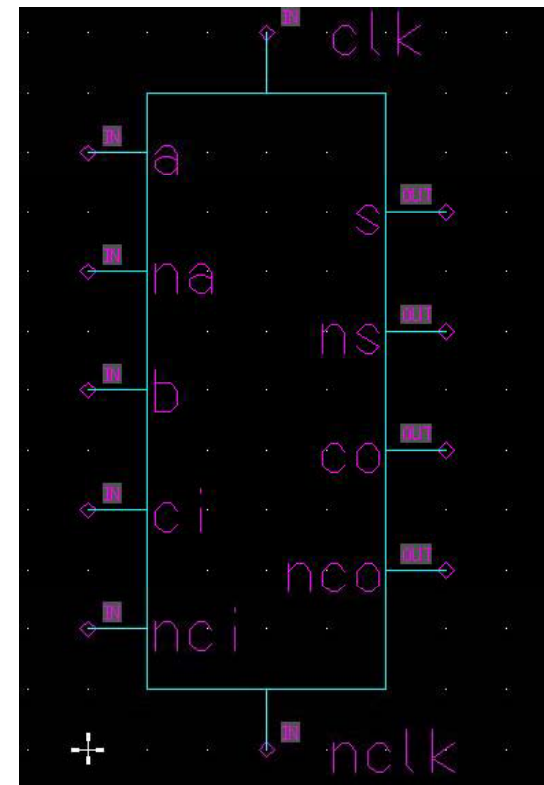


Half Adder Flip-flop symbol

Adders (continued)

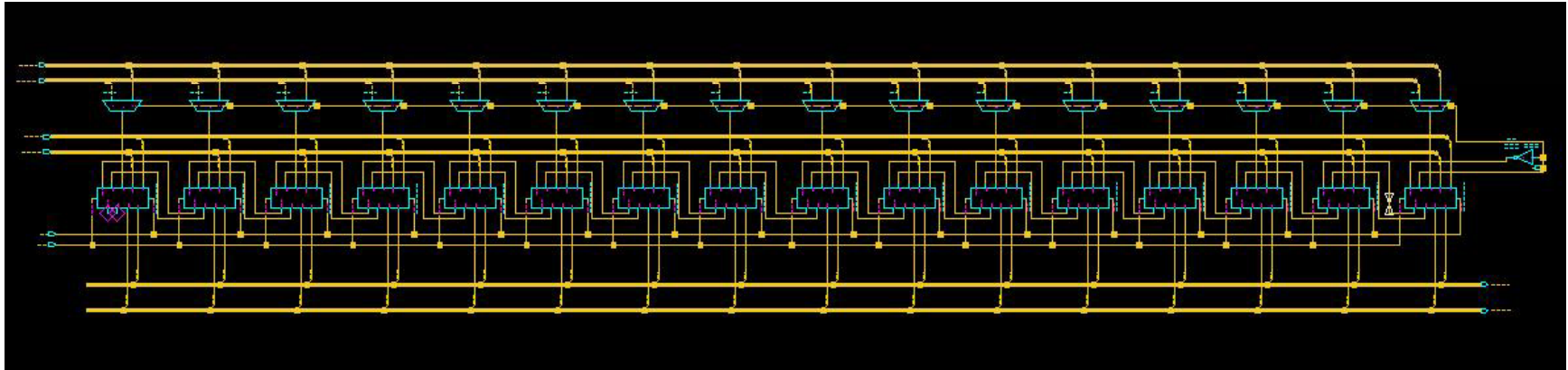


Full adder flip-flop schematic



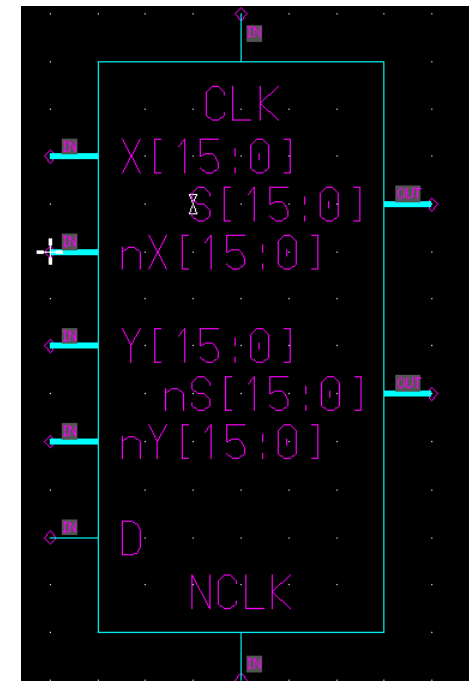
Full Adder Flip-flop symbol

Adder / Subtractor

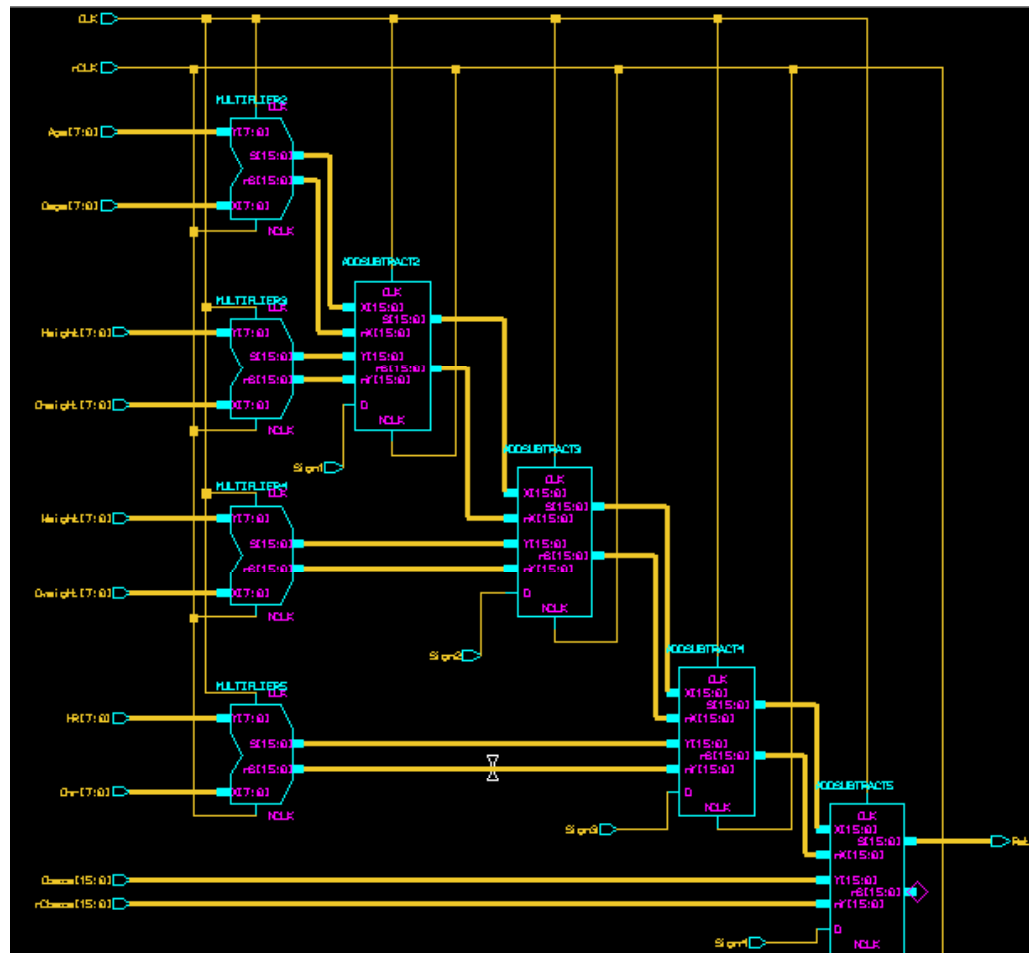


Schematic for the adder/subtractor

Symbol for the adder/subtractor



Schematic for the whole circuit

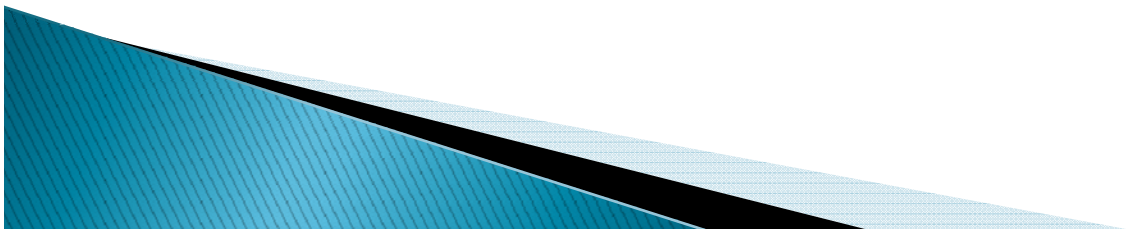


Basal Metabolic Rate Generator

At the end of the day we have a device count of 16,236 transistors.

Power Estimate and Area of the circuit

- ▶ Dynamic Power Estimate = $\alpha * C * V^2 * f$
 - $\alpha = 0.1$ for CMOS static logic
 - $C_{\text{logic}} = 16236 * 12 \lambda * .4 \text{ um} / \lambda * 2 \text{ fF/um} = 155 \text{ pF}$
 - $P_{\text{dynamic}} = 0.1 * 155 \text{ pF} * 5 \text{ V}^2 * f \approx .4 \text{ mW/MHz}$
 - Refreshing rate is 1 Hz
 - Overall power .4nW/second
- ▶ Each transistor $20 \lambda * 10 \lambda$ (λ is 0.4um in 0.8 um technology)
- ▶ Number of transistors = 16,236
- ▶ Total area $16236 * 20 \lambda * 10 \lambda * 120\% \approx 0.6 \text{ mm}^2$



Thank you for your patience !

