16-bit Parallel Input CRC

Baris Piyade

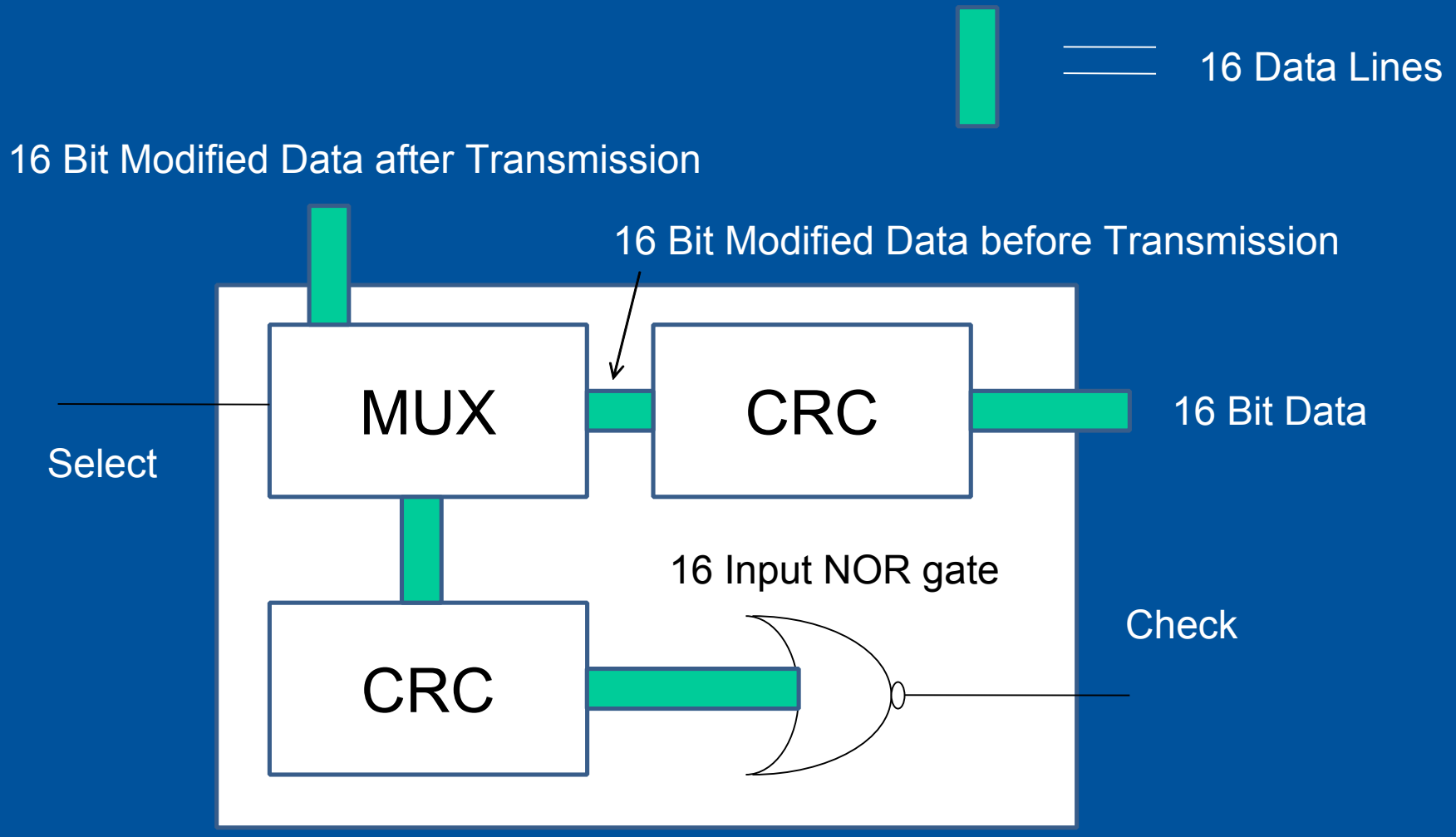
Chi Zhang

Matthew Roberts

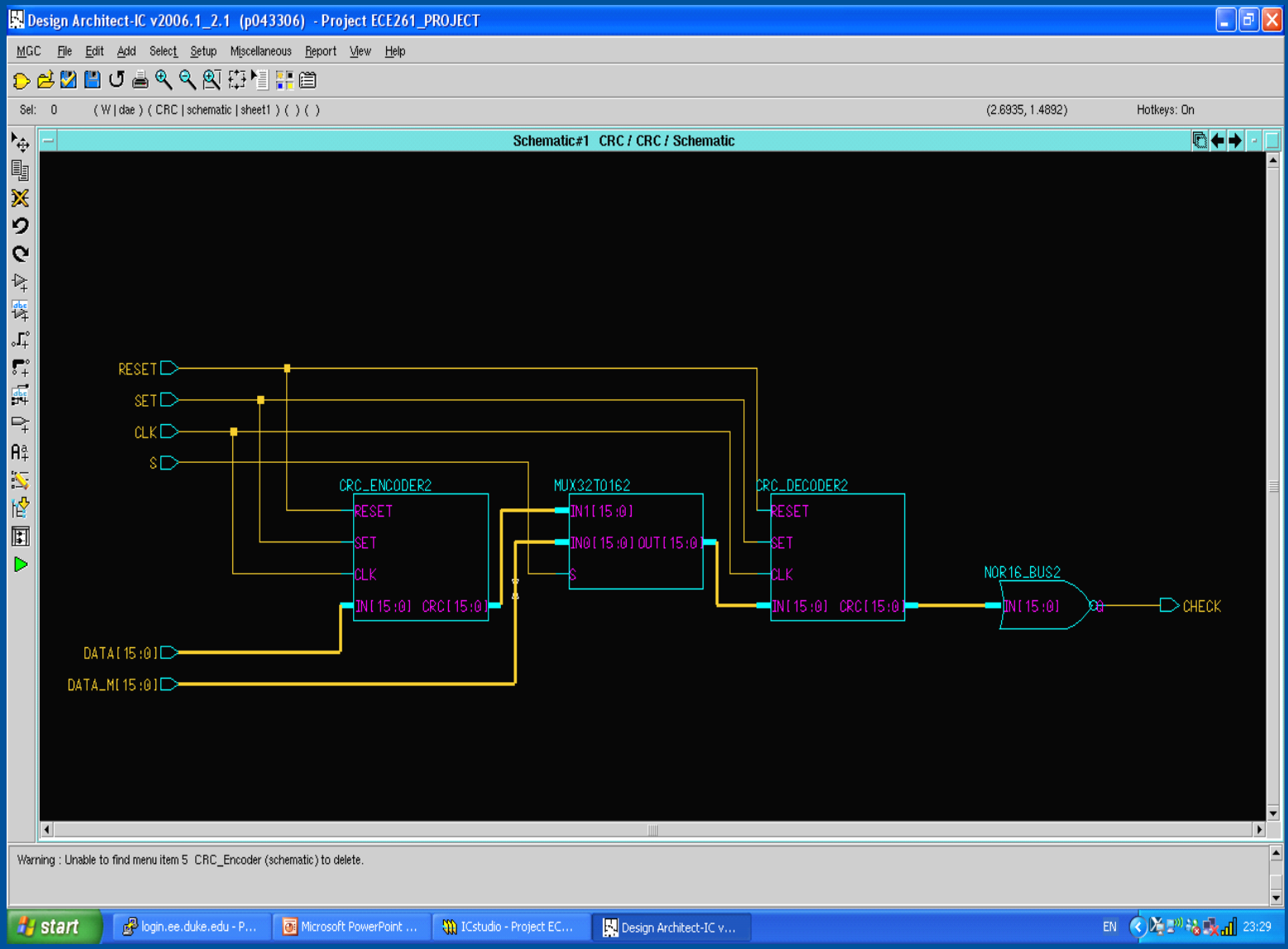
Abstract

This device is meant to mimic the operations of a 16-bit CRC checker. It contains a CRC block which encodes the 16-bit input and another which decodes it as well as a MUX and a 16-input NOR gate. The MUX selects whether you send the unmodified data through the decoder or a modified set of data. The modified data (DATA_M) is meant to represent corrupted data (i.e. data where one or more bits have been changed due to a lossy transmission line such as the path between 2 RF devices). If the unmodified data (DATA) is sent through the MUX, the output of the decoder should be all zeros which will cause the NOR gate to output a 1. If the modified data is sent through, the NOR gate should output a zero indicating that there has been data corruption.

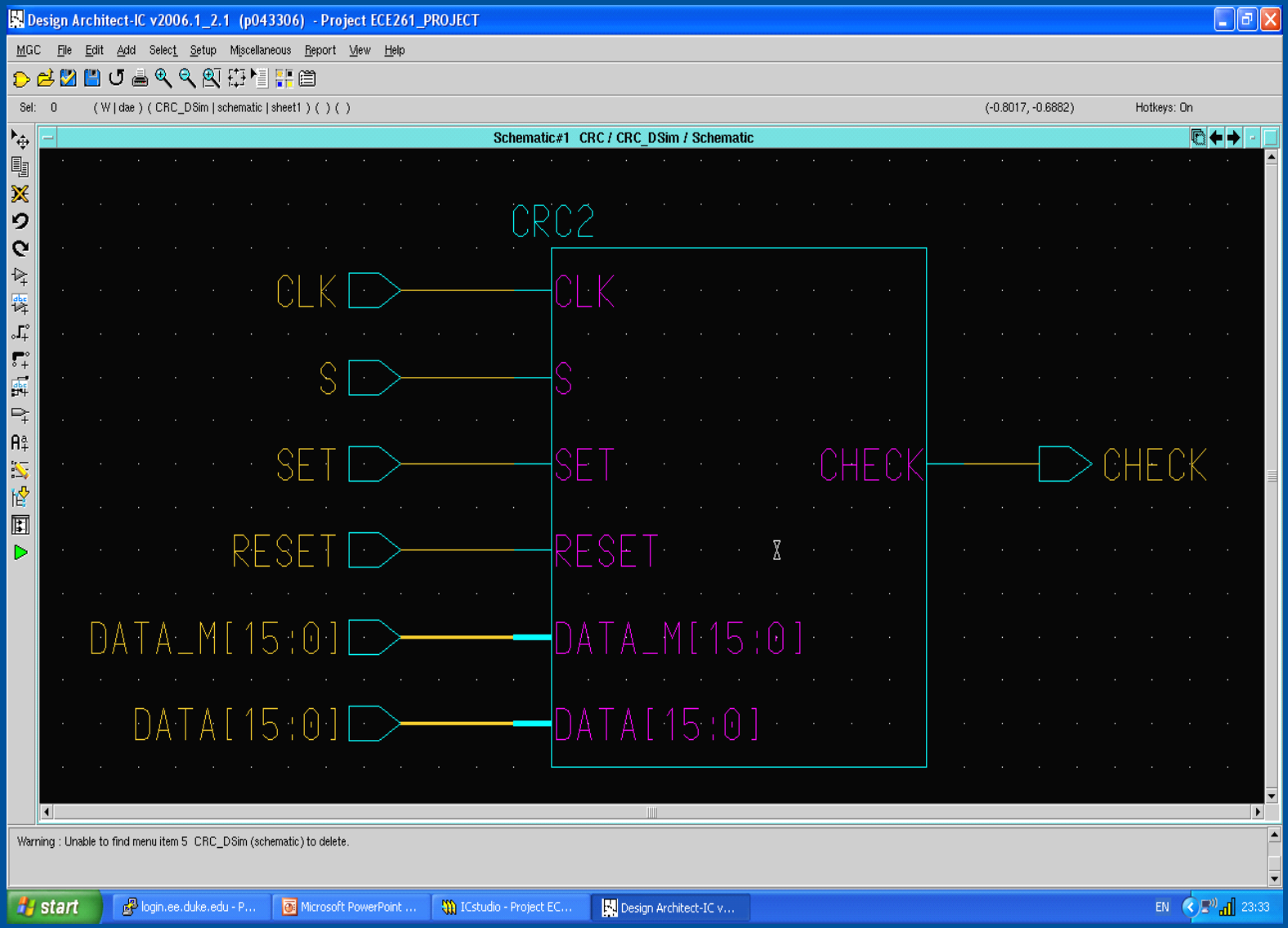
Block Diagram



The CRC Schematic



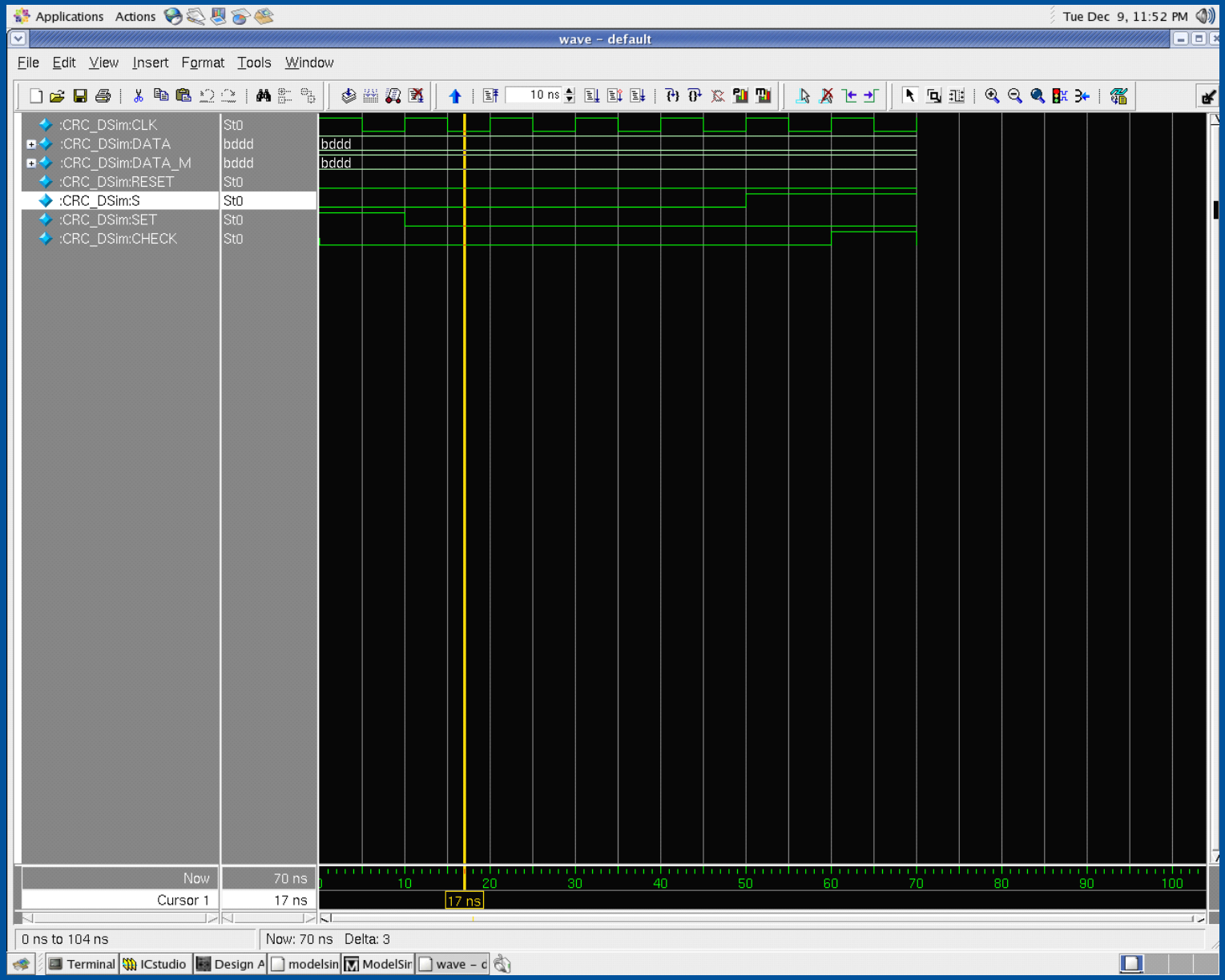
The CRC Simulation



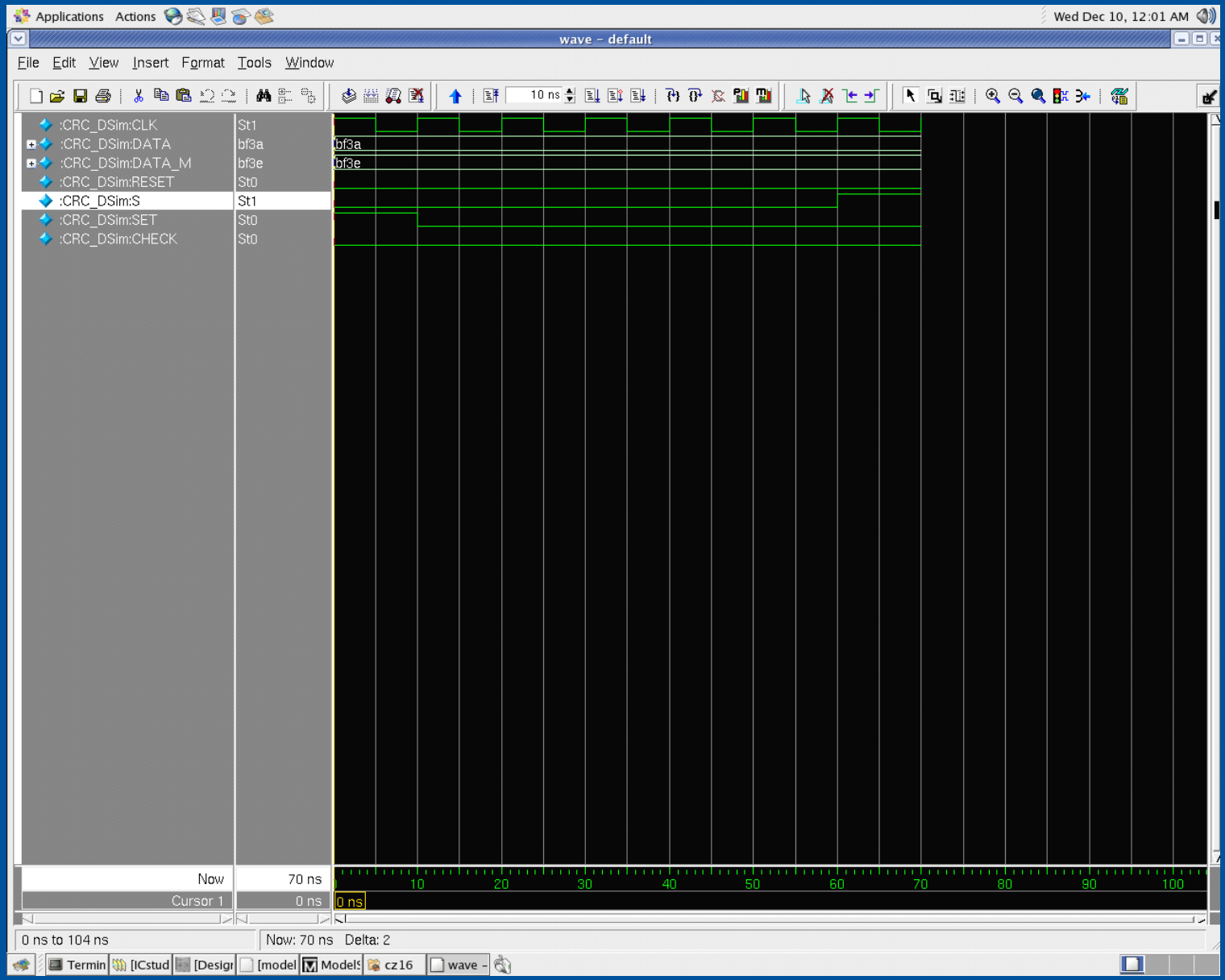
The CRC Simulation

The CRC simulation demonstrates that when "DATA" is passed through the MUX (which represents uncorrupted data) the Check output is 1. When "DATA_M" is passed and it is not identical to the CRC encoder output (which represents corrupted data), the Check output is zero

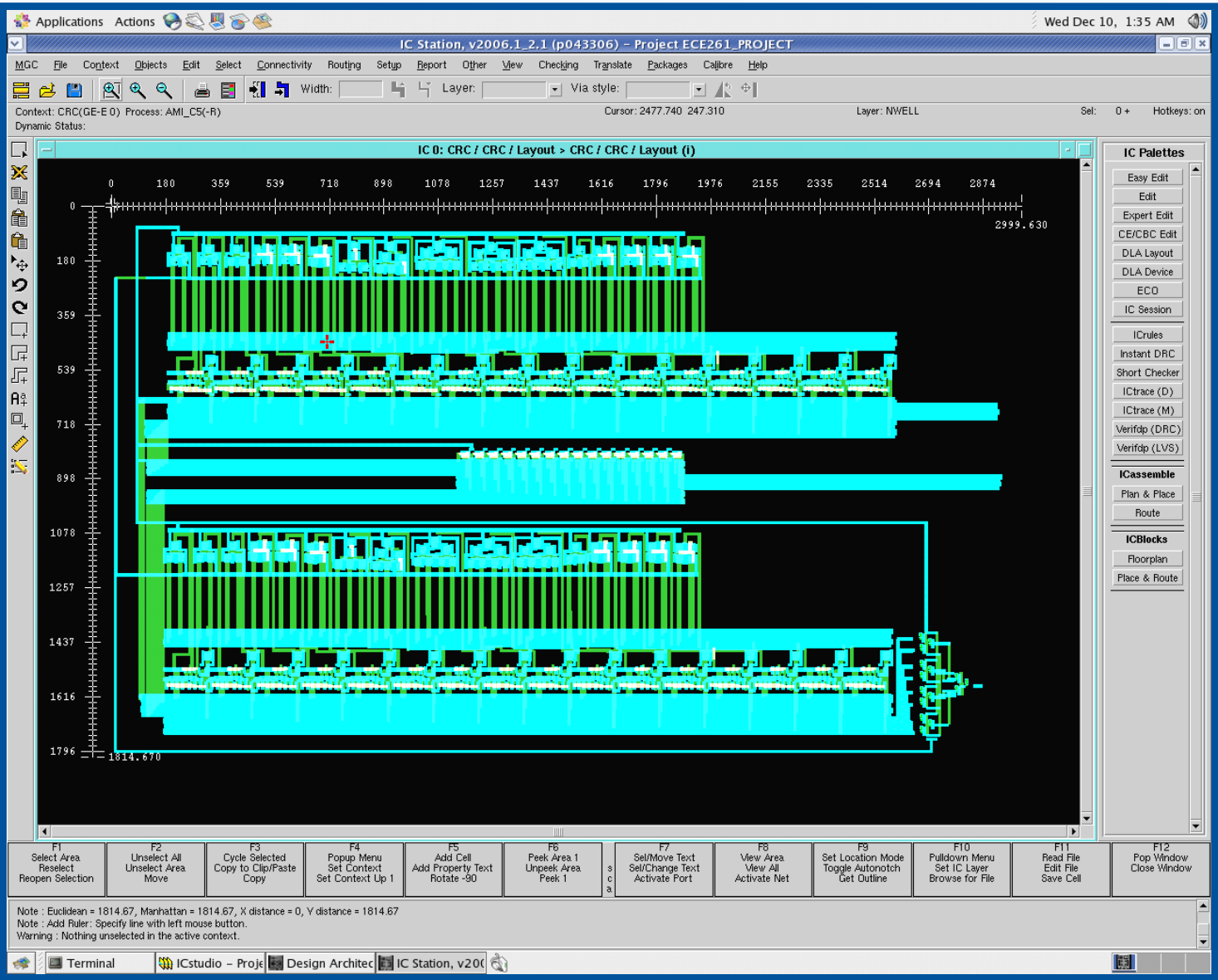
The CRC Simulation



The CRC Simulation

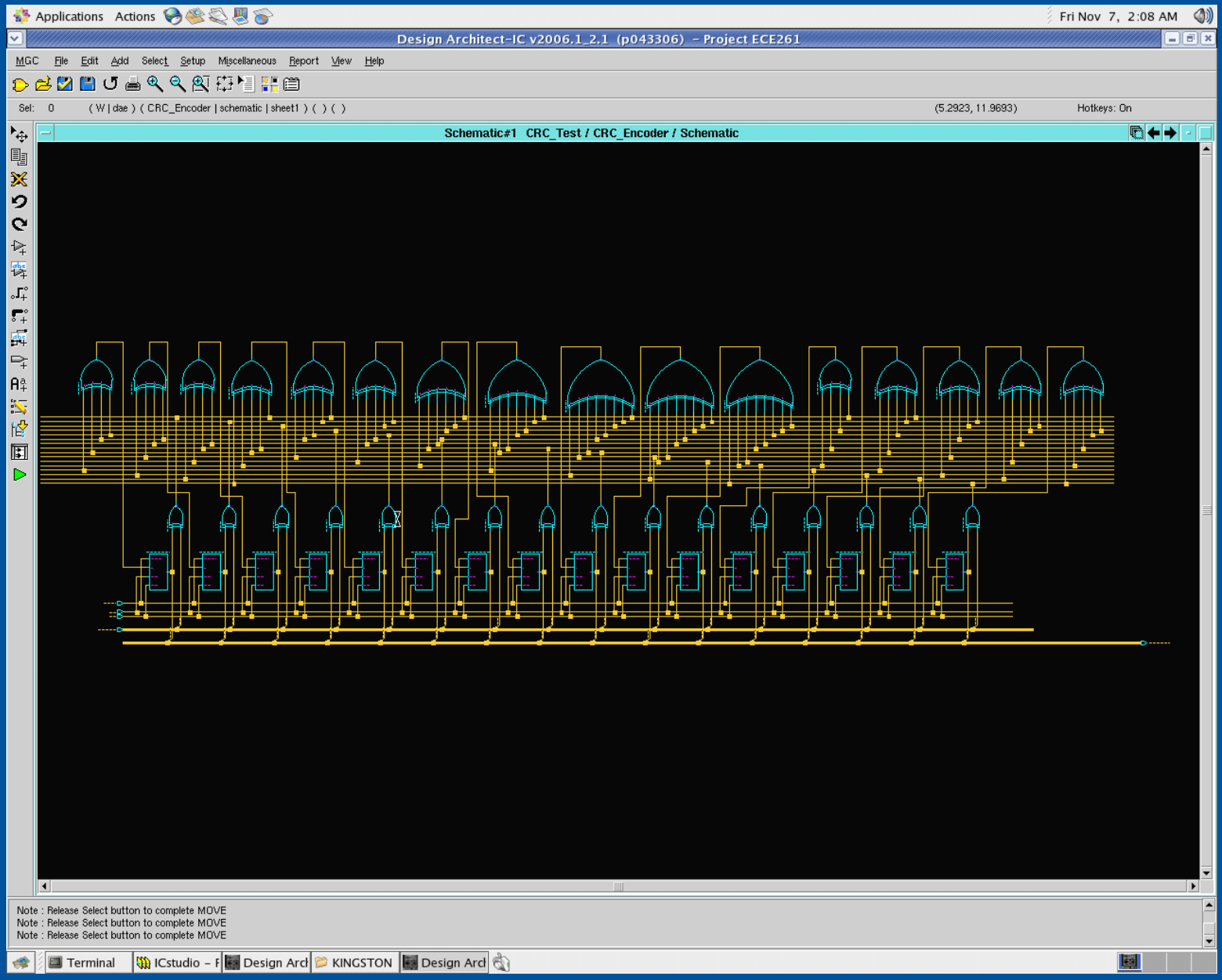


The CRC Top Level Layout

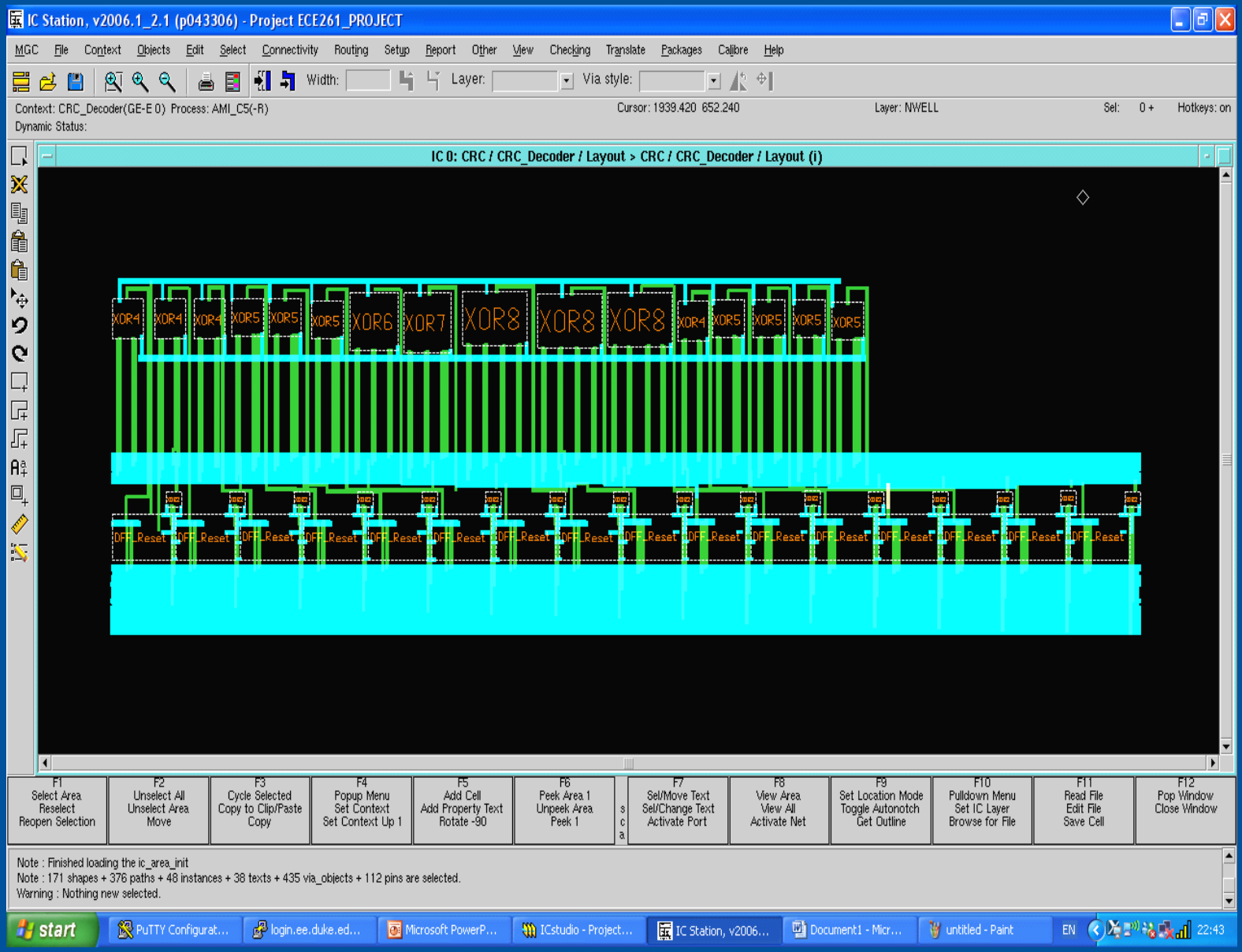


Area=1.8mm*3mm=5.4mm^2

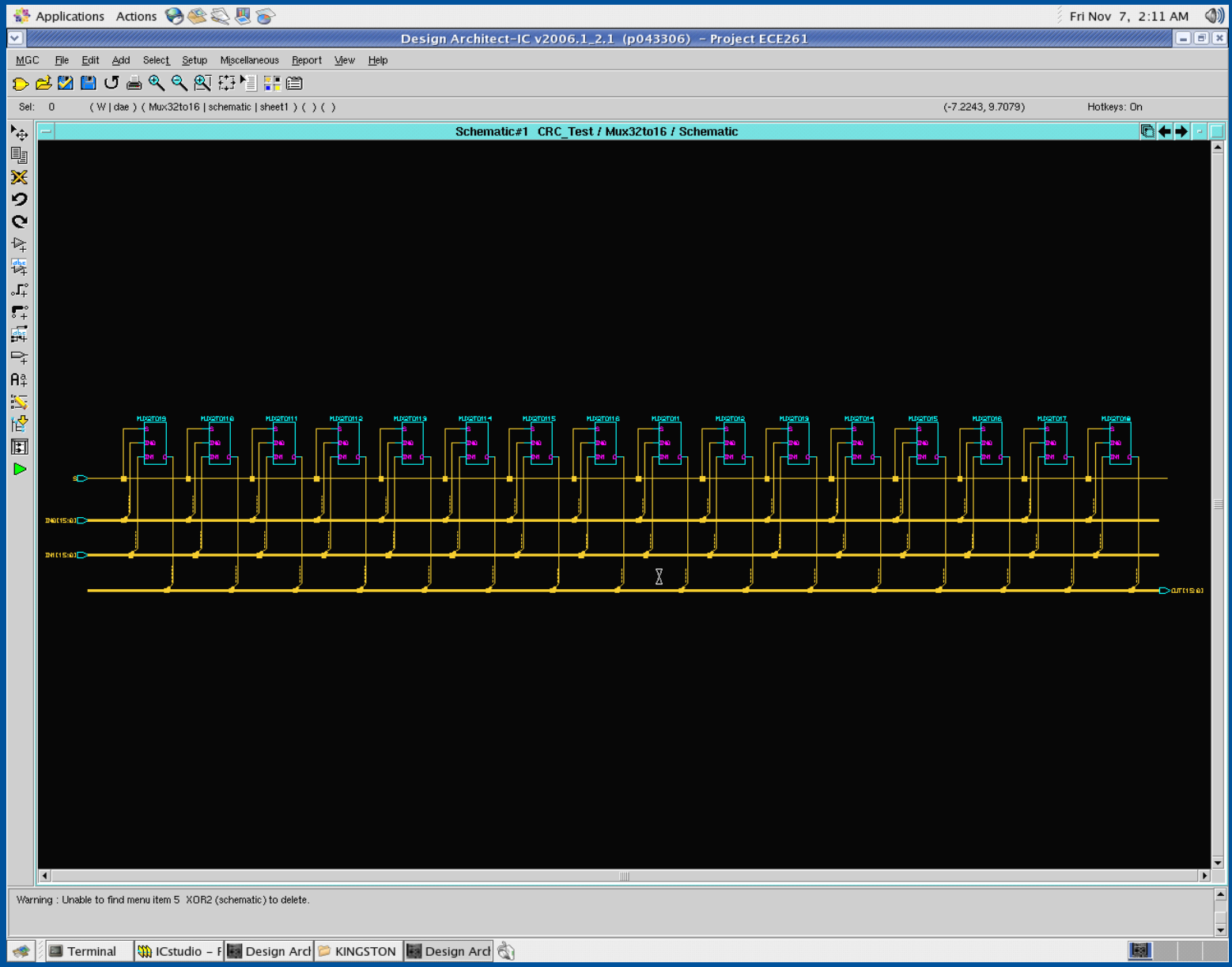
The CRC-Encoder Schematic



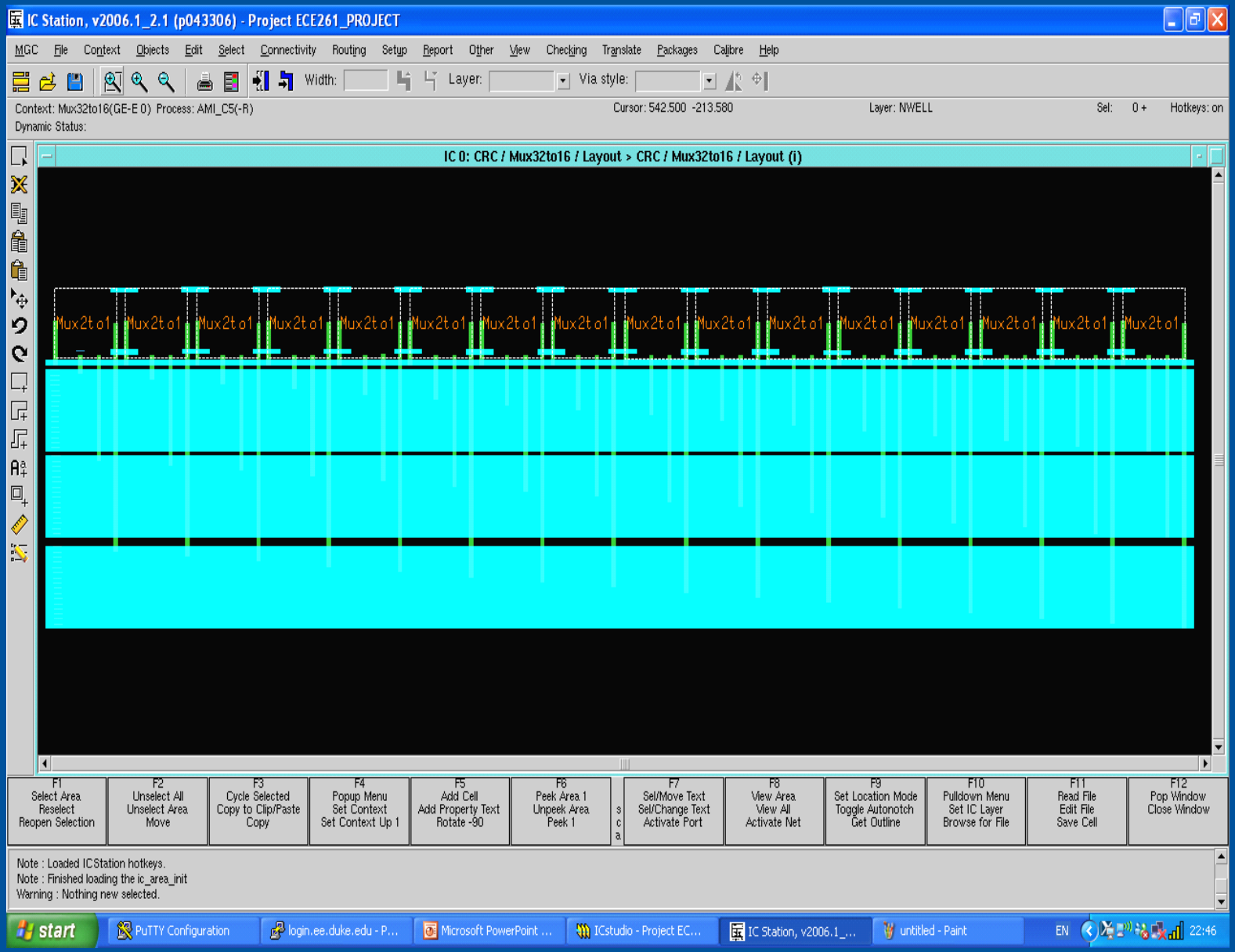
The CRC-Encoder Layout



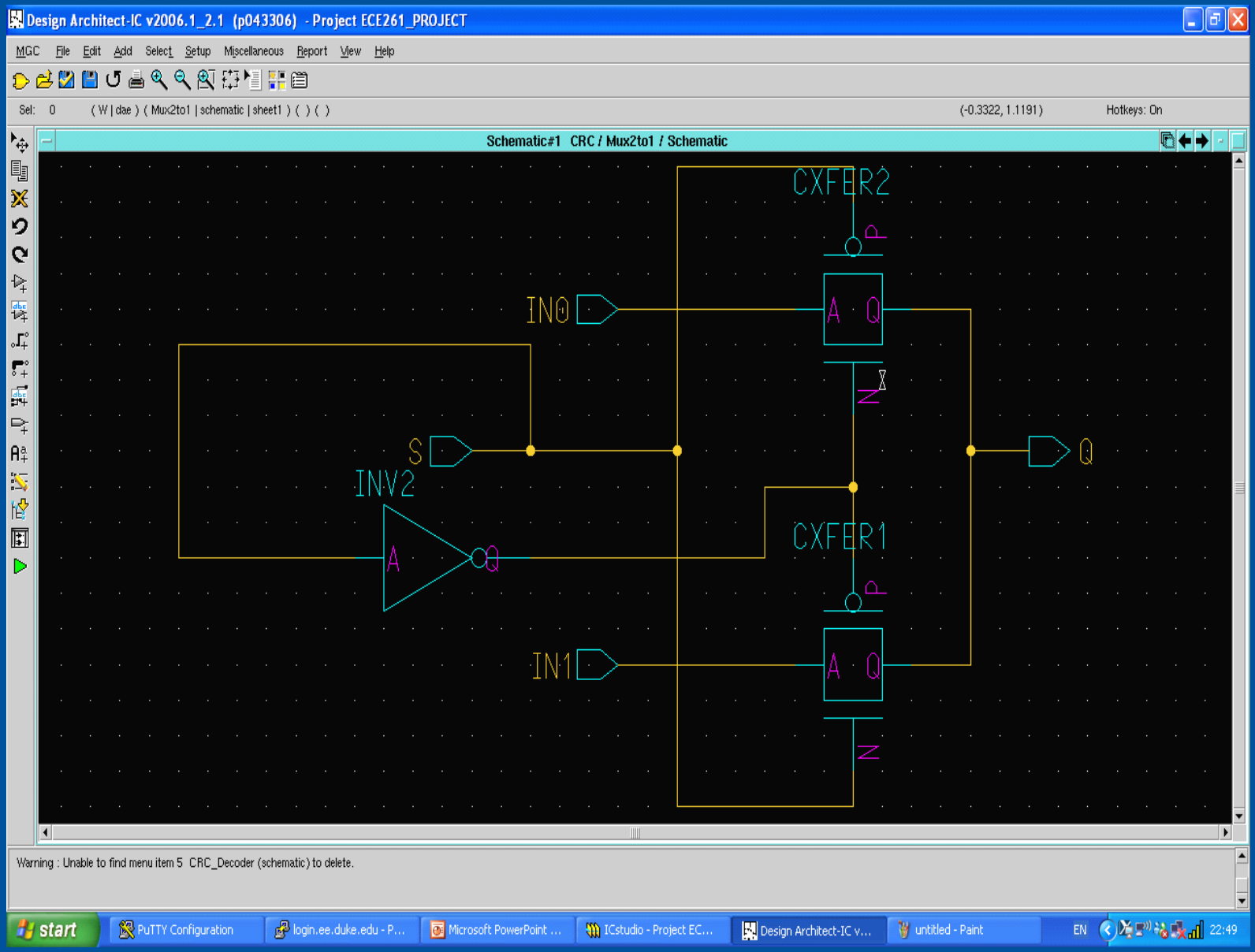
The MUX32to16 Schematic



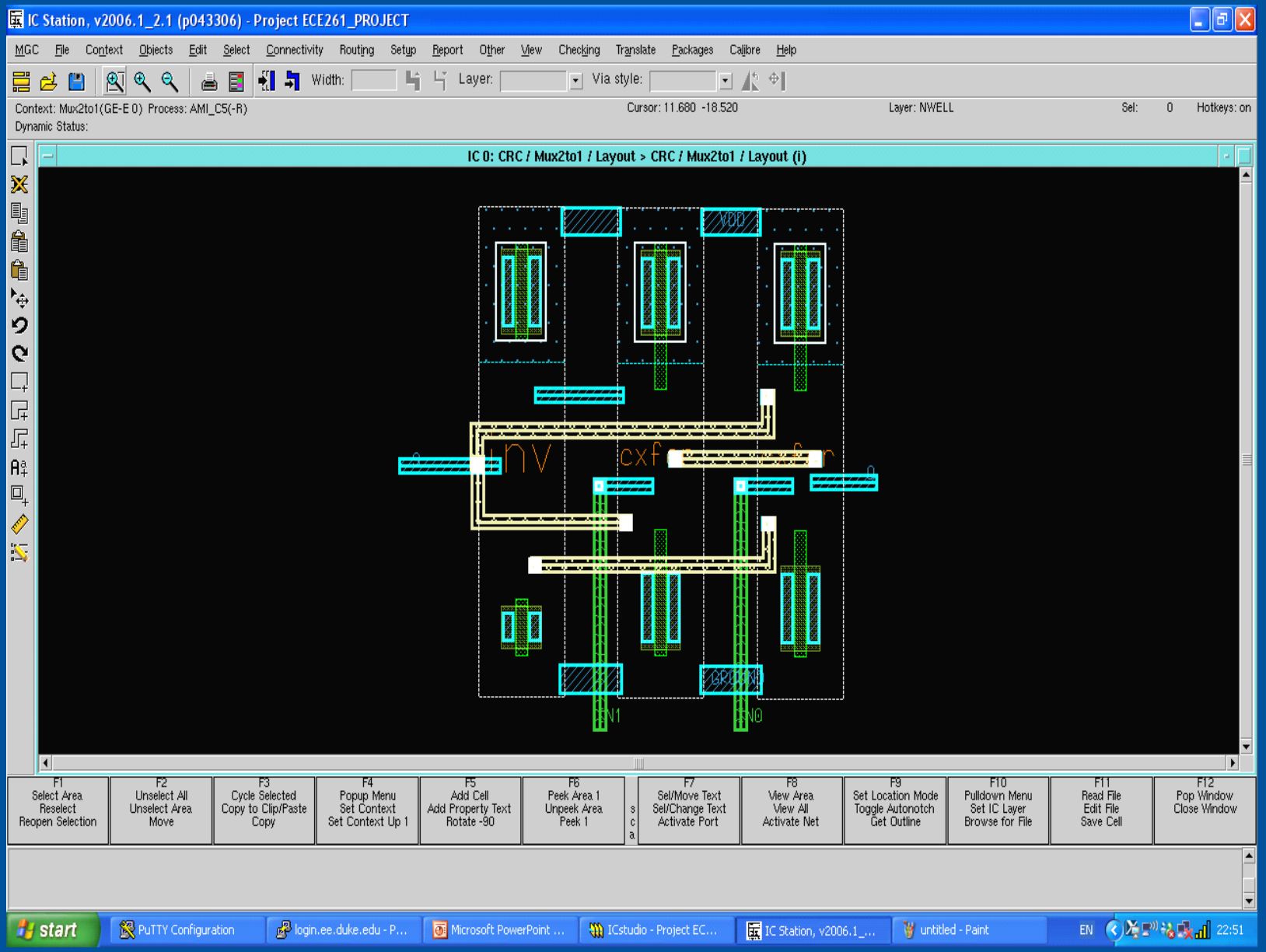
The MUX32to16 Layout



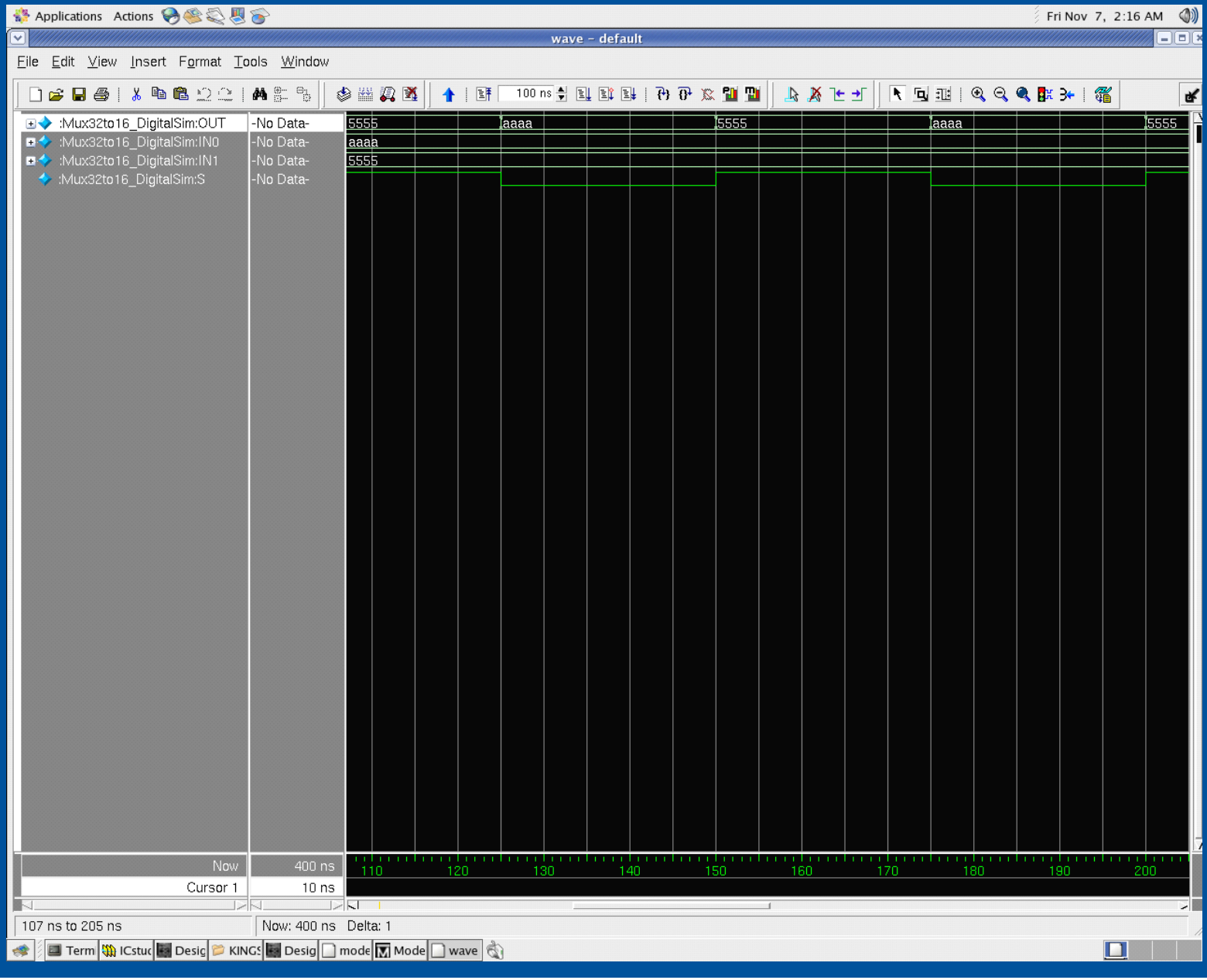
The MUX 2to1 Schematic



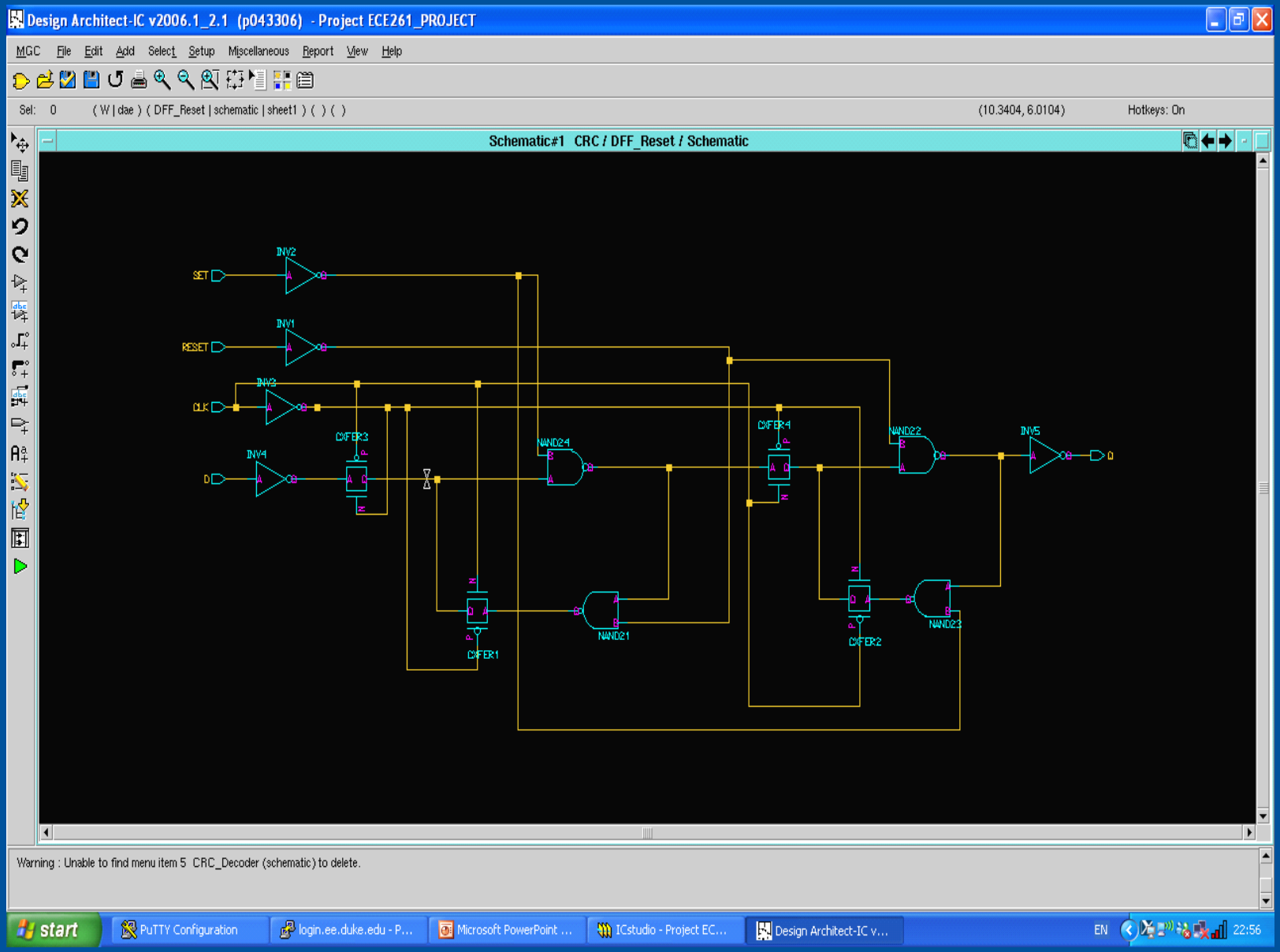
The MUX 2to1 Layout



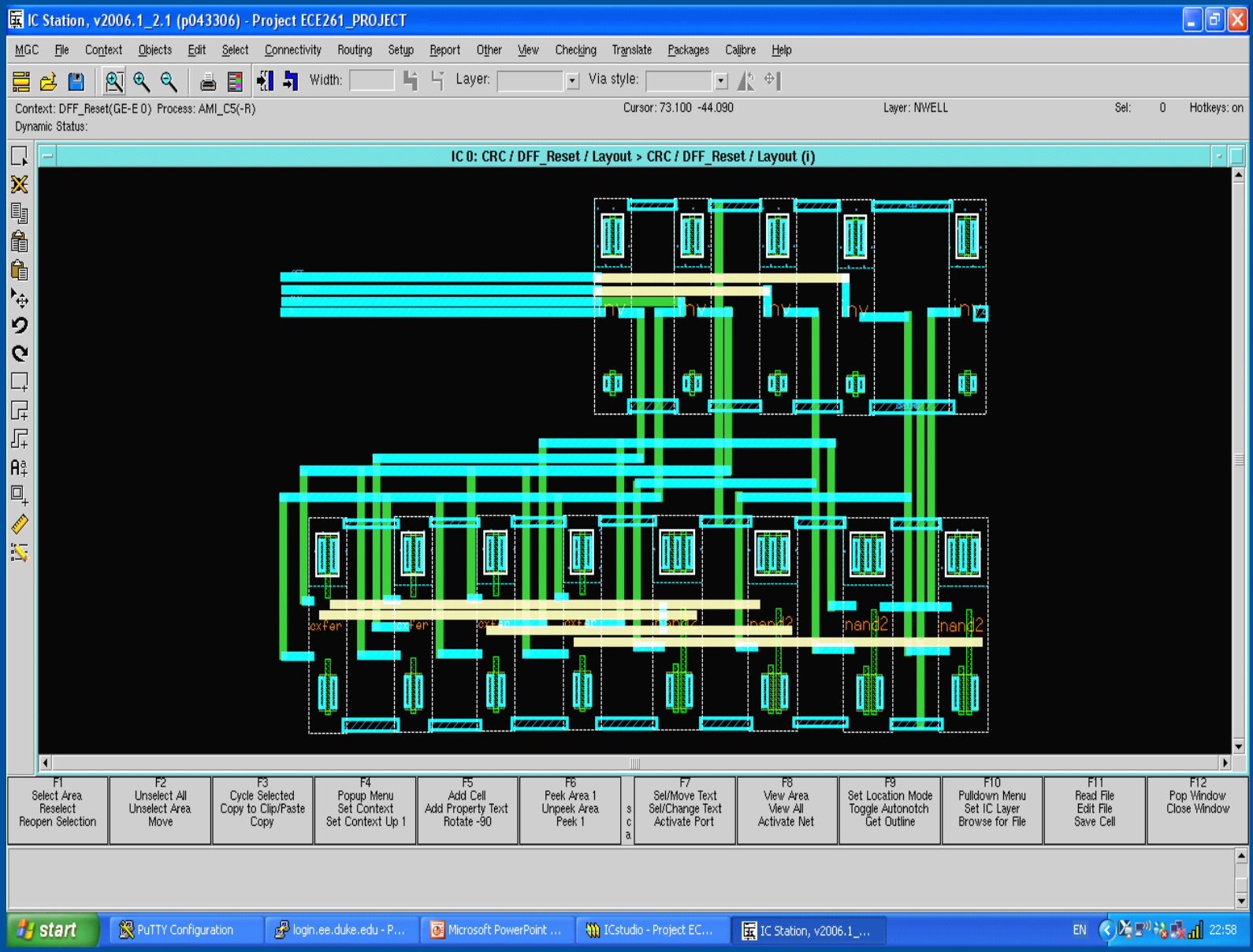
The MUX32to16 Simulation



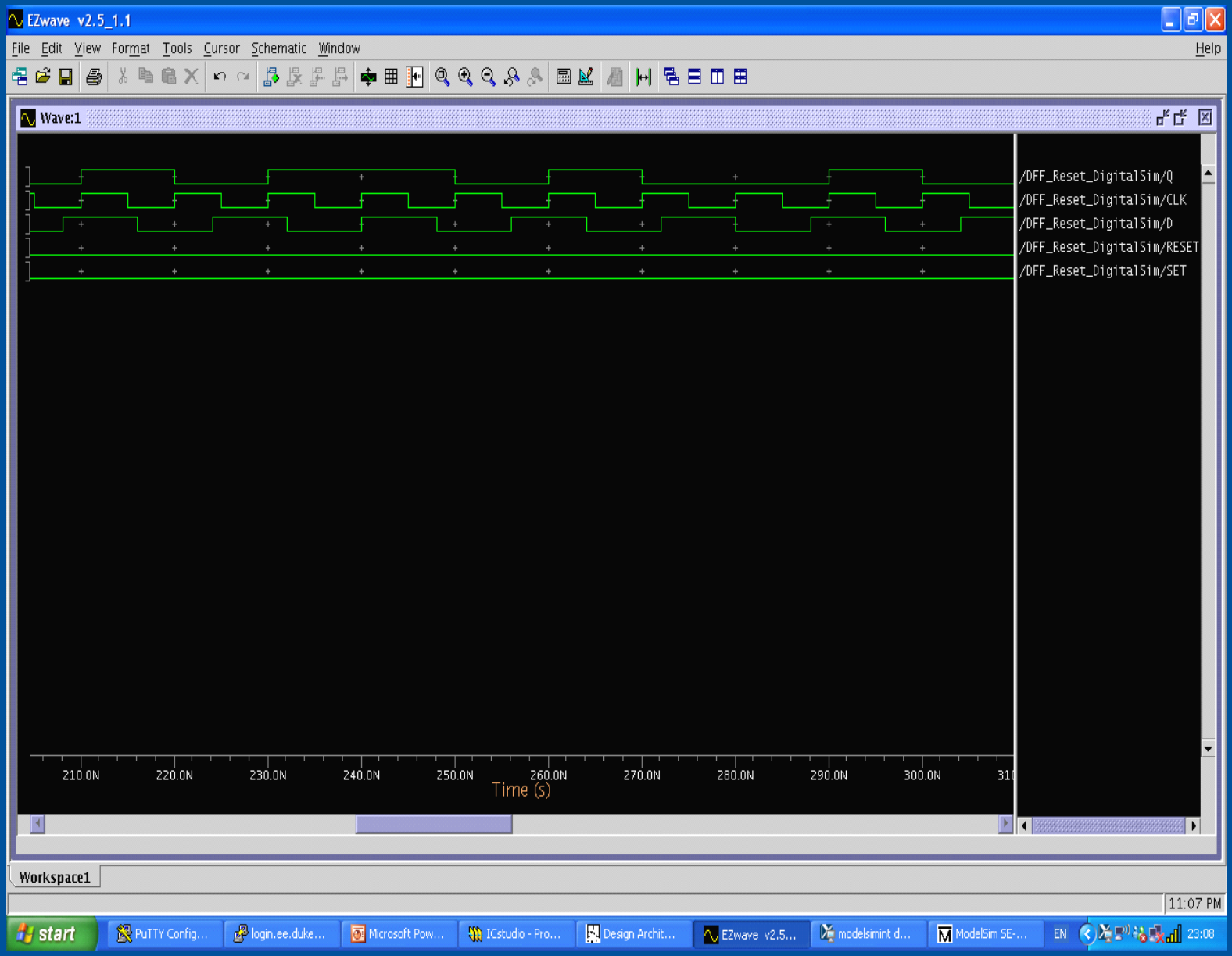
The D Flip Flop Schematic



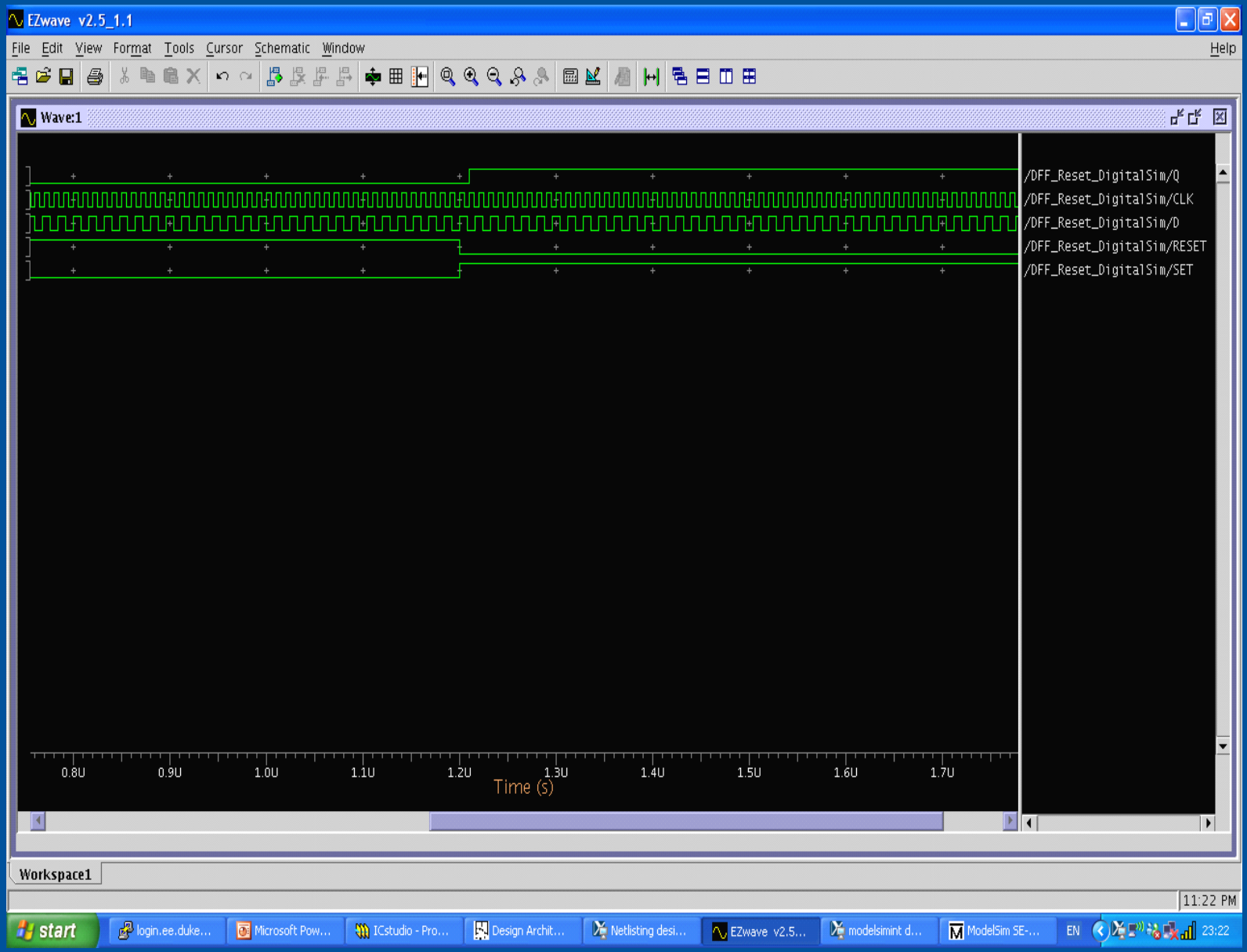
The D Flip Flop Layout



The D Flip Flop Simulation

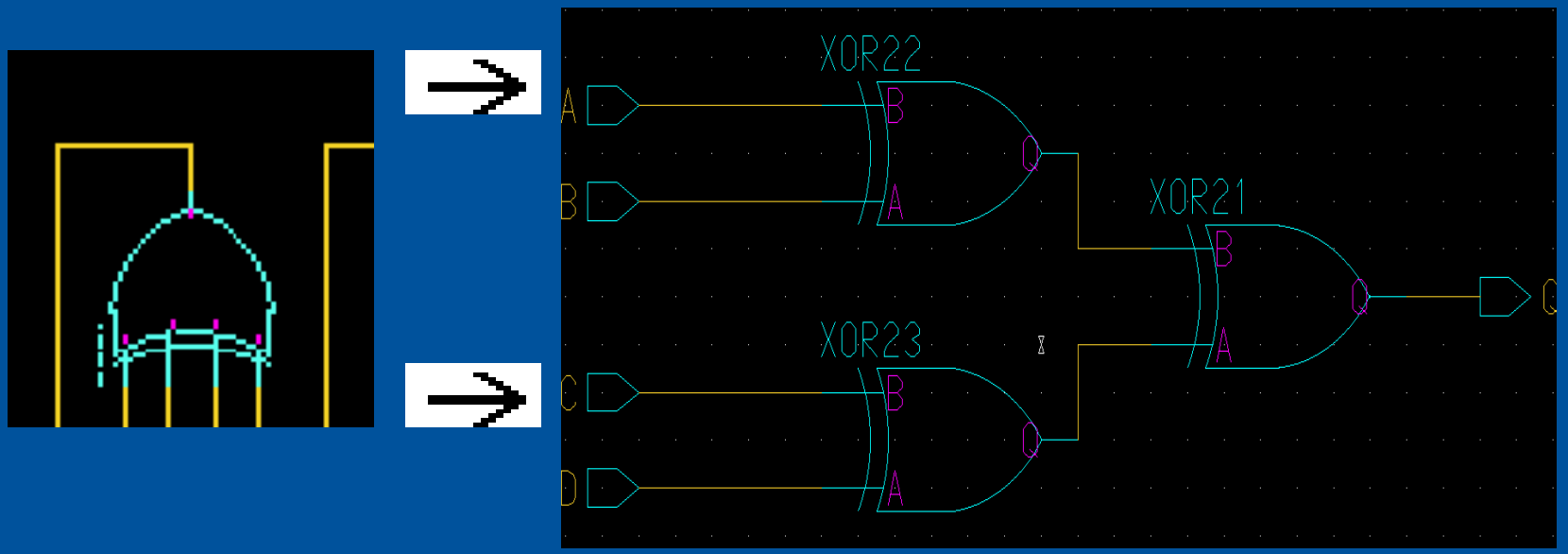


The D Flip Flop Simulation



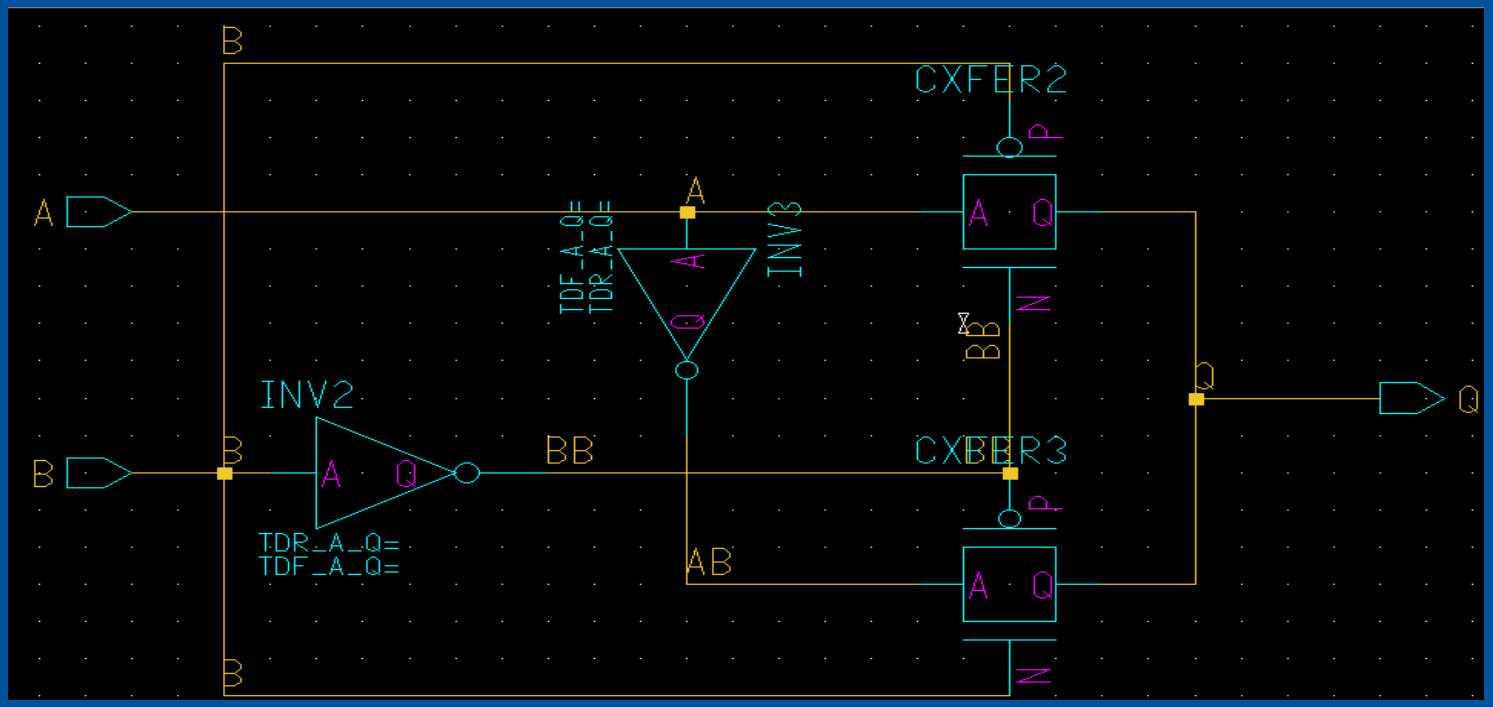
Mutiple Input XOR Gates

- Implementation: For each N input XOR gates, N-1 two-input XOR gates were used
- EX: Four Input XOR is built out of 3 2-input XORs



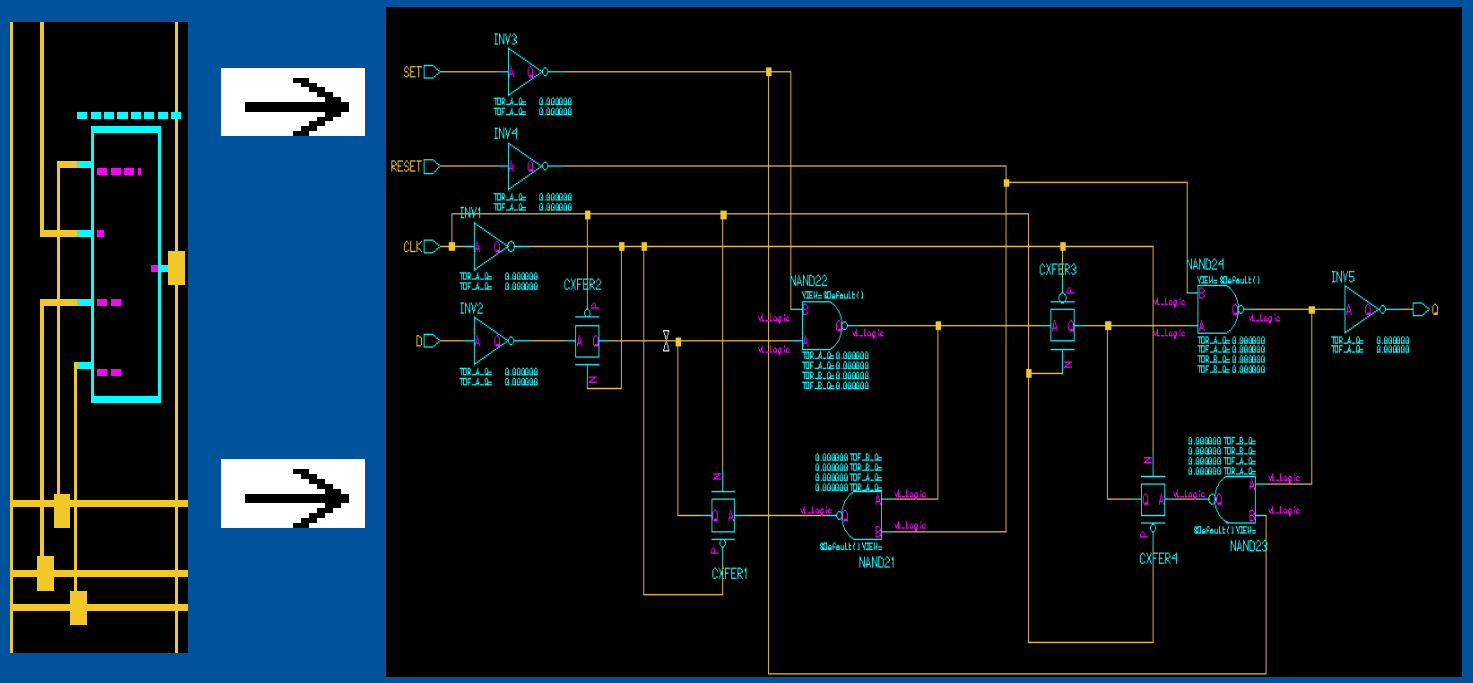
2-Input XOR Gate

- 2-input XOR gate→2 inverters & 2 transmission gates
  →4+4=8 transistors



D Flip Flop

- Implementation: 4* 2-Input NAND gates, 4 transmission gates, 5 inverters

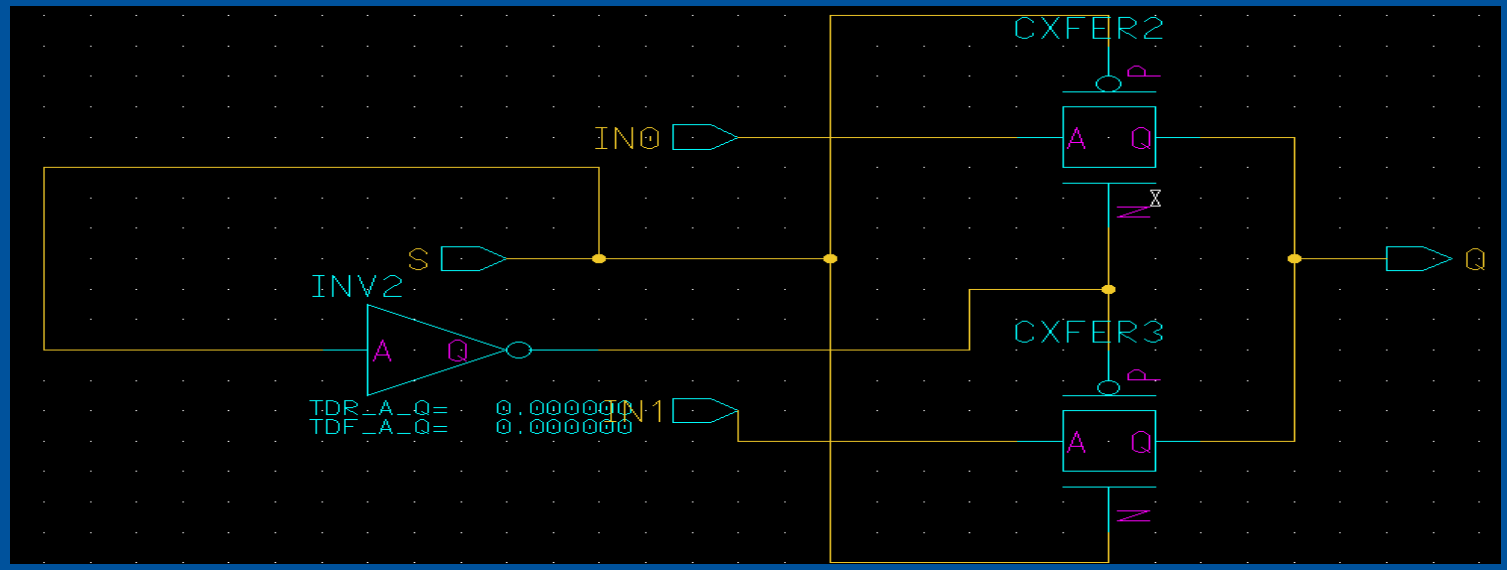


Number of Transistors in CRC

- 3*8-input XOR gates→ 21*2-input XOR gates→21*8=168 transistors
- 1*7-input XOR gates→ 6*2-input XOR gates→ 6*8=48 transistors
- 1*6-input XOR gates→ 5*2-input XOR gates→ 5*8=40 transistors
- 7*5-input XOR gates→ 28*2-input XOR gates→28*8=224 transistors
- 4*4-input XOR gates→ 12*2-input XOR gates→12*8=96 transistors
- 16*2-input XOR gates→ 16*8= 128 transistors
- 4*2-Input NAND gates→ 4*4=16 transistors
- 4 transmission gates → 4*2= 8 transistors
- 5 inverters→ 5*2=10 transistors
- 738 transistors used in the CRC design

Mux Design

- 16 2*1 MUX used:



- 2 transmission gates and 1 inverter in the MUX
- 16*(2*2+2)= 96 transistors used

NOR16 Design

- Four OR4 & One NOR4
- Each OR4= 3 OR2
- Each NOR4= 2 OR2 + 1NOR2
- Total = 14 OR2 & One NOR2

- 14*6+4= 88 transistors used

Total Number of Transistors

- CRC Encoder, CRC Decoder, 16 2*1 MUX
- NOR16 Gate

❖ 738+ 738+ 96+88= 1660 transistors

Power Estimations

- Power Consumption
  - Dynamic Power
    - Assume f = 30 MHz, $\bar{\alpha} = 1$
    - Short circuit Current
      - Not considered – rise/fall times are ideal because we used standard cells.
  - Static Power
    - Ratio Power – Not a factor
    - Leakage – Assume worst case

Power Estimations

- Max Dynamic Power:
  - $P_{dy} = \bar{\alpha} C V_{DD}^2 f = \bar{\alpha} C V_{DD}^2 f = \bar{\alpha} C_g W_g V_{DD}^2 f =$ $(1/2)(2*10^{-15}F/\mu m)(7\mu m)(5V)^2(3*10^7 s^{-1}) =$ 5.3 µW per Transistor.
  - 1,660 Transistors *5.3 µW per Transistor = **8.80 mW**

Power Estimations

- Leakage Power
  - Static Power = Leakage Power = Number of transistors*Leakage power of 1 transistor
  - Pst = Pleak = Ntran*Pleak_1
  - Vdd=3V; W= 6 um;
  - Ileak/W = 6.506 nA/um (Current Leakage per unit width assuming half good devices and half bad devices)
  - Ileak = W*Ileak/W = 39 nA;
  - **Pst = Ntran*Vdd*Ileak = 0.194 mW**;