



16-bit Parallel Input CRC

Baris Piyade

Chi Zhang

Matthew Roberts



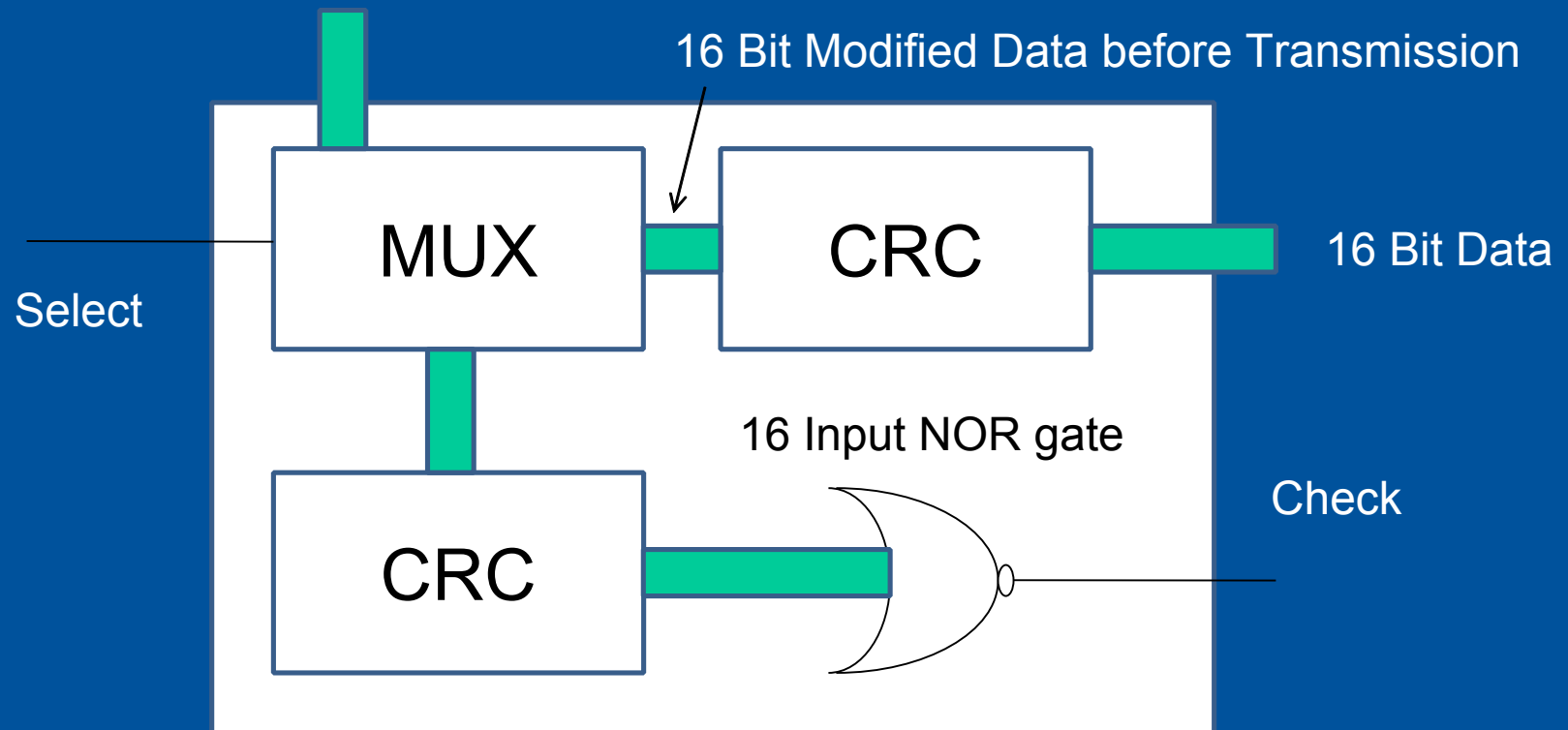
Abstract

This device is meant to mimic the operations of a 16-bit CRC checker. It contains a CRC block which encodes the 16-bit input and another which decodes it as well as a MUX and a 16-input NOR gate. The MUX selects whether you send the unmodified data through the decoder or a modified set of data. The modified data (DATA_M) is meant to represent corrupted data (i.e. data where one or more bits have been changed due to a lossy transmission line such as the path between 2 RF devices). If the unmodified data (DATA) is sent through the MUX, the output of the decoder should be all zeros which will cause the NOR gate to output a 1. If the modified data is sent through, the NOR gate should output a zero indicating that there has been data corruption.

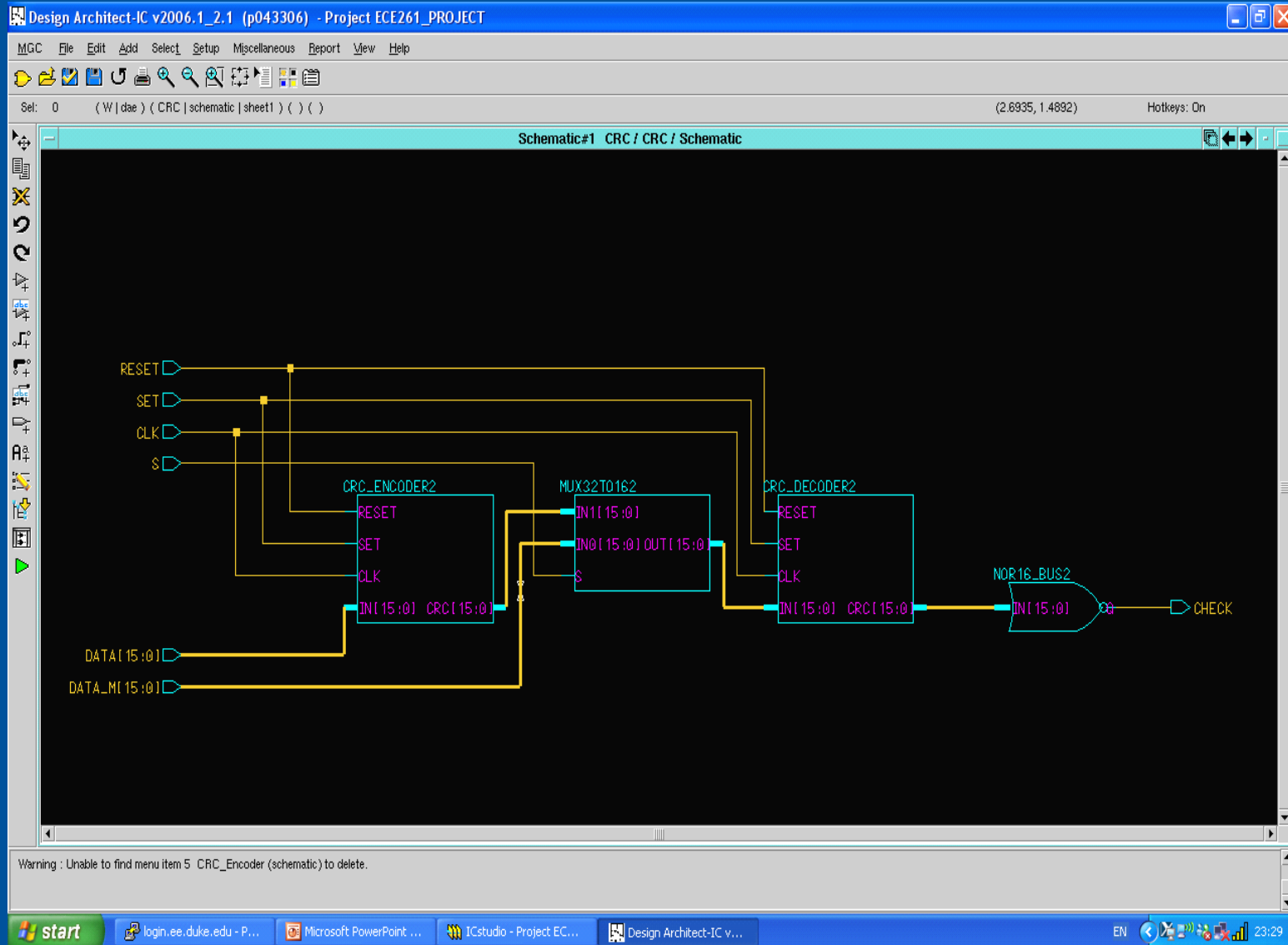
Block Diagram



16 Bit Modified Data after Transmission



The CRC Schematic



The CRC Simulation

The screenshot displays the Design Architect-IC v2006.1_2.1 software interface. The title bar reads "Design Architect-IC v2006.1_2.1 (p043306) - Project ECE261_PROJECT". The menu bar includes "MGC", "File", "Edit", "Apld", "Select", "Setup", "Miscellaneous", "Report", "View", and "Help". The status bar shows "Sel: 0", "(W | dae) (CRC_DSim | schematic | sheet1) () ()", and coordinates "(-0.8017, -0.6882)".

The main workspace, titled "Schematic#1 CRC / CRC_DSim / Schematic", shows a schematic diagram for a CRC2 component. The component is represented by a central box with the label "CRC2" above it. The inputs and outputs are as follows:

- Inputs (left side):
 - CLK (yellow) connected to CLK (magenta)
 - S (yellow) connected to S (magenta)
 - SET (yellow) connected to SET (magenta)
 - RESET (yellow) connected to RESET (magenta)
 - DATA_M[15:0] (yellow) connected to DATA_M[15:0] (magenta)
 - DATA[15:0] (yellow) connected to DATA[15:0] (magenta)
- Output (right side):
 - CHECK (magenta) connected to CHECK (yellow)

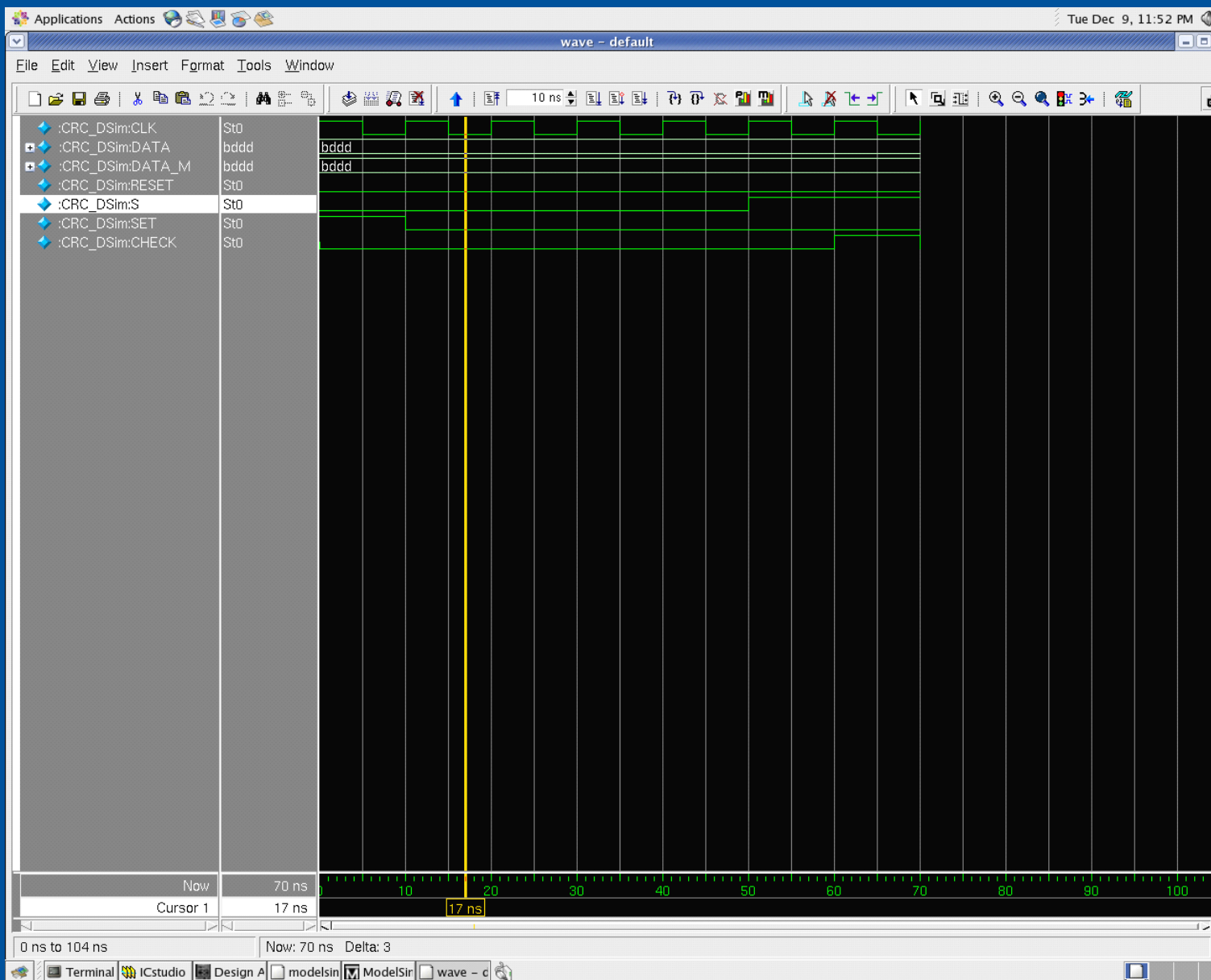
A warning message at the bottom of the workspace reads: "Warning : Unable to find menu item 5 CRC_DSim (schematic) to delete." The Windows taskbar at the bottom shows the Start button and several open applications: "login.ee.duke.edu - P...", "Microsoft PowerPoint ...", "ICStudio - Project EC...", and "Design Architect-IC v...". The system tray on the right shows "EN", network and volume icons, and the time "23:33".



The CRC Simulation

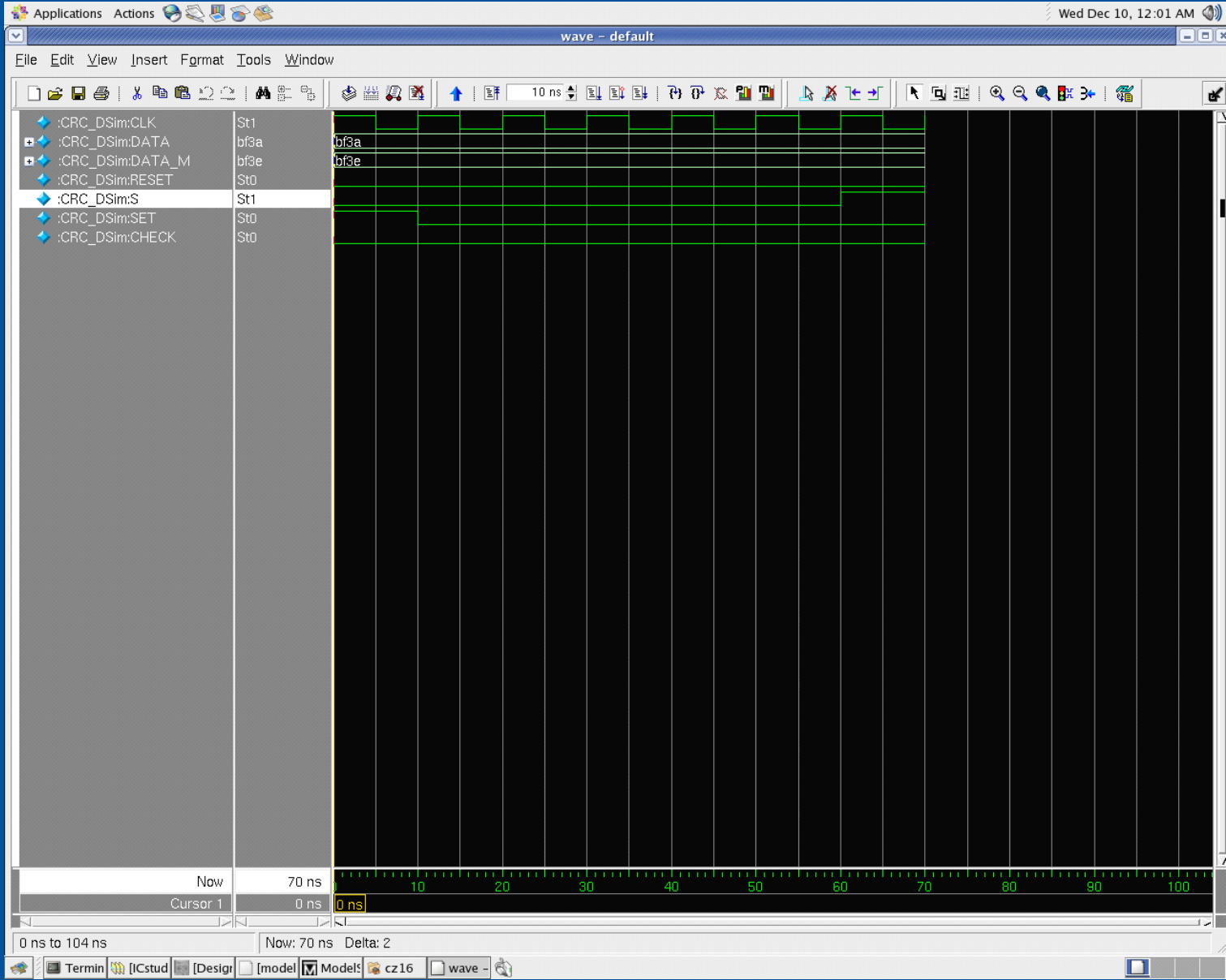
The CRC simulation demonstrates that when "DATA" is passed through the MUX (which represents uncorrupted data) the Check output is 1. When "DATA_M" is passed and it is not identical to the CRC encoder output (which represents corrupted data), the Check output is zero

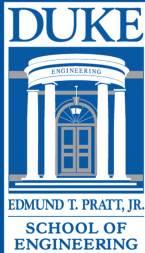
The CRC Simulation





The CRC Simulation





The CRC Top Level Layout

IC Station, v2006.1_2.1 (p043306) - Project ECE261_PROJECT

MGC File Context Objects Edit Select Connectivity Routing Setup Report Other View Checking Translate Packages Calibre Help

Context: CRC(GE-E-D) Process: AMI_C5(-R) Cursor: 2477.740 247.310 Layer: NWELL Set: 0+ Hotkeys: on

IC 0: CRC / CRC / Layout > CRC / CRC / Layout (I)

IC Palettes

- Easy Edit
- Edit
- Expert Edit
- CE/CBC Edit
- DLA Layout
- DLA Device
- ECD
- IC Session
- ICRules
- Instant DRC
- Short Checker
- ICtrace (D)
- ICtrace (M)
- Verifdip (DRC)
- Verifdip (LVS)
- ICAssemble
- Plan & Place
- Route
- ICBlocks
- Floorplan
- Place & Route

F1 Select Area Reselect Reopen Selection	F2 Unselect All Unselect Area Move	F3 Cycle Selected Copy to Clip/Paste Copy	F4 Popup Menu Set Context Set Context Up 1	F5 Add Cell Add Property Text Rotate -90	F6 Peek Area 1 Unpeek Area Peek 1	F7 Sel/Move Text Sel/Change Text Activate Port	F8 View Area View All Activate Net	F9 Set Location Mode Toggle Autonotch Get Outline	F10 Pulldown Menu Set IC Layer Browse for File	F11 Read File Edit File Save Cell	F12 Pop Window Close Window
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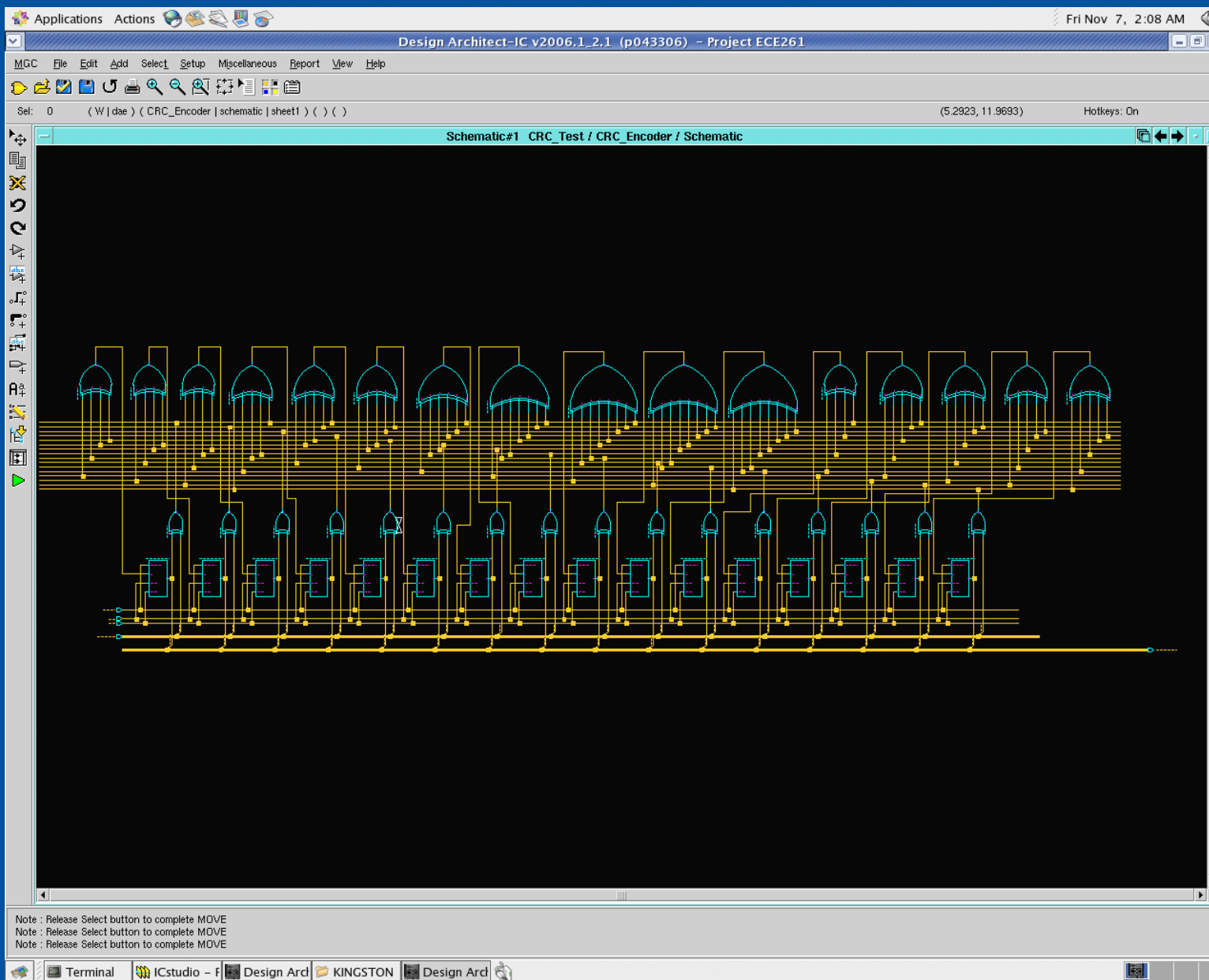
Note : Euclidean = 1814.67, Manhattan = 1814.67, X distance = 0, Y distance = 1814.67
Note : Add Ruler: Specify line with left mouse button.
Warning : Nothing unselected in the active context.

Terminal ICStudio - Proj Design Archtec IC Station, v200

$$\text{Area} = 1.8\text{mm} * 3\text{mm} = 5.4\text{mm}^2$$



The CRC-Encoder Schematic





The CRC-Encoder Layout

IC Station, v2006.1_2.1 (p043306) - Project ECE261_PROJECT

MGC File Context Objects Edit Select Connectivity Routing Setup Report Other View Checking Translate Packages Calibre Help

Width: Layer: Via style:

Context: CRC_Decoder(GE-E D) Process: AML_C5(-R) Cursor: 1939.420 652.240 Layer: NWELL Sel: 0+ Hotkeys: on
Dynamic Status:

IC 0: CRC / CRC_Decoder / Layout > CRC / CRC_Decoder / Layout (i)

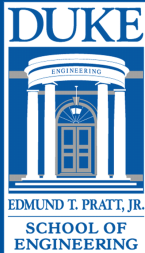
XOR4 XOR4 XOR4 XOR5 XOR5 XOR5 XOR6 XOR7 XOR8 XOR8 XOR8 XOR4 XOR5 XOR5 XOR5 XOR5

DFF_Reset DFF_Reset DFF_Reset DFF_Reset DFF_Reset DFF_Reset DFF_Reset DFF_Reset DFF_Reset DFF_Reset DFF_Reset DFF_Reset DFF_Reset DFF_Reset DFF_Reset DFF_Reset

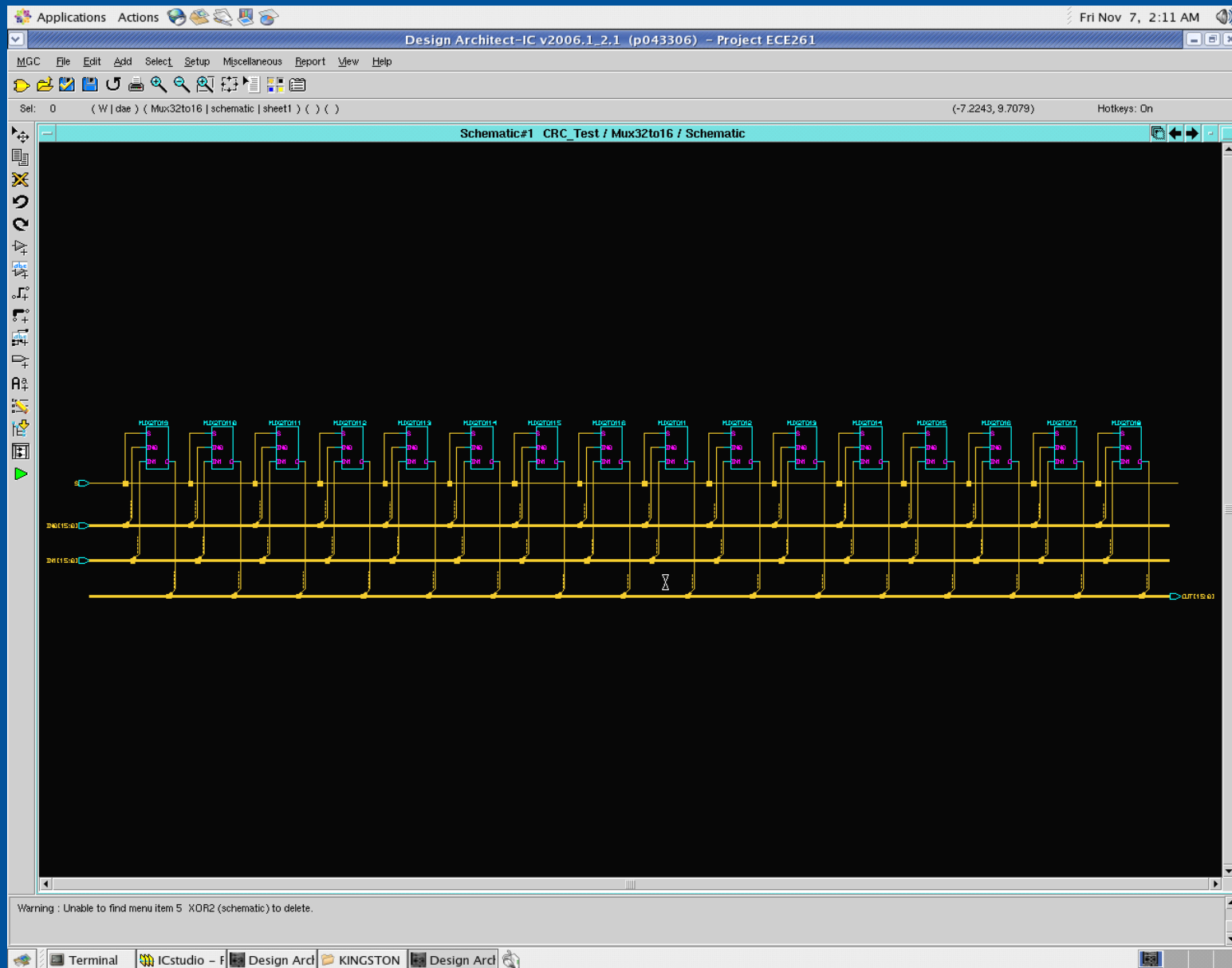
F1 Select Area Reselect Reopen Selection	F2 Unselect All Unselect Area Move	F3 Cycle Selected Copy to Clip/Paste Copy	F4 Popup Menu Set Context Set Context Up 1	F5 Add Cell Add Property Text Rotate -90	F6 Peek Area 1 Unpeek Area Peek 1	F7 Sel/Move Text Sel/Change Text Activate Port	F8 View Area View All Activate Net	F9 Set Location Mode Toggle Autonotch Get Outline	F10 Pulldown Menu Set IC Layer Browse for File	F11 Read File Edit File Save Cell	F12 Pop Window Close Window
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Note : Finished loading the ic_area_init
Note : 171 shapes + 376 paths + 48 instances + 38 texts + 435 via_objects + 112 pins are selected.
Warning : Nothing new selected.

start PuTTY Configurat... login.ee.duke.ed... Microsoft PowerP... ICstudio - Project... IC Station, v2006... Document1 - Micr... untitled - Paint EN 22:43



The MUX32to16 Schematic





The MUX32to16 Layout

IC Station, v2006.1_2.1 (p043306) - Project ECE261_PROJECT

MGC File Context Objects Edit Select Connectivity Routing Setup Report Other View Checking Translate Packages Calibre Help

Width: Layer: Via style:

Context: Mux32to16(GE-E D) Process: AML_C5(-R) Cursor: 542.500 -213.580 Layer: NWELL Sel: 0+ Hotkeys: on
Dynamic Status:

IC 0: CRC / Mux32to16 / Layout > CRC / Mux32to16 / Layout (i)

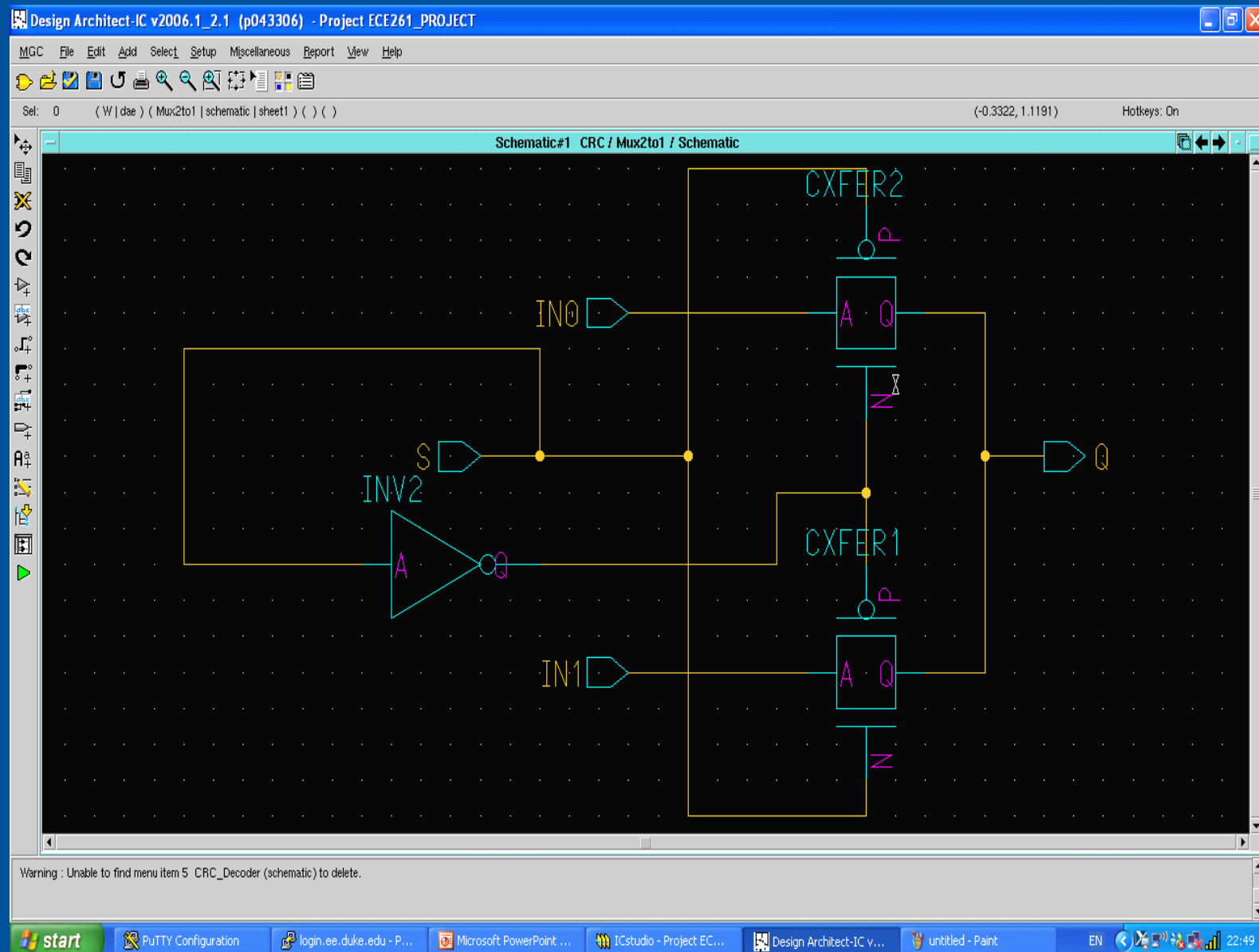
Mux2to1 Mux2to1 Mux2to1 Mux2to1 Mux2to1 Mux2to1 Mux2to1 Mux2to1 Mux2to1 Mux2to1 Mux2to1 Mux2to1 Mux2to1 Mux2to1 Mux2to1 Mux2to1

F1 Select Area Reselect Reopen Selection	F2 Unselect All Unselect Area Move	F3 Cycle Selected Copy to Clip/Paste Copy	F4 Popup Menu Set Context Set Context Up 1	F5 Add Cell Add Property Text Rotate -90	F6 Peek Area 1 Unpeek Area Peek 1	F7 Sel/Move Text Sel/Change Text Activate Port	F8 View Area View All Activate Net	F9 Set Location Mode Toggle Autonotch Get Outline	F10 Pulldown Menu Set IC Layer Browse for File	F11 Read File Edit File Save Cell	F12 Pop Window Close Window
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Note : Loaded ICStation hotkeys.
Note : Finished loading the ic_area_init
Warning : Nothing new selected.

start PuTTY Configuration login.ee.duke.edu - P... Microsoft PowerPoint ... ICstudio - Project EC... IC Station, v2006.1_... untitled - Paint EN 22:46

The MUX 2to1 Schematic





The MUX 2to1 Layout

IC Station, v2006.1_2.1 (p043306) - Project ECE261_PROJECT

MGC File Context Objects Edit Select Connectivity Routing Setup Report Other View Checking Translate Packages Calibre Help

Width: Layer: Via style:

Context: Mux2to1(GE-E 0) Process: AMI_C5(-R) Cursor: 11.680 -18.520 Layer: NWELL Set: 0 Hotkeys: on

Dynamic Status:

IC 0: CRC / Mux2to1 / Layout > CRC / Mux2to1 / Layout (i)

F1 Select Area
Reselect
Reopen Selection

F2 Unselect All
Unselect Area
Move

F3 Cycle Selected
Copy to Clip/Paste
Copy

F4 Popup Menu
Set Context
Set Context Up 1

F5 Add Cell
Add Property Text
Rotate -90

F6 Peek Area 1
Unpeek Area
Peek 1

F7 Sel/Move Text
Sel/Change Text
Activate Port

F8 View Area
View All
Activate Net

F9 Set Location Mode
Toggle Autonotch
Get Outline

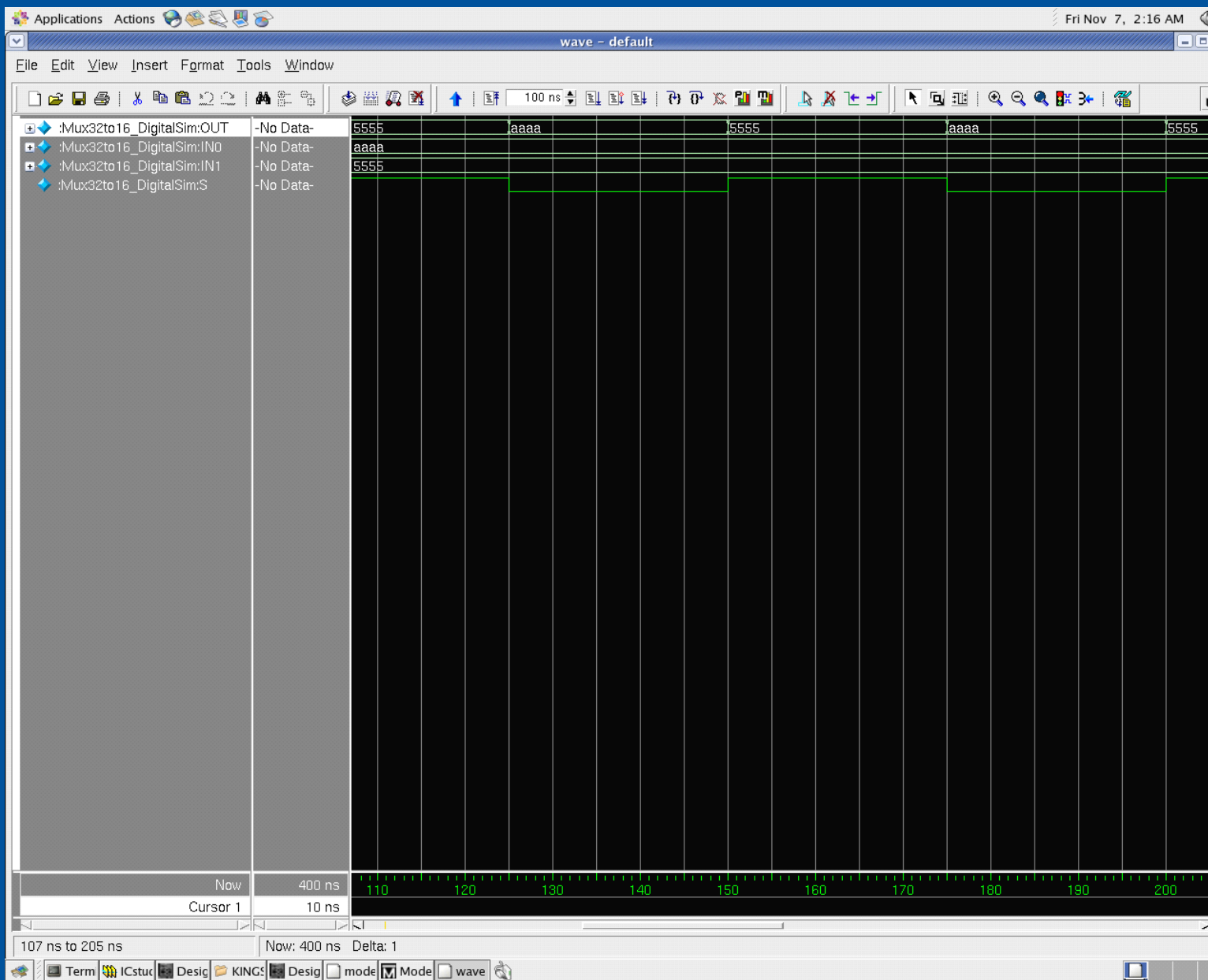
F10 Pulldown Menu
Set IC Layer
Browse for File

F11 Read File
Edit File
Save Cell

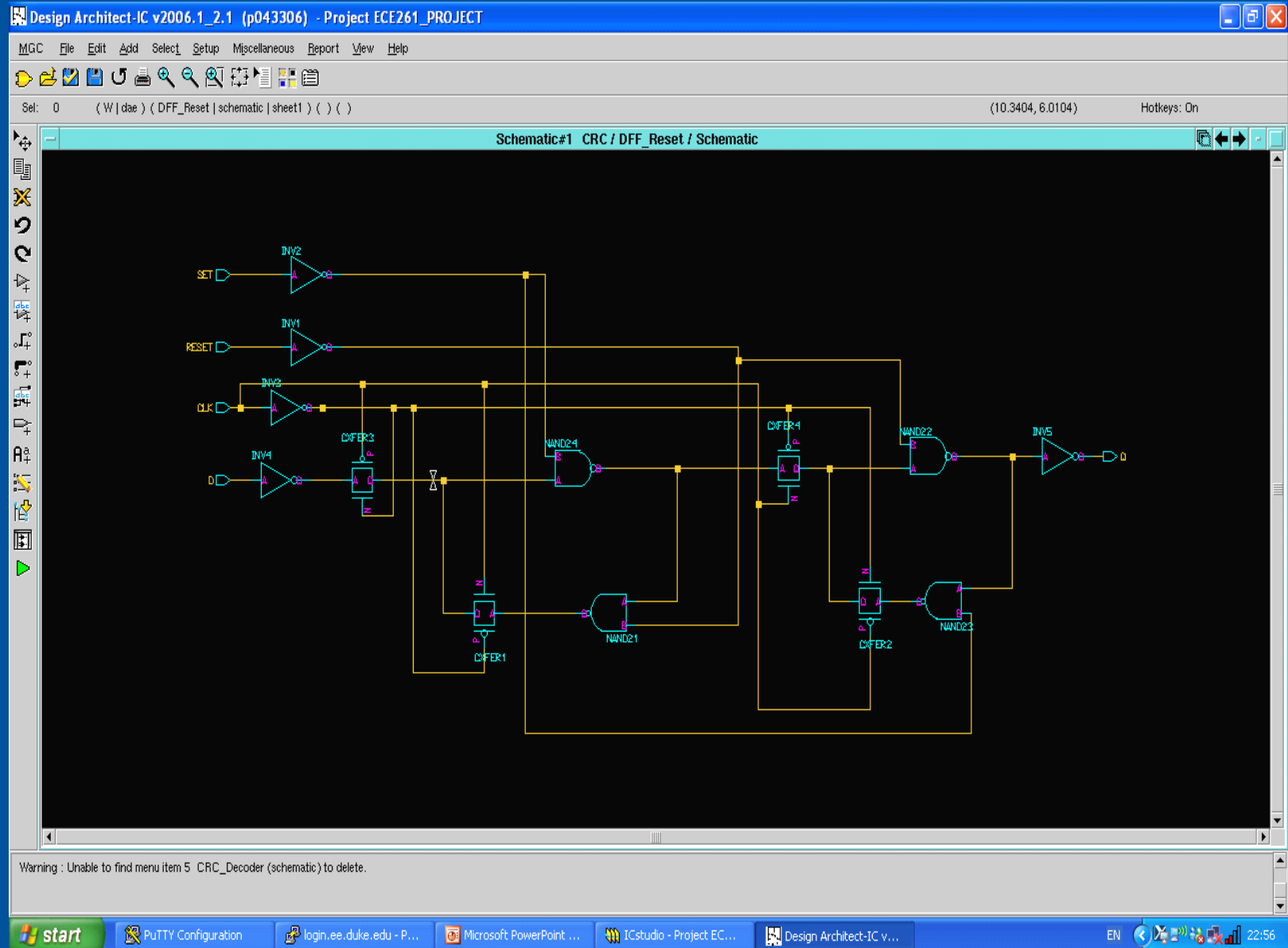
F12 Pop Window
Close Window

start PUTTY Configuration login.ee.duke.edu - P... Microsoft PowerPoint ... ICstudio - Project EC... IC Station, v2006.1_... untitled - Paint EN 22:51

The MUX32to16 Simulation



The D Flip Flop Schematic





The D Flip Flop Layout

IC Station, v2006.1_2.1 (p043306) - Project ECE261_PROJECT

MGC File Context Objects Edit Select Connectivity Routing Setup Report Other View Checking Translate Packages Calibre Help

Width: Layer: Via style:

Context: DFF_Reset(GE-E0) Process: AML_C5(-R) Cursor: 73.100 -44.090 Layer: NWELL Sel: 0 Hotkeys: on
Dynamic Status:

IC 0: CRC / DFF_Reset / Layout > CRC / DFF_Reset / Layout (i)

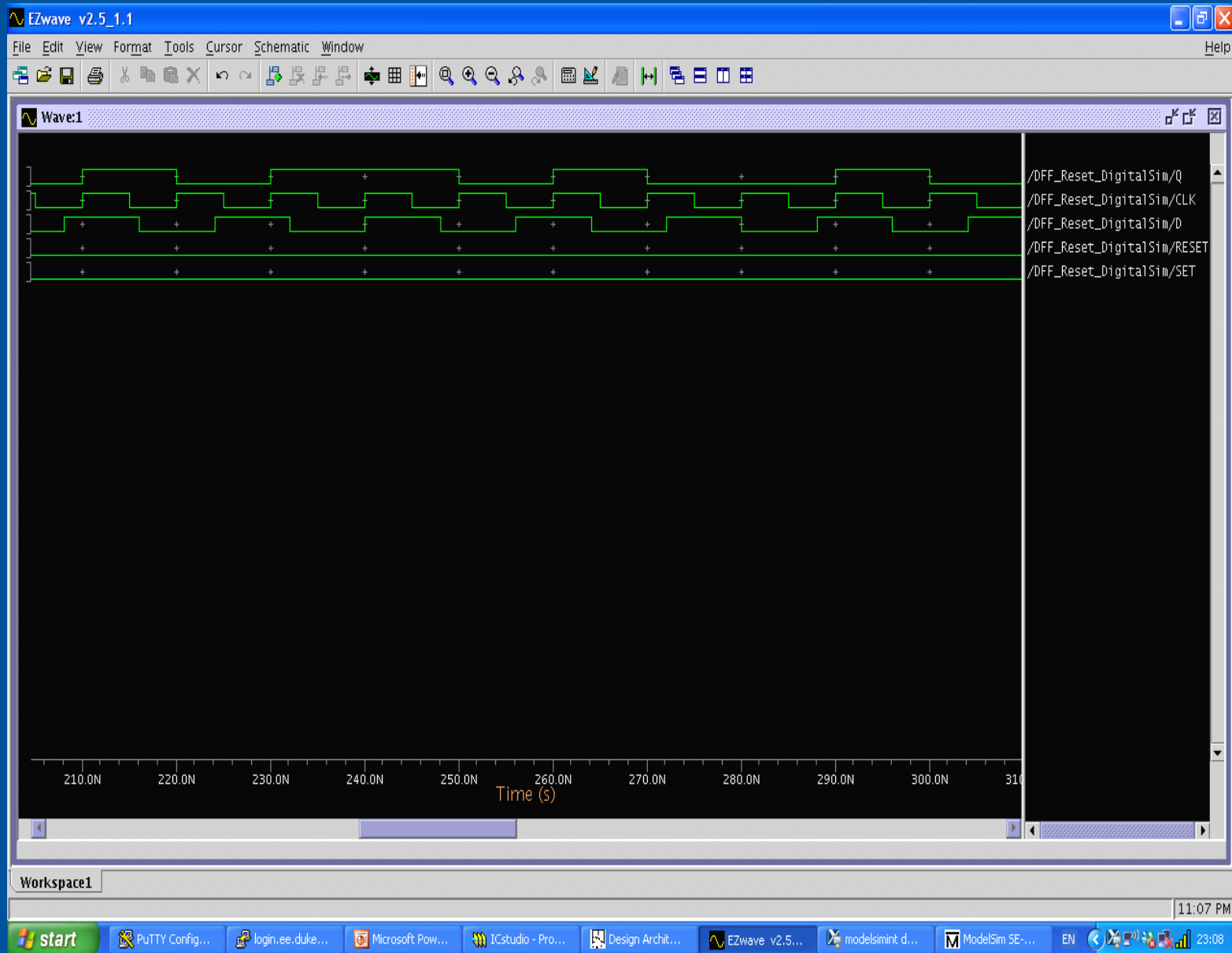
The diagram shows a top-down layout of a D flip flop circuit. It features two rows of flip flops, each with associated routing tracks in cyan and green. Labels like 'nv', 'nand2', and 'xorPar' are visible on the routing. The layout is contained within a window titled 'IC 0: CRC / DFF_Reset / Layout > CRC / DFF_Reset / Layout (i)'.

F1 Select Area Reselect Reopen Selection	F2 Unselect All Unselect Area Move	F3 Cycle Selected Copy to Clip/Paste Copy	F4 Popup Menu Set Context Set Context Up 1	F5 Add Cell Add Property Text Rotate -90	F6 Peek Area 1 Unpeek Area Peek 1	F7 Sel/Move Text Sel/Change Text Activate Port	F8 View Area View All Activate Net	F9 Set Location Mode Toggle Autonotch Get Outline	F10 Pulldown Menu Set IC Layer Browse for File	F11 Read File Edit File Save Cell	F12 Pop Window Close Window
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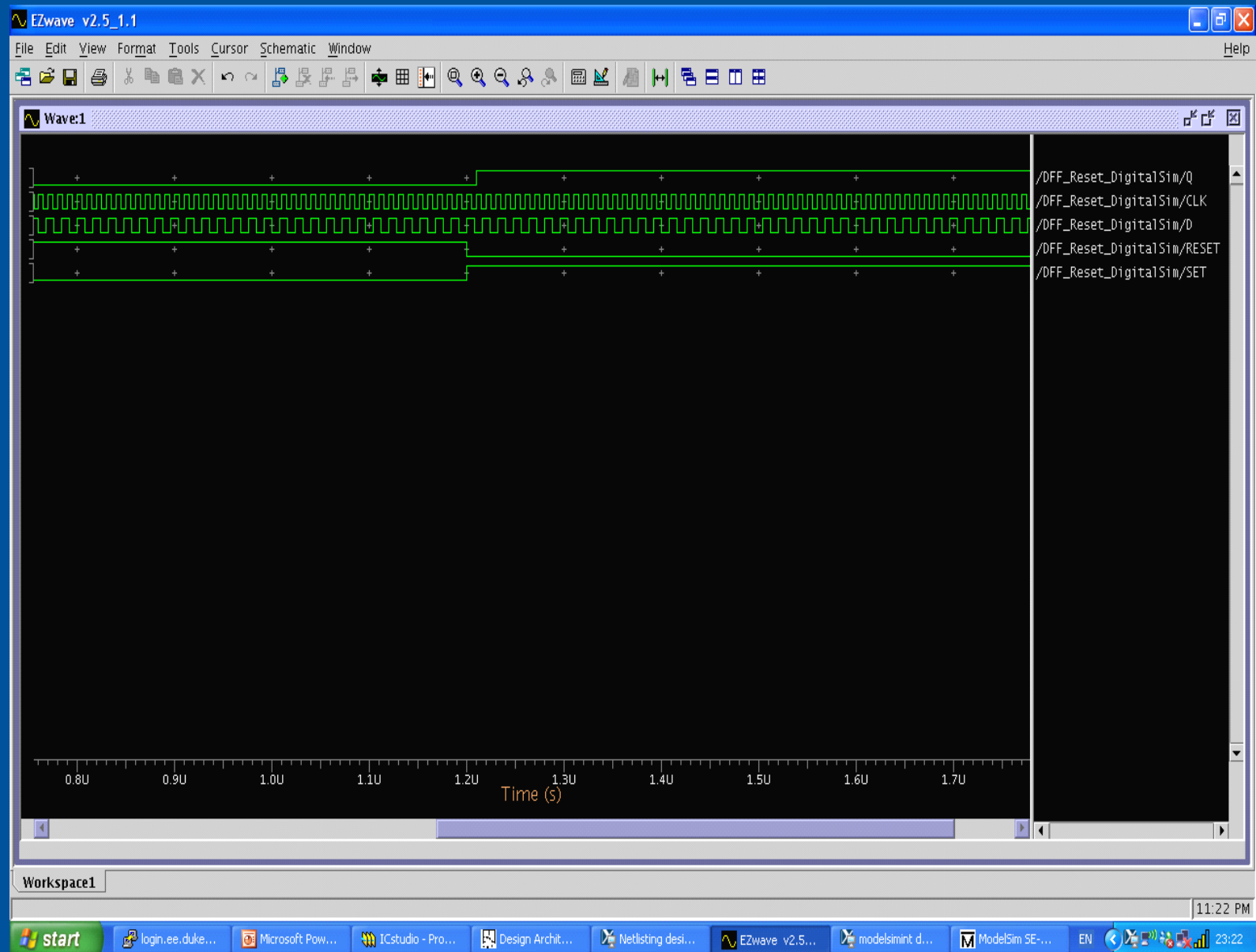
start PuTTY Configuration login.ee.duke.edu - P... Microsoft PowerPoint ... ICstudio - Project EC... IC Station, v2006.1_... EN 22:58



The D Flip Flop Simulation

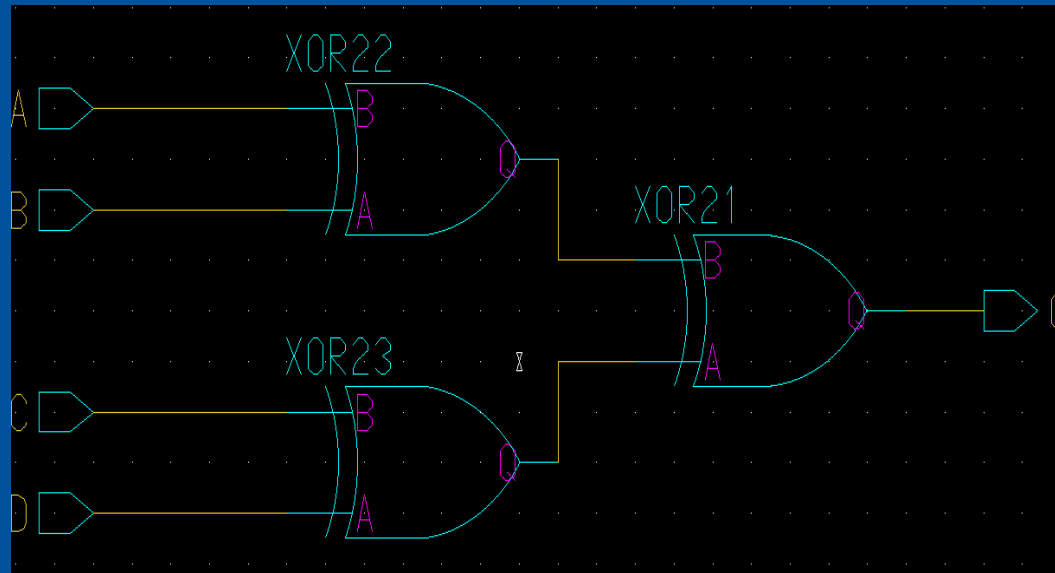
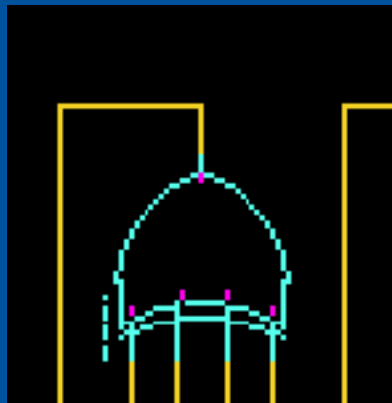


The D Flip Flop Simulation



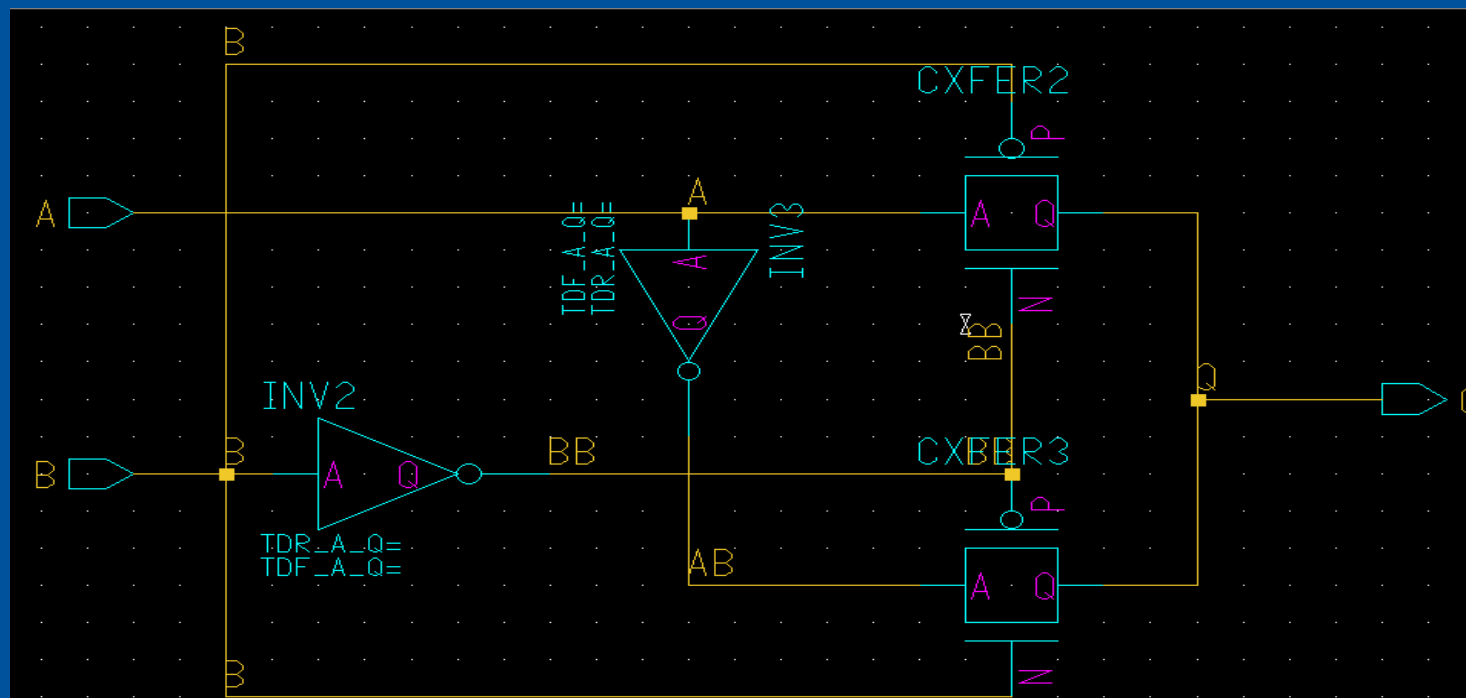
Multiple Input XOR Gates

- Implementation: For each N input XOR gates, N-1 two-input XOR gates were used
- EX: Four Input XOR is built out of 3 2-input XORs



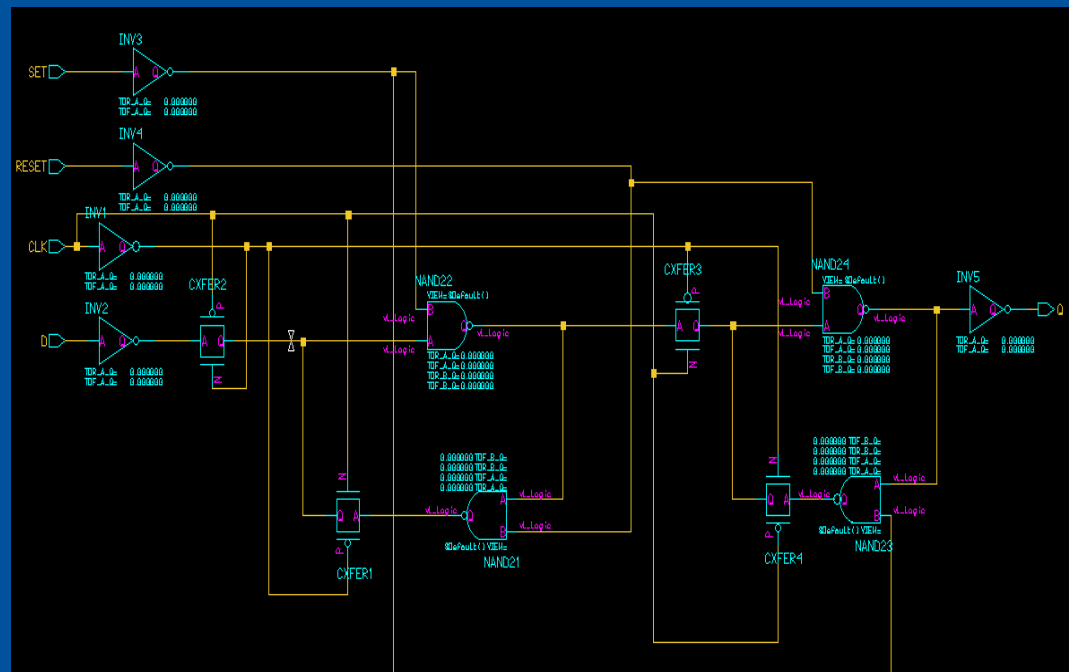
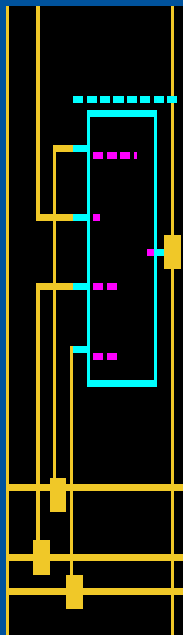
2-Input XOR Gate

- 2-input XOR gate \rightarrow 2 inverters & 2 transmission gates
 - $\rightarrow 4+4=8$ transistors



D Flip Flop

- Implementation: 4* 2-Input NAND gates, 4 transmission gates, 5 inverters



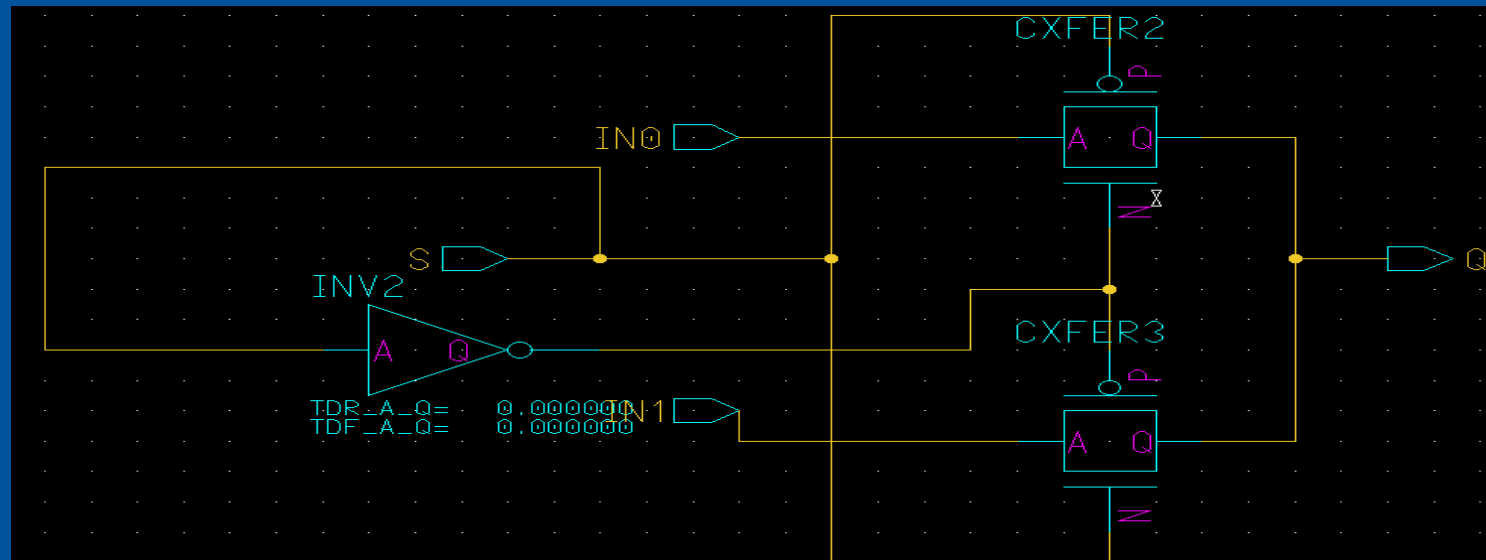


Number of Transistors in CRC

- 3*8-input XOR gates \rightarrow 21*2-input XOR gates \rightarrow 21*8=168 transistors
- 1*7-input XOR gates \rightarrow 6*2-input XOR gates \rightarrow 6*8=48 transistors
- 1*6-input XOR gates \rightarrow 5*2-input XOR gates \rightarrow 5*8=40 transistors
- 7*5-input XOR gates \rightarrow 28*2-input XOR gates \rightarrow 28*8=224 transistors
- 4*4-input XOR gates \rightarrow 12*2-input XOR gates \rightarrow 12*8=96 transistors
- 16*2-input XOR gates \rightarrow 16*8= 128 transistors
- 4*2-Input NAND gates \rightarrow 4*4=16 transistors
- 4 transmission gates \rightarrow 4*2= 8 transistors
- 5 inverters \rightarrow 5*2=10 transistors
- 738 transistors used in the CRC design

Mux Design

- 16 2*1 MUX used:



- 2 transmission gates and 1 inverter in the MUX
- $16 * (2 * 2 + 2) = 96$ transistors used



NOR16 Design

- Four OR4 & One NOR4
 - Each OR4 = 3 OR2
 - Each NOR4 = 2 OR2 + 1 NOR2
 - Total = 14 OR2 & One NOR2
-
- $14 * 6 + 4 = 88$ transistors used



Total Number of Transistors

- CRC Encoder, CRC Decoder, 16 2*1 MUX
- NOR16 Gate

❖ $738 + 738 + 96 + 88 = 1660$ transistors



Power Estimations

- Power Consumption
 - Dynamic Power
 - Assume $f = 30$ MHz, $\bar{\alpha} = 1$
 - Short circuit Current
 - Not considered – rise/fall times are ideal because we used standard cells.
 - Static Power
 - Ratio Power – Not a factor
 - Leakage – Assume worst case



Power Estimations

- Max Dynamic Power:

- $P_{dy} = \bar{\alpha} C V_{DD}^2 f = \bar{\alpha} C V_{DD}^2 f = \bar{\alpha} C_g W_g V_{DD}^2 f =$
 $(1/2)(2 * 10^{-15} \text{F}/\mu\text{m})(7 \mu\text{m})(5 \text{V})^2(3 * 10^7 \text{s}^{-1}) =$
 $5.3 \mu\text{W}$ per Transistor.

- 1,660 Transistors * 5.3 μW per Transistor =
8.80 mW



Power Estimations

- Leakage Power
 - Static Power = Leakage Power = Number of transistors * Leakage power of 1 transistor
 - $P_{st} = P_{leak} = N_{tran} * P_{leak_1}$
 - $V_{dd} = 3V$; $W = 6 \mu m$;
 - $I_{leak}/W = 6.506 \text{ nA}/\mu m$ (Current Leakage per unit width assuming half good devices and half bad devices)
 - $I_{leak} = W * I_{leak}/W = 39 \text{ nA}$;
 - **$P_{st} = N_{tran} * V_{dd} * I_{leak} = 0.194 \text{ mW}$;**