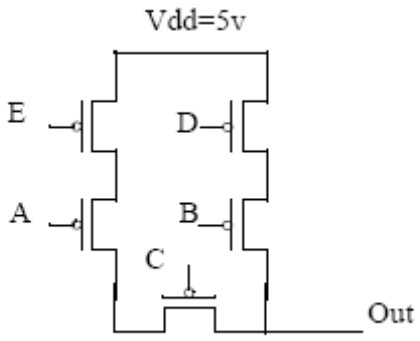
Homework 1

Assigned Sept. 6; Due: Sept. 16, 1pm During Bang-Ning office hours in DSIL lab

You are required to work on the homework on your own. Please be legible and state all assumptions clearly.

Show all work in order to receive partial credit.
1) [20 points]
Sketch two transistor-level schematics and truth table for the following:
a) CMOS 3-input XNOR gate (5pts)
b) Complex gate function F=A+E(B+CD) (15pts)
Assume the inputs are available in both the complemented and uncomplemented forms. Your design must consist of only a single stage of logic.

2) [10 points]
Design a pull-down circuit corresponding to the pull-up circuit shown below for implementing the function



3)[5 points]
a)Textbook, Page 108, Problem 2.1.

4)[5 points]
Textbook, Page 108, Problem 2.2a

5)[5 points]
Textbook, Page 110, Problem 2.15

6) [5 points]
Textbook, Page 111, Problem 2.21.