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OBJECTIVE

Permanent position with a leading VLSI/CAD company in the areas of VLSI design, system-on-a-chip design and test, and CAD. My strengths include a solid academic background, research experience in VLSI design and system-on-a-chip test, keen analytic ability, and well developed technical communication skills.

EDUCATION

Duke University

PhD candidate in Computer Engineering Graduating September 2002
Research: *Plug-and-play test architectures for system-on-a-chip*
Advisor: Dr. Krishnendu Chakrabarty
Honours: IBM Graduate Fellowship 2001
Coursework: Solid-state devices, Fault-tolerant computing

University of Illinois at Urbana-Champaign

PhD candidate in Computer Engineering August 1998–December 1999
Research: *Design Verification of Pipelined Microprocessors*
Coursework: Advanced Computer architecture, Large scale IC design, Combinatorial algorithms

Boston University

Master of Science in Computer Engineering May 1998
MS Thesis: *Built-in test pattern generation using precomputed test sets*
Honours: Electrical, Computer and Systems Engineering Chair Fellowship
Coursework: VLSI Principles and Applications, CAD Tools for VLSI Design, Computer Hardware Testing

Birla Institute of Technology, India

Bachelor of Engineering in Electrical and Electronics Engineering June 1996
Senior project: *Applying machine vision techniques for object recognition*
Coursework: Digital Systems Design, Computer-aided Network Analysis

WORK EXPERIENCE

- 1. Philips Research Laboratories**, Eindhoven, The Netherlands April 2001–July 2001
Engineering intern–System-on-a-chip test
Conducted research on test access architecture for IP cores
Manager: Erik Jan Marinissen
- 2. IBM Corporation.**, Burlington, VT June 2000–August 2000
Engineering intern–ASIC Test Group
Conducted a series of experiments designed to evaluate the efficiency of test point insertion into ASICs to improve built-in self test and system-on-chip level ASIC testability.
- 3. IBM-Motorola PowerPC Group.**, Austin, TX July 1999–August 1999
Engineering intern–Design verification
Developed a tool to automatically create bias specifications for use by Motorola's biased-random instruction generator. The test cases created were intended to be used for verification of the PowerPC.
- 4. University of Illinois**, Electrical and Computer Engineering September 1998–December 1999
Research Assistant
Conducted research in design verification of pipelined processors. I used genetic algorithms and formal verification techniques to derive high-quality biased-random tests for processors.

5. **Chrysalis Symbolic Design Inc.**, Boston, USA May 1998–August 1998
Engineering intern–Performance quantification
Performed a series of verification experiments on industry benchmark circuits to measure the performance of the Chrysalis model checker. A number of my suggestions for design modification were incorporated into later versions of the tool.
6. **Boston University**, Reliable Computing Laboratory June 1997–May 1998
Research Assistant
Performed research in sequential circuit test compression, and built-in test for embedded cores.
7. **Boston University**, Department of Electrical and Computer Engineering September 1996–May 1997
Teaching Fellow
Assisted with the teaching of courses SC752 Computer Hardware Testing, SC453 Engineering Electromagnetics and SC312 Small Computer Systems
8. **TATA-Cummins Ltd**, India, Auto-engine Facility May 1995–June 1995
PLC Programmer
Participated in the project, “Sequence Automation of the TATA-CUMMINS’s AGV (automatic guided vehicle) based materials handling system.” The project involved a detailed study of the circuits controlling the AGV developed at TATA-Cummins, and programming a SIEMENS Simatic S5 PLC

RESEARCH

I am interested in all aspects of computer-aided design of integrated circuits and systems, including synthesis, verification, layout and test. At Boston University I worked in the areas of sequential circuit test compression, built-in self test and embedded core test. At the University of Illinois, my research was in design verification for pipelined processors. At Duke University, I am conducting research on developing robust test access architectures for testing embedded-core based systems-on-chips.

PUBLICATIONS

Books and Book chapters

- K. Chakrabarty, V. Iyengar and A. Chandra, *Test Resource Partitioning for System-on-a-Chip*, Kluwer Academic Publishers, Norwell, MA, 2002, to appear.
- V. Iyengar and E. Rudnick. Design verification, in *The VLSI Handbook*, W-K. Chen (ed.). CRC Press, Boca Raton, FL and IEEE Press, New York, NY, 2000.

Journal articles

- V. Iyengar and K. Chakrabarty. Test bus sizing for system-on-a-chip. *in IEEE Transactions on Computers*, 2002, to appear.
- K. Chakrabarty, B. T. Murray and V. Iyengar. Built-in test pattern generation using twisted ring counters. *IEEE Trans. on VLSI Systems*, vol. 8, pp. 633–636, October 2000.
- T-C. Chang, V. Iyengar and E. Rudnick. A biased-random instruction generation environment for architectural verification of pipelined processors. *JETTA*, vol. 16, pp. 13–27, Feb. 2000.
- V. Iyengar, K. Chakrabarty and B. T. Murray. Deterministic built-in self testing of sequential circuits using precomputed test sets. *JETTA*, vol. 15, pp. 97–114, Aug. 1999.
- V. Iyengar, K. Chakrabarty and B. T. Murray. Huffman encoding of test sets for sequential circuits. *IEEE Trans. on Instr. and Meas.*, vol. 47, no. 1, pp. 21–25, Feb. 1998.
- V. Iyengar and K. Chakrabarty. An efficient finite-state machine implementation of Huffman decoders. *Information Processing Letters*, vol. 64, no.6, pp. 271–275, Jan. 1998.

Conference papers

- V. Iyengar, K. Chakrabarty and E. J. Marinissen, “Test wrapper and test access mechanism co-optimization for system-on-a-chip. *Proc. IEEE International Test Conference*, pp. 1023–1032, 2001.

- V. Iyengar and K. Chakrabarty. Iterative test access mechanism optimization for system-on-a-chip. *IEEE International Workshop on Testing Embedded Core-Based System Chips*, 2001.
- V. Iyengar and K. Chakrabarty. Test wrapper and test access mechanism co-optimization for system-on-a-chip. *IEEE European Test Workshop*, 2001.
- V. Iyengar and K. Chakrabarty. *Precedence-based, preemptive and power-constrained test scheduling for system-on-a-chip*, IEEE VLSI Test Symposium, pp. 368–374, 2001.
- H. Date, V. Iyengar, K. Chakrabarty and M. Sugihara. Mathematical modeling of intellectual property protection using partially-mergeable cores. *Proc. IEEE International Conference on Parallel and Distributed Processing Techniques and Applications*, pp. 611–617, 2000.
- V. Iyengar, M. Sugihara, H. Date and K. Chakrabarty. Intellectual property protection using partially-mergeable cores. *IEEE Testing Embedded Core Systems Workshop*, pp. 4.3.1-4.3.6, 2000.
- K. Chakrabarty, B. T. Murray and V. Iyengar. Built-in test pattern generation for high-performance, core-based circuits using twisted ring counters *Proc. IEEE VLSI Test Symp.*, pp. 22-27, 1999.
- V. Iyengar, K. Chakrabarty and B. T. Murray. Deterministic built-in self testing of sequential circuits using precomputed test sets. *Proc. IEEE VLSI Test Symp.*, pp. 418–423, 1998.
- V. Iyengar, K. Chakrabarty and B. T. Murray. Test set encoding for efficient sequential circuit testing. *Proc. IEEE Instr. and Meas. Tech. Conf.*, pp. 1442–1447, 1997.
- V. Iyengar, K. Chakrabarty and B. T. Murray. Built-in self testing with complete fault coverage and practical test application time. *Proc. IEEE N. Atlantic Test Workshop*, 1997.

Web articles

- V. Iyengar, A. Chandra and K. Chakrabarty. University research in system-on-a-chip testing, *EDA Vision* (www.edavision.com), vol. 1, issue 3, September 2001.

COMPUTER SKILLS

Languages: C/C++, VHDL, 8086/68K Assembly

CAD tools: Mentor tools, Chrysalis tools, Spice, Epoch (Cascade Design), Magic

Software: Matlab, LaTeX, HTML, MS Word, Idraw

ACTIVITIES

Professional memberships: IEEE; IEEE Test Technology Technical Committee

Activities: Birla Tech—Secretary, IEEE student branch; Senior Editor, News and Publications Society

REFERENCES

<p>1. Dr. Krishnendu Chakrabarty Assistant Professor Electrical & Computer Engineering Duke University, Durham, NC 27708 E-mail: krish@ee.duke.edu Tel: (919) 660-5244, Fax: (919) 660-5293</p>	<p>2. Dr. Hisham Z. Massoud Graduate Chairman & Professor Electrical & Computer Engineering Duke University, Durham, NC 27708 E-mail: massoud@ee.duke.edu Tel: (919) 660-5442, Fax: (919) 660-5293</p>
<p>3. Erik Jan Marinissen Senior Member of Research Staff Philips Research Laboratories Eindhoven, The Netherlands E-mail: erik.jan.marinissen@philips.com Tel: +31 40 27-43227, Fax: +31 40 27-44113</p>	<p>4. David Newman Manager ASICs Test group IBM, Burlington VT E-mail: dnewman@us.ibm.com Tel: (802) 769-6992</p>
<p>5. James Monzel Senior Technical Staff Member ASICs Test group IBM, Burlington VT E-mail: jmonzel@us.ibm.com Tel: (802) 769-6428</p>	<p>6. Brion Keller Senior Technical Staff Member IBM TestBench Architecture Endicott, NY E-mail: kellerbl@us.ibm.com Tel: (607) 755-8231, Fax: (607) 755-5608</p>