Microprocessor Errors/Failures

- **Error models**
  - Transient stuck-at (bit flip) on transistor or wire
  - Hard stuck-at on transistor or wire
  - Chipkill: whole chip is dead (e.g., due to power/ground short)

- **Failure models**
  - Incorrect instruction → trap/exception
  - Incorrect output
  - Dead chip (no output and/or smoke output)

Microprocessor Fault Tolerance

- **There ain’t much!**

- Most common microprocessors are designed to maximize performance per dollar
  - Intel Core2 (2- and 4-core)
  - AMD Phenom (2-, 3-, and 4-core)
  - Intel Itanium II (1- and 2-core)
  - Sun UltraSPARC IV, UltraSPARC T2 (Niagara 2)
  - IBM Power6 (2-core) → has the most fault tolerance in this list

- Microprocessors may have some limited error detection/correction in their L2 or L3 caches

- Note: microprocessors are designed with hardware for performing built-in self-test (BIST). We will cover this topic towards the end of the semester.
Fault Tolerance in Custom Microprocessors

• Most systems built from commodity microprocessors
  – Off-the-shelf parts are cost-efficient
  – And, even if they’re not very reliable individually, we can design
    reliable systems out of un-reliable parts (remember Teramac!)

• However, custom microprocessors may be built for
  those systems which require very high availability
  and/or reliability

• Example: IBM mainframe microprocessors (e.g., G5 and G6)

Fault Tolerance in the DEC VAX

• DEC’s VAX was very successful family of systems
  – Follow-ons to DEC’s PDP-11 computer
  – Forerunner of DEC/Compaq/Intel Alpha processor (now dead)
  – VAX known today for being epitome of CISC-ness

• Could detect and sometimes tolerate many faults
  – Illegal instruction execution
  – Trying to access restricted memory
  – Arithmetic exceptions (which may be due to faults)
  – Power failure
  – Etc.

• Tries to provide info with trap/interrupt
  – Places fault type info into known location

• Maintains registers specifically for error monitoring

More About the VAX (1978-1987)

• Early VAX-11/750 and VAX-11/780 had following FT
  – Built-in self-test (executed at power-on)
  – ECC on main memory
  – Multiple-bit parity on cache, TLB, and a few other structures
  – Parity bits on the SBI (synchronous backplane interconnect = bus)
  – Field-replaceable unit (FRU) is the chip (instead of board)

• In the later VAX 8600 and 8700, more FT added
  – Instruction retry
  – Better diagnostics through error logging and analysis
  – Online self-test of floating point unit (F-box in VAX lingo)
  – Error handling via a microcode routine (“micro-routine”)
  – Micro-diagnostics to self-test system and diagnose faults to FRUs
  – System diagnostic bus (SDB) for console control/observation

IBM RAS

• “RAS Strategy for IBM S/390 G5 and G6” (Mueller et al.)
Argus