Homework#2 for ECE 254 / CPS 225
Due in class on Monday, Sept 29

All homework must be done either individually or in a group of two

1 Physical/Spatial Redundancy
1.1) [15 points] You are given a choice between using TMR or 5MR to improve the availability of your system. The probability of any individual module incurring an error is 0.2, and errors in modules are independent. The cost of a system is directly proportional to the number of modules it has. Your goal is to minimize cost * Prob[system error]. Do you choose TMR or 5MR? Show your work.

1.2) [15] You are given the choice between producing either 100 Teramac-like chips OR 60 more traditional chips (the numbers of each chip type are different to equalize the cost of fabrication). Each type of chip has N devices on it. For the Teramac: the defect rate is 10/N, and the fraction of the chip that is critical logic is N/40. Assume that the chip achieves performance of either zero (if critical logic is defective) or 2P/3 if not. For the traditional chips: the defect rate is 1/(10N), and the performance is either zero (if any logic is defective) or P if not. The profit per chip (for both chips) is the chip’s performance times $100. Which type of chip would you produce to maximize your profit? Show your work. Assume for both chip types that defects are not clustered (i.e., don’t make this problem tougher than it needs to be).

2 Temporal Redundancy
2.1) [10] AR-SMT can introduce some new fault possibilities—list three. Do these drawbacks outweigh AR-SMT’s benefits?

2.2) [10] Temporal redundancy is used in network hardware more often than in general software. Why?

2.3) [15] One non-trivial problem with Razor is the possibility of causing a metastable circuit state. Discuss (in less than half a page) what metastability is, why it scares circuit designers (i.e., what problems can it cause), and ways to deal with it.

3 Information Redundancy
3.1) [10] What Hamming distance is required to be able to both correct 3-bit errors and detect 5-bit errors? Show your work.

3.2) [15] Describe (in roughly half a page) an EDC or ECC that I have not covered in class. Explain its primary features, including its cost, implementation, error model, and where it is commonly used.

4 General Fault Tolerance Concepts
4.1) [10] What kinds of redundancy might be used when swiping a DukeCard (or ATM card) through a reader?
4.2) [10] What types of redundancy are appropriate for real-time computer systems (e.g., embedded computer that controls your car brakes)? Explain your answer.