ECE 252 / CPS 220 Homework #4
Due in class on Weds, Nov 9 (submission of Q7 due by 10:00 am)
Total Points 100

Explain all of your answers to get full credit! You may NOT work with other people on
this assignment. I will not tolerate academic misconduct.

Static ILP
1) (10 points) H&P 4.8
2) (10 points) H&P 4.21

Memory Hierarchies and Caches
3) (10 points) Assume a 32-bit machine with a 64 KByte cache (total, but not including
tags) and 32-byte blocks. Assume the cache is 2-way set associative. For the address
0x1300fb18, what are the tag, index, and offset? Please write your answers in binary.
4) (10 points) Assume you have a cache with exactly 8 frames and that there is one word
per frame. Compare direct-mapped vs. fully associative for the following stream of
accesses: 1, 2, 3, 4, 5, 6, 7, 8, 9, 1, 2, 3, 4, ... (repeating sequence of 9 addresses). What les-
son do you learn from this experiment? Would a victim cache help?
5) (10 points) When might it make sense for a cache hierarchy NOT to enforce inclusion?
(Inclusion means that any block in the L1 must be in the L2.) Hint: think about the possi-
ble relative sizes of the two caches.
6) (10 points) H&P 5.13a (only part a!).

Exploring Caches with SimpleScalar
7) (40 points) We will use sim-outorder for this set of three experiments. Use the default
simulator parameters unless instructed otherwise.

Experiment #1: Explore the tradeoff between associativity and hit latency for a 4KByte L1
data cache by comparing the performance of (a) 1-cycle direct-mapped cache, (b) 2-cycle
2-way set-associative cache, and (c) 3-cycle 4-way set-associative cache. Do not modify
the other default characteristics of the L1 D$ (e.g., block size, total cache size, replace-
ment policy). However, note that sim-outorder makes you specify the number of sets—
make sure that the caches you specify are all 4 KB in total size (not including tags)! This
experiment requires no modification to sim-outorder.

Experiment #2: Add a 2-entry fully-associative victim cache (with LRU replacement) to
this L1 D$. The victim cache can be accessed in parallel with the L1 D$, and a hit in the
victim cache has no performance penalty (i.e., takes the same time as an L1 D$ hit). How
much does this help the direct-mapped cache? How about the 2-way and 4-way set-asso-
ciative caches?
Experiment #3: Explore the importance of caching for out-of-order processors by comparing a 1K vs. 4K direct-mapped L1 DS for both in-order and out-of-order processors (use the default configuration for all other parameters). This experiment requires no modification to sim-outorder.

Analysis: Explain what you have learned from these experiments, including (but not strictly limited to) the following: (a) explain how you might to choose to trade-off associativity versus hit latency, and (b) explain what the results in experiment #3 say about the relative importance of the L1 D$ for in-order versus out-of-order processors.

Submit your code for sim-outorder with the victim cache in the usual way (upload it with the name homework4.c).