Homework#6 for ECE 152
Memory Hierarchies, Caches, Memory (Chapter 5)

Hardcopy is due in class on Monday, April 11
Problem 5 must be submitted electronically by 10:00am on April 11

1) [10 points] Patterson & Hennessy 5.10.2

2) [5] P&H 5.10.4b

3) [10] P&H 5.10.5b

4) [5] P&H 5.11.1b

5) [**100 points**] Write a simulator of a single-level cache, using the high level language of your choice (Java, C++, C). The simulator, called cachesim, takes the following input parameters on the command line: name of the file holding the loads and stores, cache size (not including tags or valid bits) in KB, associativity, block size in bytes, and replacement policy (either LRU or NMRU). For example, "cachesim tracefile 32 4 8 lru" should simulate a cache that is 32KB, 4-way set-associative, has 8-byte blocks, and uses LRU replacement. This cache will be processing the loads and stores in the file called tracefile.

Assumptions: Addresses are 32-bits. The cache size, associativity, and block size will all be powers of 2. All cache blocks are initially invalid. All cache misses are satisfied by the main memory. If a block has never been written before, then its value in main memory is zero.

The trace file will be in the following format. There will be some number of lines. Each line will specify a single load or store, the address that is being accessed (in Hex), the size of the access (in bytes), and the value to be written if the access is a store (in unsigned decimal). For example:

```
store 0x1234abcd 4 152
load 0x002a173f 2
```

Your simulator must produce the following output. For each access, it must print out whether it is a hit or a miss. For each load, it must print out the value (in unsigned decimal) that is loaded. You may assume that the access size is less than or equal to the block size.

Submit this assignment in the same way in which you have been submitting project parts. Create a single file called cachesim.tar.gz. Include in this file your simulator file(s) and a README for building and running the simulator. If you have any known remaining bugs, please also include those in the README file.