

Project: Part #6 for ECE 152

Pipelined Processor

200 points

Must be submitted electronically by 10:00AM on Wednesday, April 9

IMPORTANT: Please get started early! That way, when problems arise (which they will!), you will have time to ask me and/or the TAs for help.

In this part of the project, you will pipeline the processor that you built in the previous part of this project.

As part of this project, you will:

- Demonstrate that your design works correctly in Quartus and show how fast it can execute a test program that I have provided for you at: <http://www.ee.duke.edu/~sorin/ece152/project/testprogram1.sim>.
- Download your design into the FPGA prototyping board, demonstrate that it works, and show how fast it can execute my test program.

Recall that the specification for the Duke 152/16 architecture can be found at: <http://www.ee.duke.edu/~sorin/ece152/project/duke152-arch.pdf>

1 Requirements

This processor has the exact same requirements, as far as functionality is concerned, as the previous part of the project. It must implement the ISA that I specified. The new twist is that you must pipeline your processor into at least 5 stages.

Data Hazards. Whenever data bypassing is possible, you must use it to avoid data hazards. If a stall is inevitable, the hardware is responsible for managing the stall (inserting a bubble in the pipeline).

Control Hazards. When you encounter a branch or jump, it is completely acceptable for you to wait until it is resolved before fetching another instruction. However, I encourage groups to consider higher performance options, such as adding a simple branch predictor. At the end of the semester, when the highest performing processors earn bonus points, it is

very likely that these winners will have implemented some feature(s) to handle control hazards.

2 Hardware Demos

As with the previous part of the project, we will have graded demos of the FPGA implementations that will be held in the ECE 154 lab (Hudson 202A) just after the submission deadline (exact times to be announced later). You will want to test your designs on the hardware long before then, to make sure they work correctly (even if they worked without problem in Quartus). To provide you with access to the lab with the prototyping boards (Hudson 202A), the TAs will hold office hours in the lab during the last week before the project is due.

3 Submission

Submit this assignment in the same way in which you submitted previous project parts. You must name your high-level .bdf file `pipelined.bdf`. There are no other file naming restrictions.

You may re-submit as often as you like, but a re-submission will overwrite whatever you've previously submitted for this assignment. I will grade whatever has been submitted before 10:00AM on Wednesday, April 9.