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Design tools for a DNA-guided self-assembling carbon nanotube technology

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Abstract
The shift in technology away from silicon complementary metal–oxide semiconductors (CMOS) to novel nanoscale technologies requires new design tools. In this paper, we explore one particular nanotechnology: carbon nanotube transistors that are self-assembled into circuits by using DNA. We develop design tools and demonstrate how to use them to develop circuitry based on this nanotechnology.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

The rapid advance of silicon technology towards single-nanometre device feature sizes and the foreshadowed difficulties with these developments are driving research into alternative technologies and architectures that can either replace or supplement existing silicon technologies [1]. Researchers are exploring novel nanoscale components, such as carbon nanotube transistors, as well as techniques for integrating these components into circuits. Existing top-down fabrication technology (i.e., photolithography) cannot resolve dimensions as small as desired, which has spurred research in self-assembling fabrication processes.

We are exploring one particular set of nanotechnologies, carbon nanotube field-effect transistors (CNFETs), that are self-assembled using DNA as a scaffolding. CNFETs have been demonstrated to exhibit excellent switching properties [2–6]. To fabricate a circuit out of CNFETs, which are of the order of 1–2 nm in diameter (far smaller than current photolithographic capabilities), we plan to exploit the self-assembly properties of DNA. Strands of DNA connect to each other if the base pairs on the strands are complementary. Our proposed technology is fabricated by using lattices of DNA as shown in figure 1 [7].

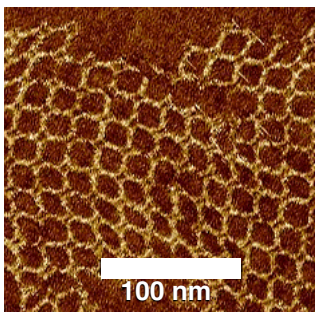

Figure 1. AFM image of a DNA lattice.

Then, by attaching a tag of single-strand DNA (ssDNA) to a specific point on the lattice and the complementary ssDNA tag to one end of a nanotube (which is called functionalization of the nanotube), we could programmably attach that end of the nanotube to the scaffold [8]. The precursor work for this has recently been demonstrated by making a back-gated CNFET with source and drain leads using metallized DNA strands [9].

We plan to use multiple pairs of DNA tags to create different connections on the lattice, in order to connect both ends of multiple nanotubes to the scaffold. If we attach two nanotubes such that they are perpendicular and cross each

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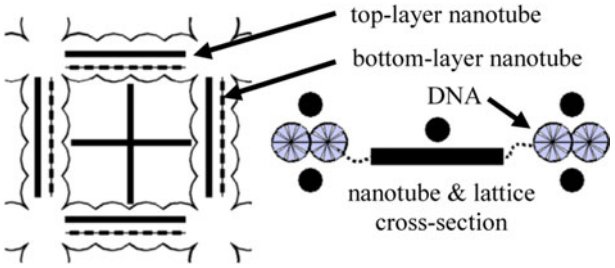

Figure 2. Schematic of the DNA lattice scaffold.

other, the top one (chosen to be metallic) acts as a gate and the bottom one (chosen to be semiconducting) acts as a channel in a CNFET. Figure 2 shows cross-connected nanotubes spanning cavities in the DNA lattice. We also plan to attach single nanotube wires to each side of each cavity. To implement a connection between two nanotube wires, we will specify a DNA tag at the gap between the wires that attracts a metallic nanosphere that later serves as a nucleation site for chemical electroless plating. By programmably attaching CNFETs and specifying wire connections, we will fabricate circuits with this technology.

However, due to current limitations in DNA self-assembly technology we do not believe that we can create lattices greater than $\sim$2 μm on a side. Thus, the functionality on any given lattice is limited. To develop large-scale systems, we plan to interconnect multiple lattice nodes. We are currently exploring computer architectures that are amenable to this kind of computational substrate. The focus of this paper is on the computer-aided design tools needed for this work.

To design lattice circuitry, we need various custom design tools to facilitate the new technology. For example, we need to be able to specify where nanotubes assemble onto the lattice and specify their connectivity. Since placement and routing are produced by DNA self-assembly, these processes require design tools that can choose DNA tags (i.e., which sequence of base pairs) for the scaffolding and for functionalizing the nanotubes. Unlike existing design tools for silicon CMOS technology, our tools must produce DNA tag sequences rather than mask artwork.

In this paper, we present the design tools and flow we have developed for the design of self-assembled circuitry. Section 2 describes our method and illustrates where we have introduced custom tools to handle the new technology. We also briefly describe a computer architecture that we have developed that is amenable to the self-assembling technology and the behavioural simulator we are using to explore architectural design. Section 3 describes the application of our design tools to several logic circuits. These results demonstrate a new capability in designing self-assembled circuitry.

2. Methodology

In this section, we present our design methodology. We begin with a high-level overview of the design flow, and then we discuss the architectural, circuit, and DNA level design flows.

2.1. Overview

Figure 3 illustrates the design flow we have applied to the self-assembling process. The highlighted path through figure 3 illustrates the sequence of deliverables (in italics) from the process. The design flow begins with an architectural description that is used to manually create a behavioural simulator that can verify the high-level procedural operations of the system. Once verified, the behavioural description can be used to manually capture gate-level modules for input to a complementary transistor synthesis tool. We have focused our efforts on the generation of layout for our process assuming a transistor level module description. Once a feasible layout has been generated and verified it is used to create an ordered set of DNA sequence allocations for fabrication. The allocation process orders the assembly of the circuit so that a constant number of DNA sequences can be used independently of the circuit size.

2.2. Architectural design

The larger context of our project is to develop self-assembled computing systems, and this requires behavioural design and simulation tools. We have developed an active network architecture that is amenable to self-assembly, and we briefly describe the system here to motivate our device-level design tool work.

The limited circuit size in our self-assembling technology precludes making single circuits that can perform all operations. Instead, we assemble several different circuit (node) types (e.g., ALU, memory) into a larger network. For ease of fabrication, nodes are randomly interconnected with

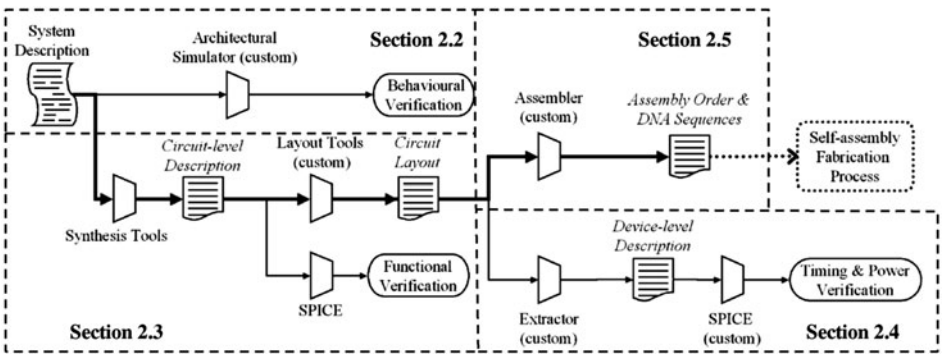

Figure 3. Design tool flow.

bit-serial links. The large-scale network of nodes is divided into cells, each of which has a via that connects it to the micro-scale. A configuration phase at system startup imposes some limited structure on this otherwise random sea of nodes. Configuration maps out defective nodes and links, organizes the memory nodes into a memory system, and establishes routing options within the network.

We have developed a custom simulator to model a single cell at the bit-serial link level to capture network communication behaviour. A detailed treatment of the system and its configuration and execution model can be found elsewhere [10]. We have included this brief overview here as motivation for our tool development and as an example behavioural simulation tool that addresses some of the issues of designing nanoscale self-assembled systems. The behavioural simulator models system-level aspects of this self-assembling technology including node interconnections. The remainder of our tools focus on the design of individual nodes.

2.3. Circuit design

The complete circuit description for the architecture described in section 2.2 is not presented here. Instead we demonstrate our process for a NAND gate, full-adder, and SR-latch. The circuit level flow begins with a device (transistor) level description of the system generated by the synthesis tools; in our case, a suite of tools from Mentor Graphics, Inc. produces this output. The transistor netlist is used to verify the functional properties of the circuit using a switch-level simulator. The unique constraints of our self-assembling process ($\sim 100 \times 100$ FETs) make large circuits infeasible. Fortunately that means that a high resolution SPICE simulation can be used to verify circuit functionality before the layout process. In this limited sense, the self-assembling technology simplifies the design flow compared to a conventional technology because it forces system architects to explicitly partition their designs.

The layout process can include automated tools and/or manual full-custom steps. Our custom layout tools provide an interface for manual layout and the exploration of design spaces through automated techniques. The constrained circuit sizes in our technology appear to make it more feasible to apply fully automated layout generation to the entire system than with conventional technologies.

The generated layout is used by a custom circuit extractor to back-annotate the original circuit with wire models and additional parasitics derived from the geometry of the layout. This requires the extractor to model the as-fabricated structure of the circuit and use geometric relationships to refine the circuit. The back-annotated circuit is simulated by the modified SPICE kernel and empirical device models as described in section 2.1. The results of this simulation are used to verify the timing and power constraints of the circuit and can be used to make decisions that feedback to the system description and earlier design process.

2.4. Device design

The device level flow begins with the transistor level description of the logic module that has been synthesized and optimized by a logic design tool. This description is first verified using a switch-level simulator and then fed to a custom automated place and route layout generator. A SPICE deck is then extracted from the generated layout to estimate performance including wire delays and other parasitics. We use a modified SPICE 3f5 kernel similar to [11] and a custom semi-empirical device model for the CNFETs and parasitics [6, 12] to estimate the performance of the circuitry. Our results are consistent with the reference data used in our models and recent observations of CNFET performance [2, 13].

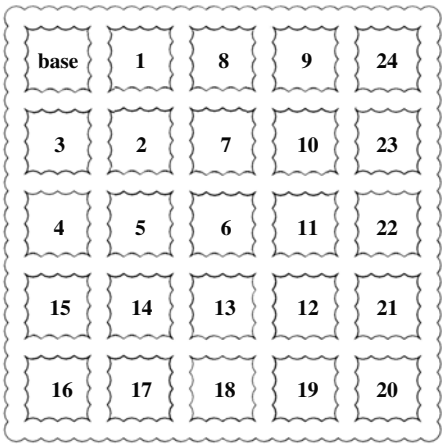

Figure 4. The assembly order follows a radial boustrophedonic pattern to build the lattice.

2.5. Self-assembled DNA design

The layout is used by a custom assembler, a tool that renders the layout into an ordered sequence of assembly steps and DNA tag identifiers as well as the self-assembling components (nanotubes or nanoparticles) to which the tags must be attached.

The assembler uses the stitching algorithm illustrated in figure 4 to order the DNA tag allocations. This pattern is better than simple line scans because it minimizes the span of the lattice at all stages, which appears to be important in forming planar DNA lattices [7].

Our assembly ordering assumes a single 'active' cavity (i.e., one available for binding nanotubes, etc) in the scaffold at each step in the process. That is, we assume that the scaffold is extended in the direction of the next cavity (as specified by the assembly pattern) before each assembly step. To prevent components from binding to previously assembled cavities the lattice can be passivated with short DNA fragments that bind to unused locations on the cavity after each assembly step.

At each step the assembler generates the tags and components specified in the layout for that cavity. Figure 5 illustrates the positions of each tag in the cavity.

Each position has four associated orientations: north, east, south, and west. That is, a DNA tag can bind a component at any of its orientations. Further, nanoparticles bind to a reserved portion of the DNA tag and do not prevent nanotubes from binding to the same tag (i.e., nanotubes have their own portion as well).

A tag and orientation are specified for each attachment point of a component. For example, a nanoparticle can be specified with a single tag and orientation. The specifier N7

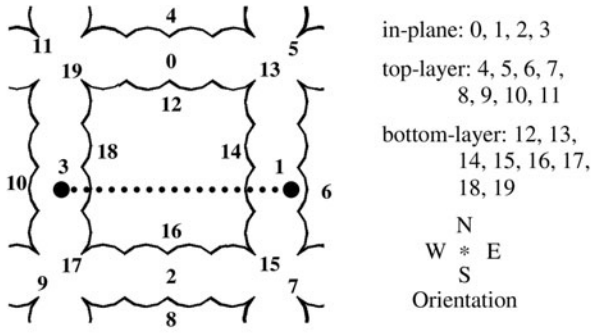

Figure 5. Tag location legend. Each number represents the location of a DNA tag. 'N', 'E','S', and 'W' designate an orientation with respect to the location.

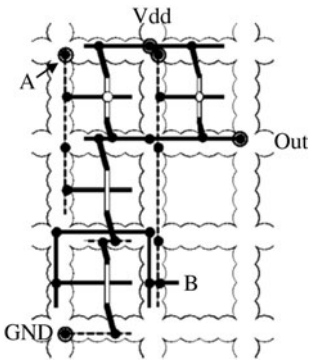

Figure 6. NAND gate layout (boundary cavities have been removed).

represents the north (side) of location 7. A nanoparticle at N7 and a nanotube connecting (N7, S5) will fuse during the metallization process.

The exact sequence of the DNA used for each tag is taken from a pool of sequences that are known not to interfere with each other. The pool is generated using binding energy minimization techniques to avoid cross-hybridization [14]. The size of this pool using our technology and this assembly ordering is 20 sequences. However, the number of DNA sequences required to form one additional active cavity in the scaffold lattice scales as the perimeter of the device grows, and minimizing this is a topic of future research.

The output from the assembler, the assembly ordering and DNA tag allocation, is then used to direct the self-assembly of the circuit. The remainder of this paper describes the application of our tools to several simple logic structures.

3. Case studies

We demonstrate our design methodology by designing a NAND gate, full-adder, and SR-latch. While these circuits are trivial, the process we have developed introduces the tools needed by this self-assembling technology.

Each circuit layout was generated manually and converted to a SPICE netlist for switch-level verification. The NAND and SR-latch layouts are illustrated in figures 6 and 7, respectively.

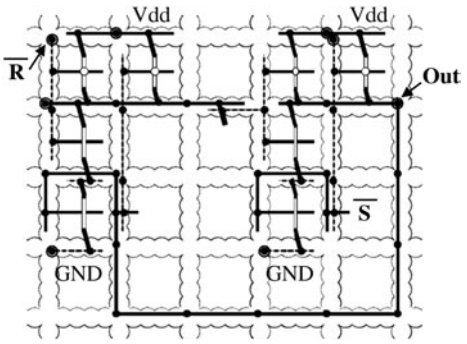

Figure 7. SR-latch layout.

Table 1. Layout features.

	Span (cavities)	Layout efficiency (FETs/cavity)
NAND	3×2	0.67
Full-adder	10×12	0.23
SR-latch	4×5	0.40

Table 2. Circuit performance.

Technology	Circuit	E_t (10^{-18} J)	t_d (ps)
CNFET	NAND	40	24
	Full-adder	192	104
	SR-latch	94	16
0.18 μm CMOS	NAND	19×10^3	60
	Full-adder	47×10^3	250
	SR-latch	28×10^3	140

Table 1 lists several simple measures of the NAND, full-adder, and SR-latch layouts.

Each cavity has an area of 4×10^{-4} μm^2 determined by the spacing of the DNA scaffold, which has been designed to span a 20 nm pitch. In terms of transistor density the cavity area corresponds to 2500 transistors μm^{-2} or approximately 30 times the density of current CMOS technologies (e.g., 65 nm CMOS has ~80 transistors μm^{-2}).

Table 2 lists the transition energies (E_t) and switching delay (t_d) for each circuit simulated using the method described in section 2.4. These results were obtained by loading each circuit output with an FO-4 inverter tree (i.e., four parallel inverters) and conditioning each square wave input through a series of four CNFET inverters. These testing conditions mimic typical circuit topologies by smoothing sharp input signals (i.e., sharp input signals can make a circuit appear faster) and placing realistic loads on the outputs. The results in table 2 are from the worst-case single-input transition event for each circuit. For comparison, simulation results from a 0.18 μm CMOS technology are included. The CMOS circuits here are identical to the CNFET circuits with the exception that CNFETs have been replaced with minimum size N-FET and P-FET transistors. The variation in the relative E_t and t_d between the circuits reflects poorly chosen transistor sizes (or multiplicity of CNFETs) and results in an imbalanced design. Even so, the performance improvement of CNFET logic over CMOS logic is evident.

In table 3, we illustrate the assembly sequence of the NAND gate as generated by our tool. Each row represents

Table 3. DNA sequence allocations and assembly order for a NAND gate. Each step is numbered.

Lattice extension	Active site	CNFETs	Metallic CNTs	Nanoparticles
0. Base 2. East 4. South	Site 2	**P-type**: 7. (S0, N2)	5. (E3, W1), 13. (S19, N17), 14. (E11, W5)	1. G15, 3. V7, 6. E18, 8. N8, 9. S4, 10. W5, 11. S19, 12. N17,
15. West 16. South 17. East	Site 5	**N-type:** 20. (S0, N2)	18. (E3, W1), 25. (S19, N17), 26. (E11, W5)	19. E18, 21. N16, 22. S4, 23. W5, 24. S19
27. East	Site 6		32. (S19, N17), 33. (E11, W5)	28. W5, 29. E11, 30. S19, 31. N17
34. North	Site 7	**P-type:** 37. (S0, N2)	35. (E3, W1), 43. (S19, N17), 44. (E11, W5)	36. E18, 38. N8, 39. S4, 40. E11, 41. S19, 42. N17
45. North	Site 8			46. G17
47. East 48. South	Site 10			49. V9
50. South 51. South 52. West	Site 13		55. (S11, N9), 56. (S19, N17)	53. S19, 54. S11
57. West	Site 14	**N-type:** 60. (S0, N2)	58. (E3, W1), 67. (S11, N9), 68. (E11, W5)	59. E10, 61. N16, 62. S12, 63. W5, 64. E11, 65. S11, 66. G17
69. West 70. South 71. East	Site 17		73. (E19, W13)	72. E19

a single active cavity (indicated by the number in brackets as specified in figure 4) and the assembly actions needed to complete it. For example, steps 0–2 are used to extend the lattice in a particular direction to follow the stitching pattern, and steps 3–14 assemble the components for the cavity (cavity 2 is active). In this table, 'V' indicates a Vdd connection (1.0 V) and 'G' indicates a ground connection (0 V). These connections could be made out of the plane of the lattice (or node) to microscale contacts above and below the lattice.

Some cavities are not used in this layout due to the placement of the circuit on an overly large lattice (in this case a 5×5 cavity lattice). Table 3 illustrates how tangled the self-assembly process can become even for trivial design problems (e.g., a NAND gate). This underscores the need for the continued development of design tools capable of handling this emerging technology.

4. Conclusions

The development of self-assembling technologies that can either replace or supplement existing silicon technologies requires new design automation tools because of the distinctions between self-assembling and conventional photolithography processes. This fundamental change in technology motivates the development of design tools that address these differences.

In this paper, we have presented the design tools for one such self-assembling circuit technology. The technology we explore, which uses DNA to programmably self-assemble the circuit components, requires different tools from those used for silicon CMOS design. Starting with a circuit description, we use tools for placement, routing, and electrical simulation to develop a viable circuit. We then use a custom tool to generate DNA tag sequences that will enable this circuit to be fabricated using self-assembly.

Future work will extend this tool chain beyond individual circuit nodes in order to encompass large-scale designs, including computer architectures.

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